Design and Simulation of Asymmetrical Multilevel Inverter with Reduced Switches

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Abstract: **In recent days, electronic devices are very sensitive to harmonics. The harmonic free and high power rating sources are increased to meet the requirement of industries. As conventional two level inverters are not able to provide good quality power, multilevel inverters are becoming more popular due to their ability to generate more output voltage with fewer harmonic. A new multilevel inverter topology with different magnitude of dc voltage sources has been introduced that requires lesser number of circuit components as compared to other topologies for same levels in output voltage. In this topology, minimum switches are required for generation of higher level output voltage. The method is easy to implement and simple. The extended version of this topology generates more number of output voltage levels. Both the operational accuracy and Total Harmonic Distortion (THD) of the output voltage have been evaluated using simulation in MATLAB environment. Asymmetrical multilevel inverters are mostly suited for high power and medium applications. A comparison is done on the basis of THD to check the performance accuracy of different voltage levels of Asymmetrical cascaded H-bridge multilevel inverter. The inverters are simulated and its results are verified through MATLAB/Simulink software.**

***IndexTerms - Asymmetrical, Multilevel inverter, Harmonics, Total Harmonic Distortion*.**

I. INTRODUCTION

Currently, many industries are in need of high power for many applications, and some of them also need medium and high power source based on the requirement of industrial loads. For this purpose only multilevel inverters has been introduced in the year of 1981as an alternative to high power and medium voltage situations. Multilevel inverter is a power electronic device which is used to produce pure sinusoidal voltage from several voltage levels of dc voltage. Mostly a 2 level inverter is used to generate the ac voltage from dc voltage. Its major work is to provide high output power from medium voltage source like battery, super capacitor, solar panel, etc. The concept of multilevel inverter is a modification of two level inverter. In a two level inverter only two different voltage levels like $+v_{dc}/2$ and $-v_{dc}/2$ are produced as an output for a vdc input. Even though this method of ac production is effective, it has a drawback of producing harmonic distortion in its output and also has a high dv/dt as compared to multilevel inverter type. So that more than two voltage levels are needed to produce a smoother stepped output waveform and the output waveform obtained here also has lower dv/dt and also has lower harmonic distortion [1-5]. Smoothness of the output voltage waveform depends on voltage level, when we increase the voltage levels it leads to smoothen the voltage waveform. But increase in voltage level makes the circuit complex as components increases.

Inverters are generally classified into two groups based on the value of dc voltage sources like symmetric and asymmetric multilevel inverter. The value of dc voltage source will be equal in symmetric inverter and value of dc voltage sources will be unequal in asymmetric multilevel inverter. The main objective of multilevel inverter is to give a high output power from medium voltage source. Low rated devices can be used to generate higher voltage. Increased number of voltage levels leads to produce pure sinusoidal output. It is necessary to reduce switching frequency for PWM operation. These are the some of the needs of multilevel inverter [6-10].

A Multilevel inverter is advantageous over other conventional inverter as it uses high switching frequency pulse width modulation. Few merits of them are given as follows

- They generate output voltage with reduced harmonic distortion and lower dv/dt stress and therefore electromagnetic compatibility will be reduced.
- It produces smaller common mode voltage and therefore stress developed in the bearings of motor connected to a drive can be reduced.
- It can operate in both fundamental switching frequency and high switching frequency PWM. Lower switching frequency leads to low switching loss and higher efficiency.
- They generate input current with low distortion.

But it also has some drawbacks like, need of more number of power semiconductor switches, which makes the system complex and overall system expensive [11-15]. For this reason multilevel inverters are planned with reduced number of switches and components, which satisfies our need. Multilevel inverters are broadly classified into two types based on the type of source we are using like common DC source and separate DC source. Common DC source are further classified into two types like Diode Clamped multilevel inverter and Flying Capacitor multilevel inverter. Likewise separate DC source are also classified into Cascaded H- Bridge multilevel inverter.

II. PROPOSED SYSTEM

A. Basic Unit

Fig.1.shows the basic unit for proposed multilevel inverter. It consists of six unidirectional switches S_1, S_2, S_3, S_4, S_5, S_6 and two voltage sources V_1, V_2 with different magnitude. From Fig.1, it is clear that the switch combinations should not be turned 'ON' simultaneously as it will lead to a short circuit of voltage sources. The voltage across switch S_1, S_2 will be V_2 and the voltage across switch S_5, S_6 will be V_1 and the voltage across switch S_3, S_4 will be V_1+V_2. So that simultaneous turning 'ON' of switches in same leg should be avoided.

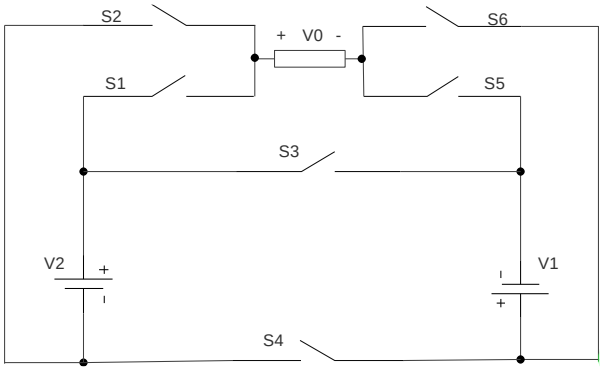

Fig.1. Circuit Diagram of 7 level basic units

To obtain different voltage levels in output waveform using structure shown in Fig.1, different switching combinations are given in Table I.

From the table, it is clear that 1 and 0 imply the conducting and non-conducting state of the switches respectively. To obtain more voltage levels in output waveform, the magnitudes of two voltage source be different otherwise in case of equal values of dc voltage sources, voltage levels decreases to three. To achieve all possible voltage levels both positive and negative, the values of dc voltage sources should be in the ratio 1:2.

TABLE I
Look up table for 7 Level Inverter

S1	S2	S3	S4	S5	S6	V_0
1	0	0	1	1	0	V_1+V_2
1	0	0	1	0	1	V_2
0	1	0	1	1	0	V_1
0	1	0	1	0	1	0
1	0	1	0	0	1	$-V_1$
0	1	1	0	1	0	$-V_2$
0	1	1	0	0	1	$-(V_1+V_2)$

B. Extended Level Circuit Configuration

To generate more level in output voltage, more switches and dc voltage source are connected with basic unit. Fig.2 shows the circuit diagram of extended level multilevel inverter by connecting switches and more dc voltage sources with basic unit. Along with one dc source, two switches are added for obtain higher levels.

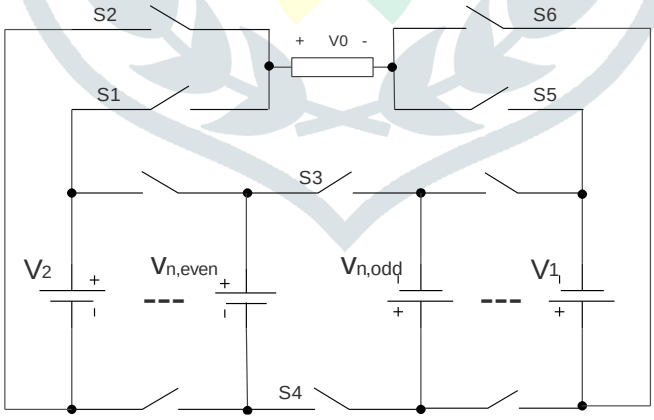

Fig.2. Circuit Diagram for extended level multilevel inverter

In the proposed general topology, the number of dc voltage sources (N_{source}), number of switches (N_{switch}), and maximum output voltage (V_0, max) and number of output voltage levels (N_{step}) are calculated as follows:

$N_{source} = n$ (1)

$N_{switch} = 2n + 2$ (2)

$V_{0,max} = V_n + V_{n-1}$ (3)

$N_{step} = 2^{n+1} - 1$ (4)

Where, n is the number of dc voltage source used in proposed circuit.

C. Magnitude of Dc Sources

Magnitude of dc voltage sources for general topology can be determined as follows:

$V_n = \{5^{(n+1/2)-1}V_{dc},$ *for odd n,* $n = 1, 3, 5,$ (5)

$= \{2 \times 5^{(n/2)-1} V_{dc}, \quad for\ even\ n, \quad n = 2, 4, 6, \qquad (6)$

III. CONTROL STRATEGY

The distortion factor and harmonic content is much reduced by adjusting the width of the pulses. The widths of the pulses are varied in accordance with the amplitude of a sine wave. The gate pulses are generated by comparing the reference signal with the carrier signal. The frequency of the reference signal is called as fundamental frequency and referred as f_r and the triangular wave of high frequency is selected as a carrier signal and is denoted as f_c .The inverter output frequency is decided by the fundamental frequency.

In frequency modulation index, the modulation index depends on the frequency of the reference signal and the carrier signal used. The frequency modulation index of the m_f of the multilevel inverter can be defined as

$$m_f = \frac{f_c}{f_r} \qquad (7)$$

where,

f_c - frequency of carrier signal

f_r - frequency of reference signal

In amplitude modulation index, modulation index depends on the amplitude of carrier signal and the reference signal used. In general the value of modulation index varies between 0 and 1. Amplitude modulation index (m_a) can be defined as

$$m_a = \frac{A_r}{(n-1)A_c} \qquad (8)$$

where,

A_r -Amplitude of reference signal

A_c -Amplitude of carrier signal

The peak amplitude of the reference signal, controls the modulation index M, and rms output voltage V_0.The number of pulses per half cycle depends on carrier frequency.

IV. SIMULATION AND RESULTS

Performance analysis of different levels of asymmetric CHB MLI is realized in MATLAB software. Simulation of 7 levels and 15 levels is modelled in the software. A comparative analysis has been done between these different levels on the basis of their THD levels and as the number of levels is increased harmonic content should also get reduced and more the sinusoidal waveform is achieved. Here switches are operated using fundamental frequency control technique. Switches are operated in such a manner that output voltage with 50Hz frequency is obtained.

a. 7 Level Asymmetrical Multilevel Inverter

The reference and gate pulse pattern for seven level asymmetrical cascaded multilevel inverter is shown in fig.3.(a)-(g).

Fig.3.(a) Reference Signal

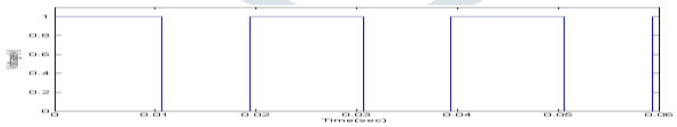

Fig.3.(b) Gate Pulse S_1

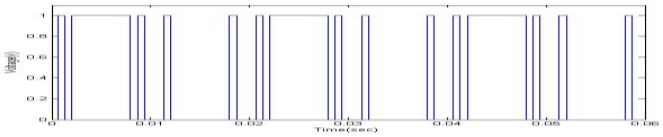

Fig.3.(c) Gate Pulse S_2

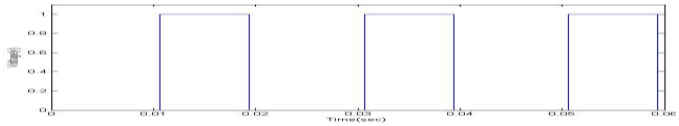

Fig.3.(d) Gate Pulse S_3

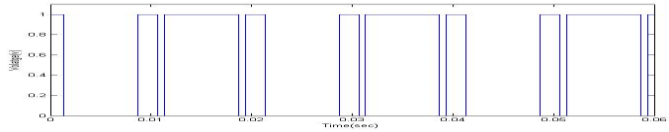

Fig.3.(e) Gate Pulse S_4

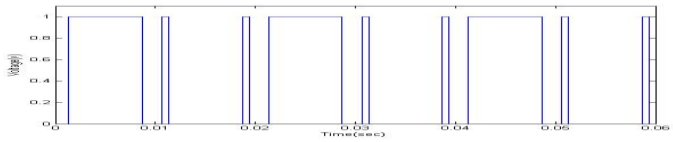

Fig.3.(f) Gate Pulse S_5

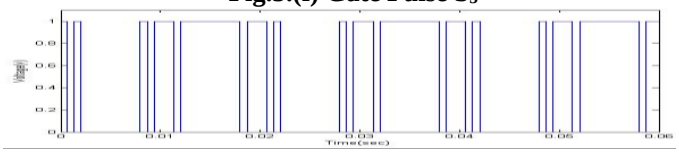

Fig.3.(g) Gate Pulse S_6

The magnitude of dc voltage for proposed 7 level inverter can be determined as follows.

$$V_1 = V_{dc} \quad (9)$$
$$V_2 = 2V_{dc} \quad (10)$$

The DC voltage sources magnitudes for V_1, V_2, are 75 and 150V and assuming V_{dc}= 75V. The output phase voltage waveform is shown in Fig. 4 respectively.

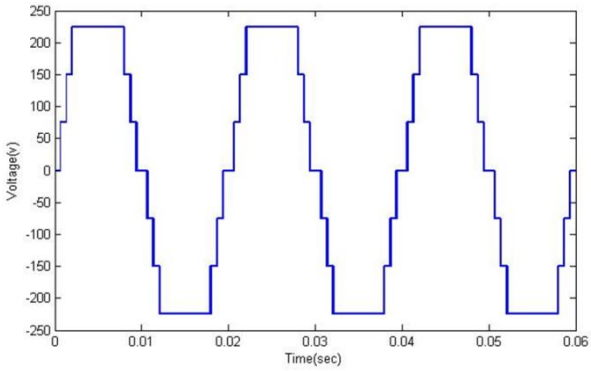

Fig. 4. Output voltage of 7 level inverter

b. 15 Level Asymmetrical Multilevel Inverter

The circuit diagram of 15 level inverter is shown in fig.5.Eight switches and three voltage sources are used in the H-bridge of the inverter. Each H-bridge consists of four switches. Inverter leg 1 has positive switch S1 and S2 and another leg of this circuit consists of switches S5 and S6 and another leg of this circuit consists of switches S3 and S4 another leg of this circuit consists of switches S7 and S8. It can be seen from Fig.5, that the switch combinations, should not be turned 'ON' simultaneously as it will lead to a short circuit of voltage sources. Similarly, simultaneous turn 'ON' of should be avoided. 1 and 0 imply the conducting and non-conducting state of the switches respectively. So, 15 levels of output voltages are achieved in the form of staircase.

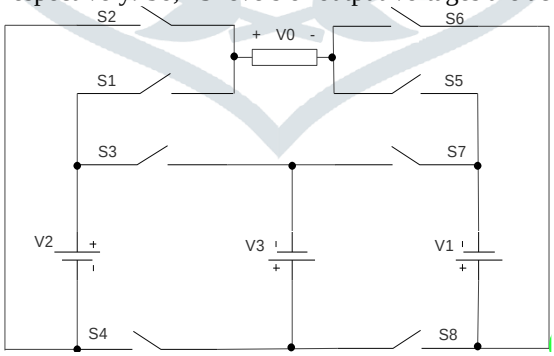

Fig. 5. Circuit diagram of 15 level inverter

The magnitude of dc voltage for proposed 15 level topology can be determined as follows.

$$V_1 = V_{dc} \quad (11)$$
$$V_2 = 2V_{dc} \quad (12)$$
$$V_3 = 5V_{dc} \quad (13)$$

The magnitude of dc voltage sources are V_1, V_2, and V_3 are 30V, 60V and 150V respectively and assuming V_{dc}=30V.

TABLE II
SWITCHING TABLE FOR 15 LEVEL INVERTER

No	S_1	S2	S_3	S_4	S_5	S_6	S_7	S_8	V_0
1	1	0	0	1	1	0	1	0	V_3+V_2
2	1	0	0	1	0	1	1	0	$V_3+V_2-V_1$
3	0	1	0	1	1	0	1	0	V_3
4	0	1	0	1	0	1	1	0	$V_3- V_1$

5	1	0	0	1	1	0	0	1	V_1+V_2
6	1	0	0	1	0	1	0	1	V_2
7	0	1	0	1	1	0	0	1	V_1
8	0	1	0	1	0	1	0	1	0
	1	0	1	0	1	0	1	0	
9	1	0	1	0	0	1	1	0	$-V_1$
10	0	1	1	0	1	0	1	0	$-V_2$
11	0	1	1	0	0	1	1	0	$-(V_1+V_2)$
12	1	0	1	0	1	0	0	1	$-(V_3-V_1)$
13	1	0	1	0	0	1	0	1	$-(V_3)$
14	0	1	1	0	1	0	0	1	$-(V_3+V_2-V_1)$
15	0	1	1	0	0	1	0	1	$-(V_3+V_2)$

The gate pulse for 15 level asymmetrical cascaded multilevel inverter is shown in fig.6.(a)-(h) as follows,

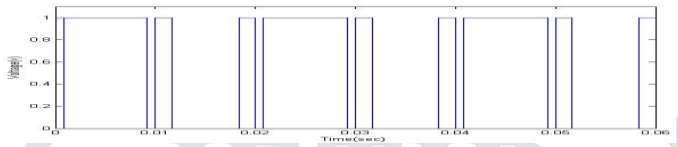

Fig.6.(a) Gate Pulse S_1

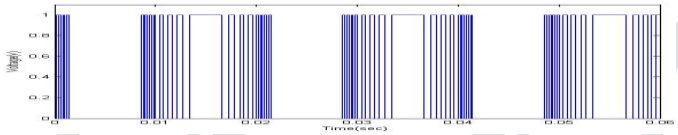

Fig.6.(b) Gate Pulse S_2

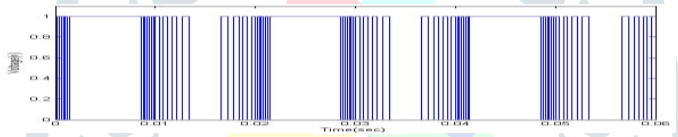

Fig.6.(c) Gate Pulse S_3

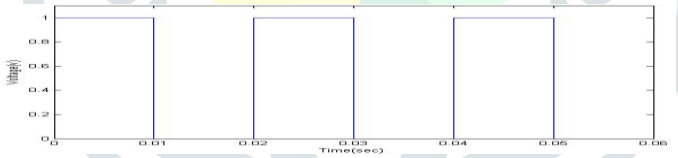

Fig.6.(d) Gate Pulse S_4

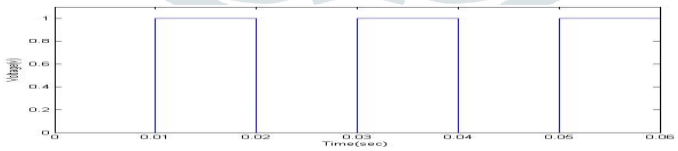

Fig.6.(e) Gate Pulse S_5

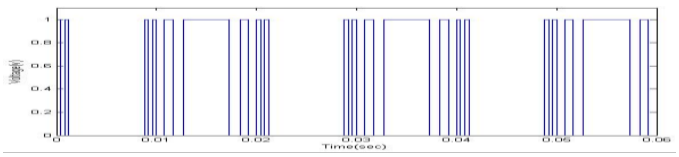

Fig.6.(f) Gate Pulse S_6

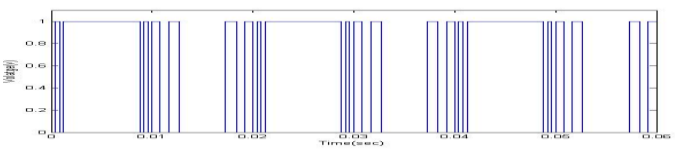

Fig.6.(g) Gate Pulse S_7

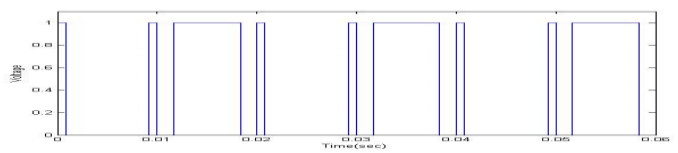

Fig.6.(h) Gate Pulse S_8

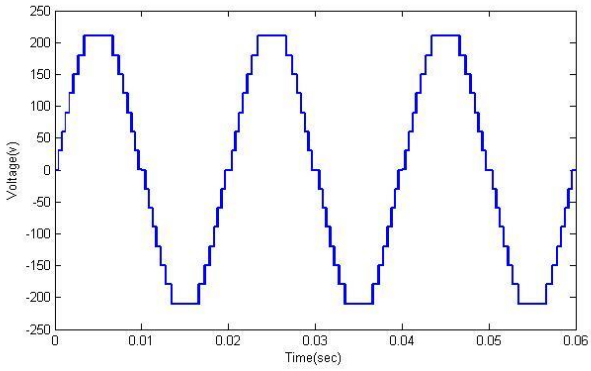

Fig. 7. Output voltage of 15 level inverter

Fig.7. shows the output waveform of extended 15 level inverter. The comparison of 7 level and 15 level inverter shown in Table III.

Table III. Comparison of DC Voltages and Levels

Levels	DC Voltage (V)		
	V_1	V_2	V_3
7	75	150	
15	30	60	150

Table IV compares the components required for normal cascaded H-Bridge and Proposed Multilevel inverter circuit.

Table IV. Comparison of Source and Switches

Levels	Cascaded H-Bridge Multilevel Inverter		Proposed Asymmetrical Multilevel Inverter	
	No. of. DC Sources	No. of. Switches	No. of. DC Sources	No. of. Switches
7	3	12	2	6
15	7	28	3	8

The cost is much reduced by reducing the no .of dc sources and switches. From the table, it is inferred that the proposed multilevel inverter is suitable high power applications.

Table V gives the total harmonic distortion present in the circuit for 7 level and 15 level inverter.

Table V. **Comparison between THD and levels**

Levels	THD (%)
7	15.55
15	6.68

V. CONCLUSION

The new asymmetrical multilevel inverter is designed and analyzed in MATLAB Software. The basic unit is simulated with two voltage sources and six switches in order to obtain the 7 level output voltage. The results shows that the efficiency of the system is increased more when compared to the conventional 7 level inverter circuit. The total harmonic distortion and circuit components required is also much reduced. The proposed circuit is easily extended for higher version with minimum components with a wide range of multiple source inputs. The DC voltage sources magnitudes for each level is selected through the methods of arrangement of dc sources. A subharmonic controlled PWM strategy is used for the generation of gate signals. The different structures are simulated for obtaining different levels in output voltage by connecting switches and dc voltage sources with basic unit. From the analysis of harmonic contents, it is observed that the increase in number of levels, leads to decrease the THD and thereby makes the waveform almost reaches the sinusoidal shape. The performance accuracy of proposed topology is verified with the help of simulation output waveform of 15 level inverter. After comparison it is concluded that fifteen level inverter is found to be effective in reducing the harmonics.

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