Design of High-speed 16 to 4 Priority Encoder Using GDI

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Abstract ---A priority encoder compresses 2^n multiple binary inputs into n number of outputs based on priority and it has been used in communication applications like, to control interrupt requests by acting on the highest priority request and encode the output of a parallel ADCs (Analog to Digital Converter), which persistently impose special design constraints in terms of high frequency and minimal area. In this paper proposed the GDI (Gate Diffusion Input) technique-based 16 to 4 priority Encoder. Which allow less propagation delay of combinational digital circuits and minimal area in terms of transistor count, compared these two parameters among CMOS and GDI Technologies. All the simulations are done in DSCH 3.8 Micro-Wind tool in 45nm technology.

Keywords: Priority encoder, GDI, CMOS.

I. INTRODUCTION

Circuit which performs a particular processing of an information operation that is specified logically by a group or set of boolean functions is termed as Combinational circuits. Based on the levels present at input pins, combinational circuit output will change at any instant of time.

The functionality of encoder is to convert into code from a set of input signals. The encoder has main role in electronic projects, and it is used in networking, communication systems like telecommunication etc., to transform data from one part to other. It is reverse to the decoding. But the problem with the encoder is if more than one input is high at a time then it gives error and generates the unknown output. Priority encoder overcomes this problem. It can accept all possible combinations of inputs and produces correct output.

Priority encoder output is the binary form of the original number starting from 0 of Most Significant Bit, MSB, input, which act on the highest priority [1] encoder interrupt input to control the interrupt requests. Based on the logical expression $M=\log_2^N$, the priority encoder produces an output by taking N inputs, where N is normally 4, 8 or 16. Whereas data M is usually binary code of 2, 3 or 4. "M" indicates the forced input.

Generally combinational circuits design using CMOS Technology. This paper proposed the GDI technology-based priority encoder, which has more efficient than the CMOS based priority encoder in terms of transistor count and delay. This paper is organised into seven sections with differentiating CMOS with GDI, then design of PE along schematic capture, simulations, extraction of parameters and explanation of results.

II. CMOS

CMOS is technically defined as of **"Complementary Metal Oxide Semiconductor"** [2] as low power technology. The CMOS Technology utilizes both NMOS and PMOS [4-5] to design different logic functions. The CMOS is designed so that Both the N-channel MOSFET and the P-channel MOSFET characteristics are match (during ON and OFF state).

CMOS technology has one important characteristic which allows the design of logic devices using only simple switches, without the need for a pull-up resistor, because one signal can turn OFF one transistor and turn ON other at at time. In present days, the nMOS and bipolar process for almost all digital logic applications are dominated by CMOS design. nMOS is conducts Low or 0 when input is High or 1, but weak in conducting High or 1. pMOS conducts High or 1 when input is Low or 0, but weak in conducting Low or 0. Hence, nMOS is used for pull-down network, whereas pMOS is used for pull-up network.

III. GDI

GDI is **"Gate Diffusion Input"** [3]. The main advantage of this method is, logic design can be easily done with curtailing of power consumption, propagation delay and area. This method uses a simple cell which has one nMOS and one pMOS like a CMOS inverter. But there are differences, in CMOS Only Gate acts as input but in GDI, source and drain terminals also act as inputs as shown in below Fig1 [6].

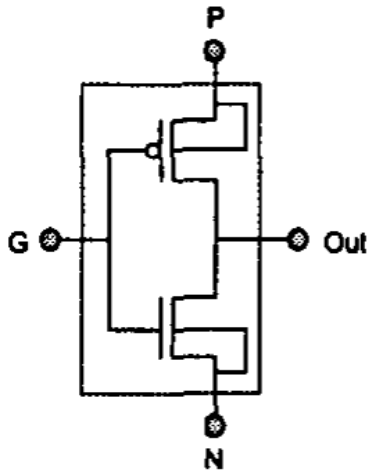


Fig1. Basic GDI Cell

To design logic gates like OR, AND, MUX with CMOS technology need more than two transistors. But for GDI technology two transistors are enough. The below table1 [6] shows the various functions of GDI cell based on the different inputs to the three terminals.

N	P	G	Out	Function
'0'	B	A	$\acute{A}B$	F1
B	'1'	A	$\acute{A}+B$	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\acute{A}B+AC$	MUX
'0'	'1'	A	$\acute{A}$	NOT

Table1 Functionality of GDI cell

IV. PRIORITY ENCODER

A circuit that produces a smaller number of outputs by compressing the binary inputs with highest priority. There are four inputs and two outputs with one control output. Priority of A1 defined by when Y3 or Y2 are high, also A0 controlled by Y3. The circuit diagram of 4 to 2 priority encoder is as shown in below fig2 [7].

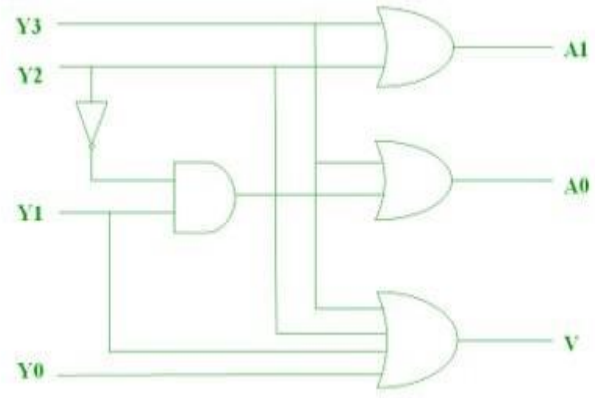


Fig 2. 4 to 2 Priority Encoder

Truth table is an essential element of any design gives the output for a combination of input. One can show all input combinations or simply donot care the status of the input by x. A 4 to 2 PE is as shown in below table2 [7].

INPUTS				OUTPUTS		
Y3	Y2	Y1	Y0	A1	A0	V
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

Table 2. 4 to 2 Priority Encoder truth table

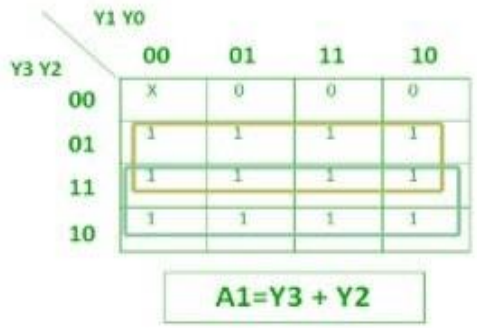
Minterms are

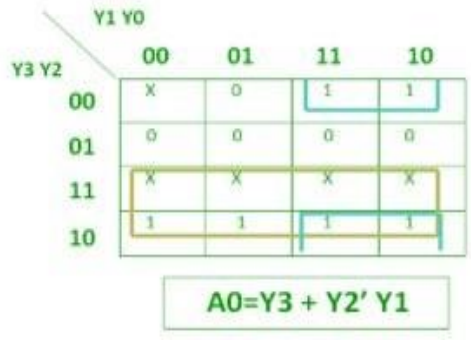
$A1 = \sum m\,(1, 2, 3, 5, 6, 7, 9, 10, 11, 13, 14, 15)$

$A0 = \sum m\,(1, 3, 4, 5, 7, 9, 11, 12, 13, 15)$

Next step is to get the logic equations for each output using Sum of Products with true logic. From the truth table obtained the Minterms. Using Karnaugh map(K-map) minimization technique, minimized the equations and implemented the 4 to 2 priority Encoder.

This is shown in K-map in fig





V. CMOS PRIORITY ENCODER

Designed the 16 to 4 Priority Encoder by writing the truth table and from that truth table derived the output equations, based on that equations design of 16 to 4 Priority Encoder is done**. A sixteen inputs would give a uncontrollable truth table So minimize the the table to comprehend the output combination inputs control each output.**
The Obtained equations are minimized using Boolean minimization techniques. Final minimized equations are

$Y0 = \sum (\bar{D}_{14}\,\bar{D}_{12}\,\bar{D}_{10}\,\bar{D}_8(\bar{D}_6\,\bar{D}_4\,\bar{D}_2\,D_1 + \bar{D}_6\,\bar{D}_4\,D_3 + \bar{D}_6\,D_5 + D_7) + \bar{D}_{14}\,\bar{D}_{12}\,(\bar{D}_{10}\,D_9 + D_{11}) + \bar{D}_{14}\,D_{13} + D_{15})$

$Y1 = \sum (\bar{D}_{13}\,\bar{D}_{12}\,\bar{D}_9\,\bar{D}_8(\bar{D}_5\,\bar{D}_4\,D_2 + \bar{D}_5\,\bar{D}_4\,D_3 + D_6 + D_7) + \bar{D}_{13}\,\bar{D}_{12}\,(D_{10} + D_{11}) + D_{14} + D_{15})$

$Y2 = \sum(\bar{D}_{11}\bar{D}_{10}\bar{D}_9\bar{D}_8(D_4+D_5+D_6+D_7) + D_{12}+D_{13}+D_{14}+D_{15})$

$Y3 = \sum (D_8 + D_9 + D_{10} + D_{11} + D_{12} + D_{13} + D_{14} + D_{15})$

Based on the above equations there is a need of 3,4 and 5 inputs of CMOS based AND and OR gates. First developed these basic gates and using them designed priority encoder.

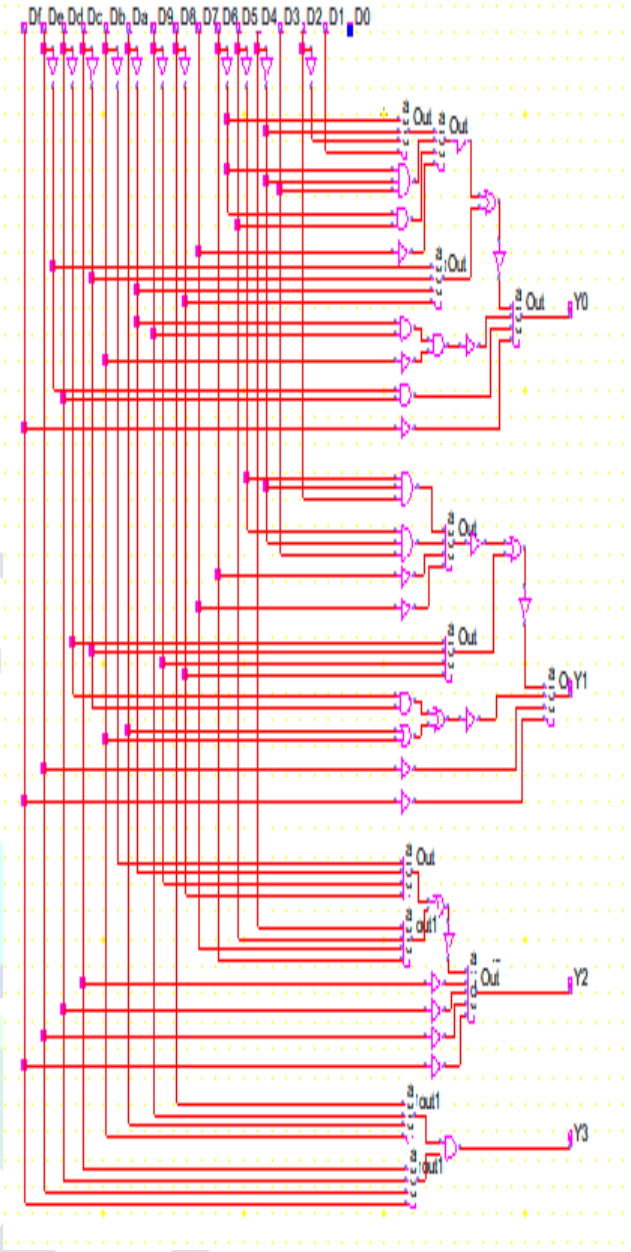


Fig3. CMOS based 16 to 4 Priority Encoder

After implemented design, Simulation is done in DSCH 3.8 Micro-Wind tool. Generated the waveform as shown in Fig4.

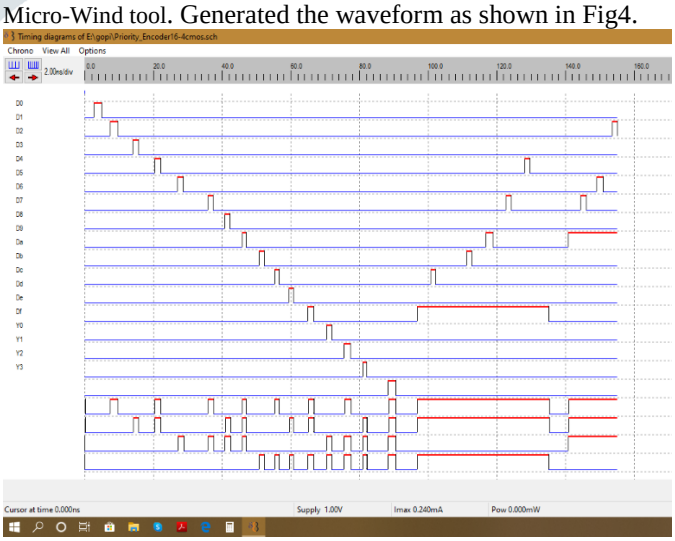


Fig4. CMOS 16 to 4 Priority Encoder Waveform

VI. GDI PRIORITY ENCODER

Implemented 16 to 4 GDI which were based on priority encoder using the same equations used to design CMOS 16 to 4. Before the development of 16 to 4 PE, designed 3,4 and 5 inputs AND and OR gates using GDI. By using the same gates Implemented 16 to 4 priority encoder.

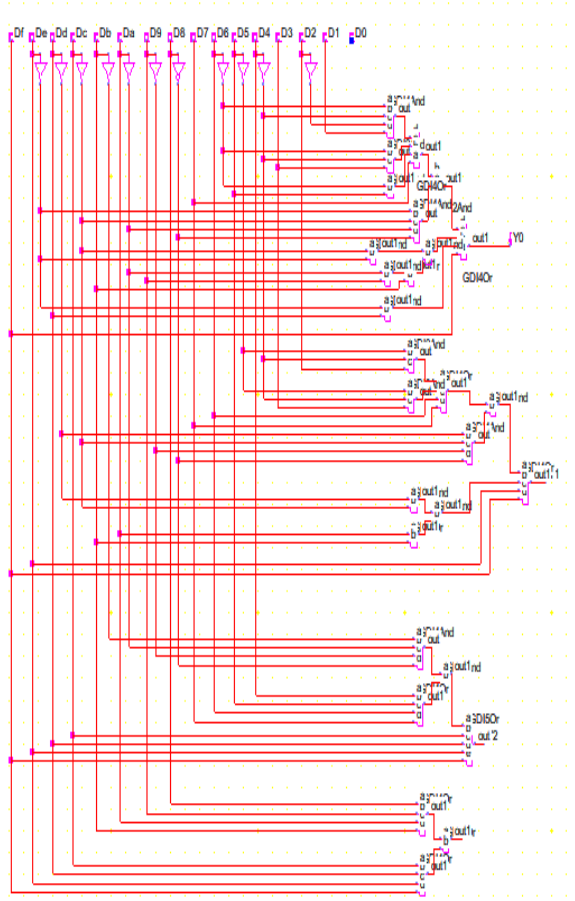


Fig5. GDI based 16 to 4 Priority Encoder

After completing design, simulation is done in DSCH 3.8 Micro-Wind tool. Obtained waveform as shown in Fig6.

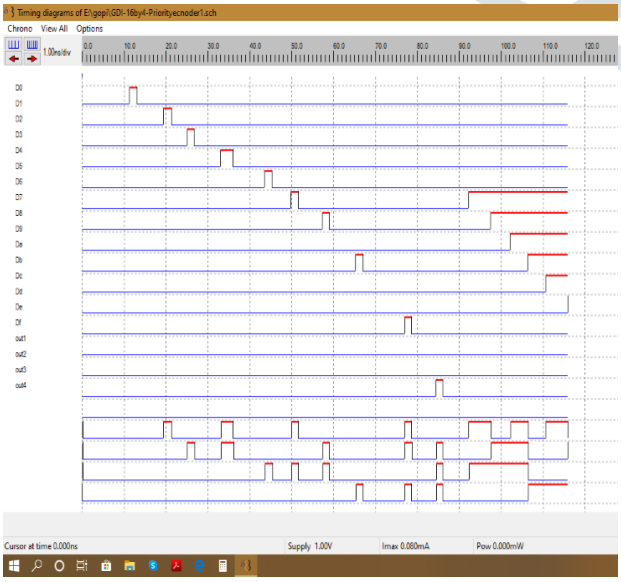


Fig6. GDI 16 to 4 Priority Encoder Waveform

VII. RESULTS AND COMPARATIVE ANALYSIS

Generated properties for both CMOS and GDI compared those properties.

Technology	No. Of symbols	No. Of Lines
CMOS	75	236
GDI	59	226

Table3. Property Analysis

From the table, we can observe that No of gates required to design the GDI based 16 to 4 priority Encoder is less than the gates required to design CMOS based 16 to 4 priority Encoder. So, GDI technology is less complexity than CMOS technology.

The delay calculated for the CMOS based 16 to 4 priority Encoder and GDI based 16 to 4 priority Encoder in the DSCH 3.8 Micro wind tool.

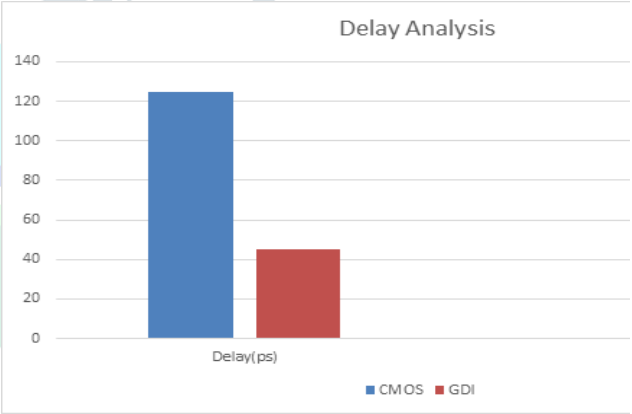


Fig7. Delay Analysis Chart

From the above Fig7, GDI based Priority encoder is faster than CMOS based priority encoder.

VIII. CONCLUSION

The Priority Encoder is one of the crucial components in many applications so if it is efficient in terms of its design metrics then it will help in improving efficiency of entire design. So, in this project concentrated on design metrics of Priority Encoder. The GDI technology gives better results than CMOS. The GDI based 16 to 4 priority Encoder has 66% less delay than the CMOS based 16 to 4 priority Encoder and it has less complexity.

IX. REFERENCES

[1] Design and Analysis of Priority Encoder with Low Power MTCMOS Technique, IEEE 2018.

[2] k. Roy and S. Prasad, "Low-Power CMOS VLSI circuit design": Wiley Interscience Publication, 2000.

[3] Munesh Tripathi and Gajendra Sujediya, "Low Power based Manchester Encoder by GDI", IEEE 2018.

[4] J.G Dekgado-Frias and J. Nyathe, "High-performance Encoders with priority look ahead", IEEE Trans. Circuits Sysl, Fundam. Theory Appl. Vol. 53, pp- 1390 to 1393, September 2000.

[5] S. A. hafeez and S. Harb, "A VLSI high performance priority Encoder using standard CMOS library," IEEE transactions on Circuits and System II, Vol. 53, pp- 597 to 601, No.8, August 2006.

[6] Gate-Diffusion Input (GDI) - A novel power efficient method for digital circuits: a design methodology

[7] An Efficient Design of 4 - to - 2 Encoder and Priority Encoder Based on 3-dot QCA Architecture.