Analysis of Process Supply Voltage and Temperature Compensated Supply Circuit for an Inverter

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Abstract: In this paper, an inverter uses as a load for a for a process, supply voltage and temperature (PVT) compensated supply circuit. A PVT circuit provides a constant voltage while the input supply (Vcc) and temperature of the circuit varies. As we know that a digital circuit very common to use but its output effected by the supply and environmental changes. By the PVT circuit we can reduce the supply variation and temperature variation problem. In the PVT circuit a current mirror circuit are used for providing a constant current to every branch. A current mirror circuit with the p/n diode we obtain a complementary to absolute temperature (CTAT) and process to absolute temperature (PTAT). The CTAT and PTAT voltage adjustment through a resistance we obtain a constant voltage. The validation of result is done using a 0.18µm CMOS technology in a CADENCE Virtuoso tool and find a power consumption through an inverter which as a load.

Index Terms **- PVT, CMOS, CADENCE Virtuoso, Static Power, Dynamic Power, MOSFET, Thermal Voltage.**

I. INTRODUCTION

In the current scenario Digital Circuit is more common to use because it is easy to carry and provides lot of feasibility in day to day regular life but digital circuit faces two major problems that is define as environmental effect and supply variation of the circuit that is degrade the circuit performance. To reduce that problem some of the researcher gives the concept of body bias of the MOSFET but due to body bias a leakage current come on the picture and provide high power dissipation [1].

Fig. 1 represent as the conventional process, supply voltage and temperature compensated supply circuit which is combination of a CMOS op-amp, resistor and diode that are essential in PVT circuit [2]-[5]. The PVT circuit are also design with the help of bipolar transistor but they are not useful for semiconductor memories circuit. Three basic differences between BJT and MOSFET is the subthreshold current is small due to the large drain to source resistance R_{DS} in the subthreshold operation [6], MOSFET have an intrinsic matching problem and the drain current I_D does not have the same temperature coefficient as to BJT. In the conventional circuit three major part are necessary first power supply rejection ratio second temperature coefficient third line sensitivity [7]. The basic drain current equation is

$$I_D = \beta(V_{GS} - V_{TH})^{\alpha} \quad (1)$$

$$I_D = I_S \cdot (e^{V_D/V_T} - 1)$$

$$\cong I_S \cdot e^{V_D/V_T} \quad (2)$$

Where β is defined as $0.5\mu(T)C_{OX}(W/L)$, µ(T) is the mobility of the electrons or holes in which T is the operating temperature, C_{OX} is the gate-oxide capacitance. From the figure (1) V_{REF} provide small voltage as input supply increases so that load of the circuit does not work properly.

$$V_D = V_T \cdot \ln(I_D/I_S)$$

$$V_D \propto V_T \quad (3)$$

$$V_D \propto 1/I_S \quad (4)$$

From the equation 3 and 4 the diode voltage directly related to thermal voltage and inversely related to saturation current. Saturation current highly affected with temperature as compare to thermal voltage so that this type of decrement gives a Complementary to absolute temperature and difference of two diode voltage provides Process to absolute temperature.

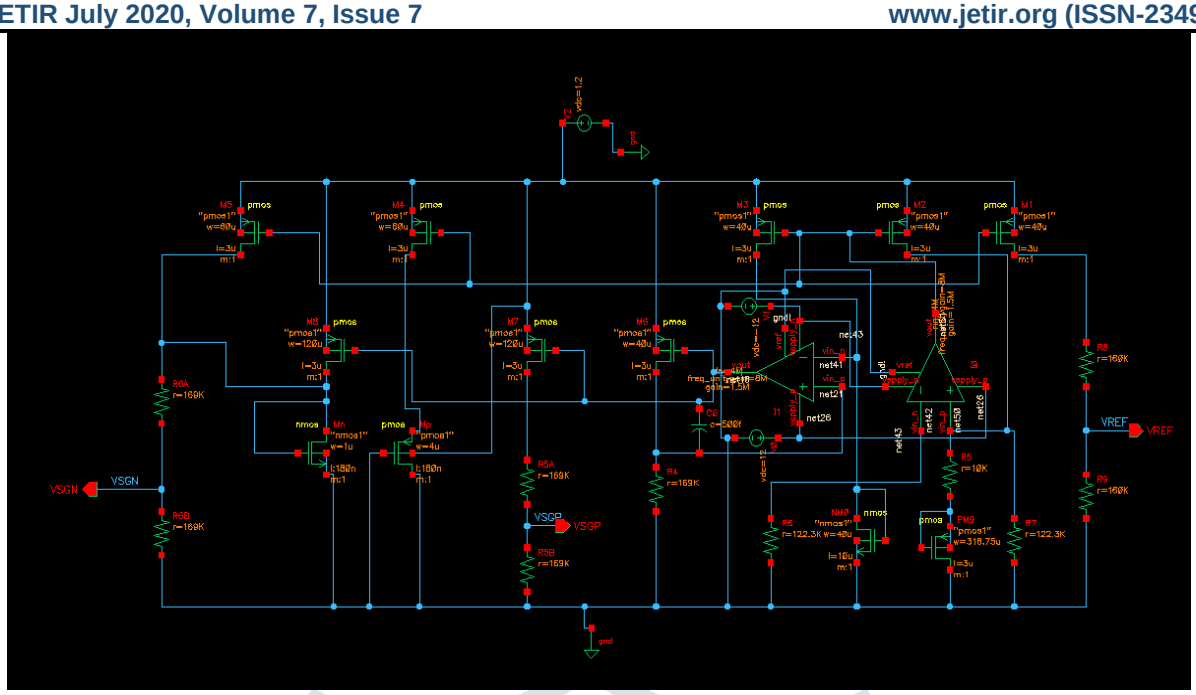


Figure 1: Reference PVT circuit

In the figure (1) we also use diode that may be p/n type the basic diode current equation

$$I_D = I_S \cdot (e^{V_D/V_T} - 1) \quad (5)$$

Where I_D is diode current and I_S are saturation current, V_D and V_T represent as diode voltage and threshold voltage respectively [8]-[10]. In the reference PVT circuit op-amp circuit used which has two inputs V_a and V_b, are controlled to be the same voltage. By the conventional PVT circuit we can cover the temperature range from -27^0C to 125^0C and this circuit design with the 0.4µm CMOS technology which are too much large from propose PVT circuit [11]-[12]. The final equation from the reference circuit is

$$V_{REF} = V_{f1} + R2/R3\ dV_f = V_{REF_conv} \quad (6)$$

Where V_{f1} is the built in voltage of the diode and it have negative temperature coefficient of $-2mV/^0C$, whereas thermal voltage V_T has a positive temperature coefficient of $0.086\ mV/^0C$ where dV_f is proportional to the thermal voltage V_T [7]-[10]. The delay equation of MOSFET is the combination of t_{pHL} and t_{pLH} is define below

$$t_d \approx \frac{C_L V_{DD}}{2\beta(V_{DD} - V_{TH})^{\alpha}} \quad (7)$$

this equation maintains the delay of an inverter which behave as load of the circuit, t_{pLH} and t_{pHL} represent as following $t_{pHL} + t_{pLH}$

$$= \frac{C_L V_{DD}}{2\beta(V_{DD} - V_{THN})^{\alpha N}} + \frac{C_L V_{DD}}{2\beta(V_{DD} - V_{THP})^{\alpha P}} \quad (8)$$

Where $V_{DD,}$ and V_{THN} and V_{THP} are the supply voltage and threshold voltages for nMOS and pMOS respectively.

2. Proposed PVT Circuit

The proposed circuit obtain by the using of complementary to absolute temperature (CTAT) and process to absolute temperature (PTAT). A CTAT voltage form when a constant current pass through the diode by this the diode voltage vary with respect to temperature. Similarly process to absolute temperature formed by the help of subtraction of two CTAT voltage. From the adjustment of resistance and supply voltage we form a reference voltage that will provide better supply to a load. In this paper we use an inverter as load that will not affected by supply and temperature variation and it also provide less power dissipation on the output side.

PM0,PM1,PM2	**20µ/2µ**	**NM0, NM1**	**20µ/2µ**	**R0**	**3.5KΩ**
R1	**100KΩ**	**Vdc**	**x**	**p/n**	**m:1**

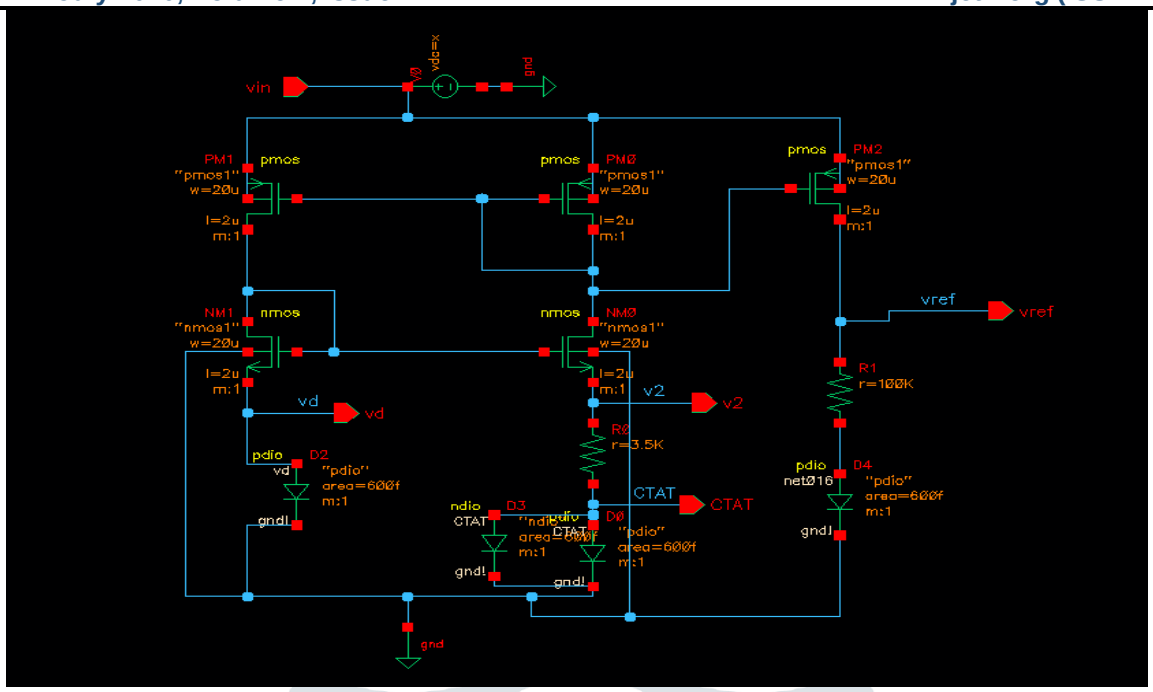


Figure 2: Proposed PVT Circuit for constant voltage (V_{REF})

2.1 CTAT

Complementary to Absolute Temperature is simply a diode voltage a temperature increases diode voltage decreases. A CTAT voltage form when a constant current pass through a diode in figure (2) PM0, PM1, PM2 work as current mirror and diode have p type for low threshold voltage V_{TH}. Representation of CTAT in figure (3) where a 5µA current pass through a diode and diode voltage decrease with increase in temperature /^{0}C.

we can define as V_T and I_S both are varying with temperature variation where

$$V_T=KT/q \quad \text{and} \quad I_S=BT^{4+m}\exp(-Eg/KT) \tag{9}$$

So that

$$dV_T/dT = K/q \tag{10}$$

$$dI_S/dT = I_S[(Eg/KT^2) +(4+m/T)] \tag{11}$$

From the equation (7) represent as positive temperature coefficient and equation (8) represent as negative temperature coefficient which have high negative value with increase in /^{0}C.

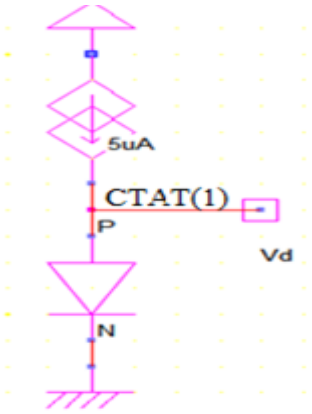


Figure 3.1(a): CTAT voltages circuit (V_D)

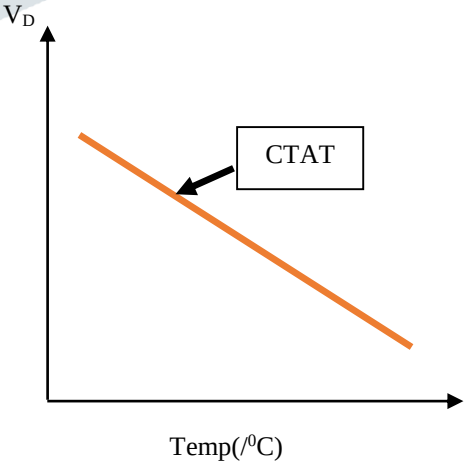


Figure 3.1(b): A general CTAT voltages waveform(**millivolt**)

2.2 PTAT

Process to Absolute Temperature is simply a difference of two diode voltages because we require a relation of V_D with respect to V_T only. Difference of two CTAT voltage define as PTAT voltage. From the figure 4.1(a) represent as PTAT voltage.

$$V_{D1} =V_T \ln (I_D/nI_S) \tag{12}$$

$$V_D - V_{D1} = V_T \ln(I_D/I_S) - V_T \ln(I_D/nI_S) \quad (13)$$

$$V_D - V_{D1} = V_T \ln(n) \quad (14)$$

Representation of V_D and V_{D1} voltage with circuit diagram.

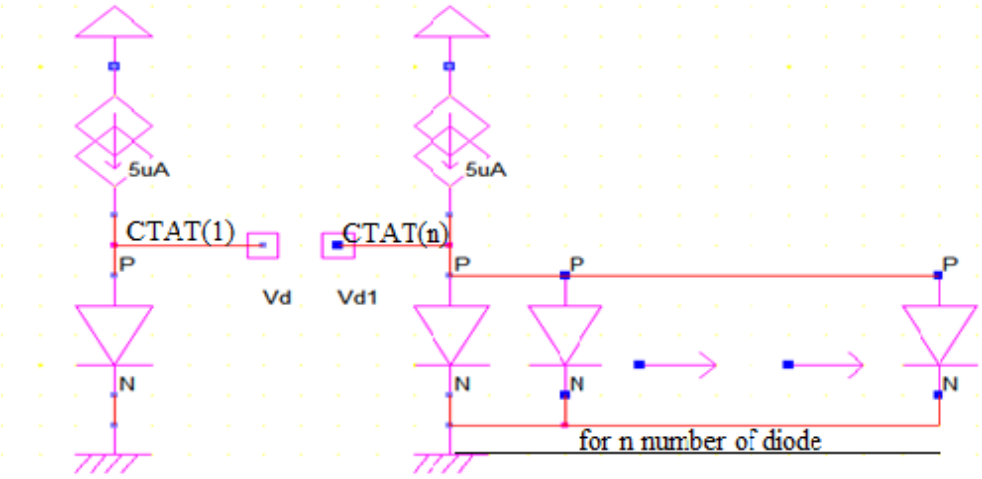


Figure 4.1(a): PTAT voltages circuit(volt)

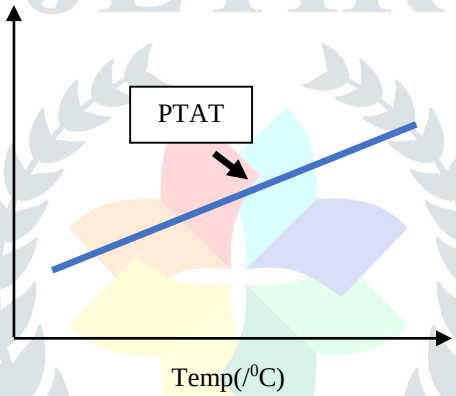


Figure 4.1(b): A general PTAT voltage waveform (microvolt)

For a reference voltage V_{REF} we add CTAT and PTAT voltage with some adjustment that shows in figure (5) where K1 and K2 are variable.

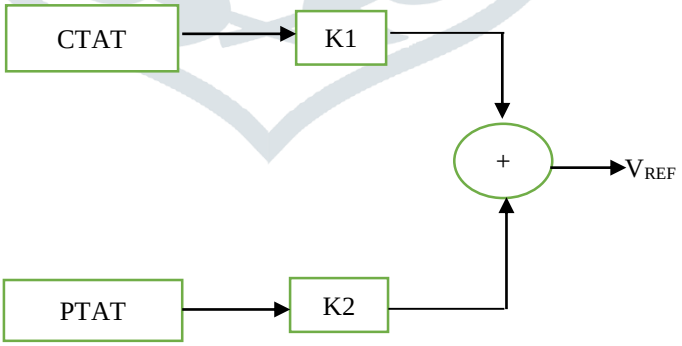


Figure 5(a): Combination of CTAT and PTAT voltage

$$K1\,(CTAT) + K2\,(PTAT) = V_{REF} \quad (15)$$

From the figure 5(a) we adjust the CTAT and PTAT voltage with K1 and K2 where K1 and K2 are variable

$$K1\,(85\mu V) = K2\,(1.6mV) \quad (16)$$

by the solution K1=18.82 and K2=1 with this help to obtain resistance value and K1 = R2/R1 ln(n) in the propose circuit n=2 are taken as diode numbers and R0 and R1 value is 3.5KΩ and 100KΩ respectively.

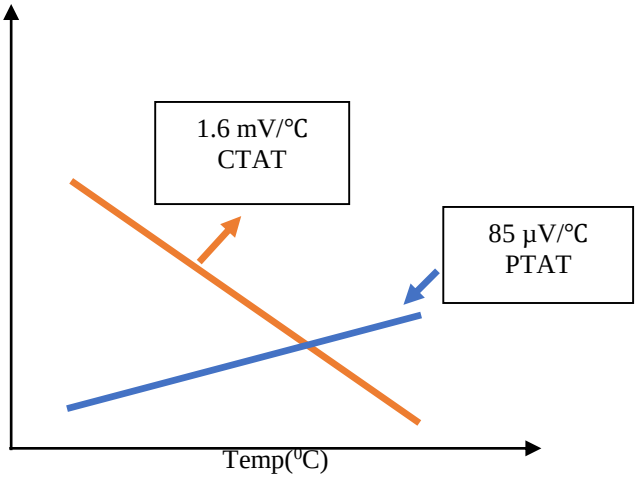


Figure 5(b): Combination of CTAT and PTAT voltage

3. SIMULATION AND RESULTS:

The propose circuit are validate using Cadence Virtuoso tool with gpdk 0.18µm technology. The analysis is taken in the two form first on the basis of reference voltage with the variation of input sully and temperature second analysis are taken with the load of inverter. In the figure (7) waveform of the propose PVT circuit are represent with the variation of input supply. In this waveform input supply vary from 1.6volt to 5volt and reference voltage V_{REF} provide an approximate constant voltage range from 1volt to 1.8volt. In the figure (8) waveform of propose PVT circuit shown with the variation of temperature. In the propose circuit temperature vary from -50^{0}C to 125^{0}C for that reference voltage V_{REF} provide approximate voltage from 1.5 volt to 1.6 volt. The figure (9) shows the waveform of inverter with the static power description. Inverter are design with .18µm technology and it shows static power dissipation on vary with input supply. Inverter pMOS and nMOS are define with proper W/L ratio so that it provides best output with full swing. But when we are using inverter with propose PVT circuit it provide less static power dissipation as compare to without propose PVT circuit use. In the figure (9) the output of propose PVT circuit V_{REF} work as input supply (V_{DC}) for an inverter so that this circuit also provide compensation on input supply variation and temperature effect. In the figure (9) propose PVT circuit define as a symbol that symbol cover all the transistor of the propose PVT circuit. Figure (10) represent static power dissipation using the Propose PVT circuit. Some of the chart also present in the following section which explain the comparison between the Reference Circuit and Propose PVT Circuit.

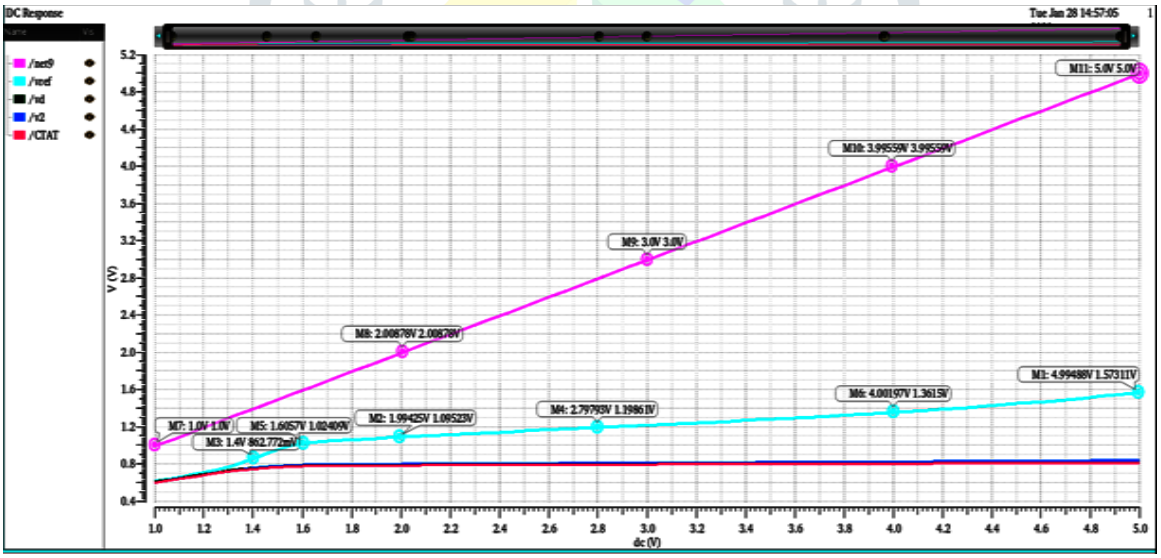


Figure 6: Waveform of Propose PVT circuit with variation of input supply (dc volt)

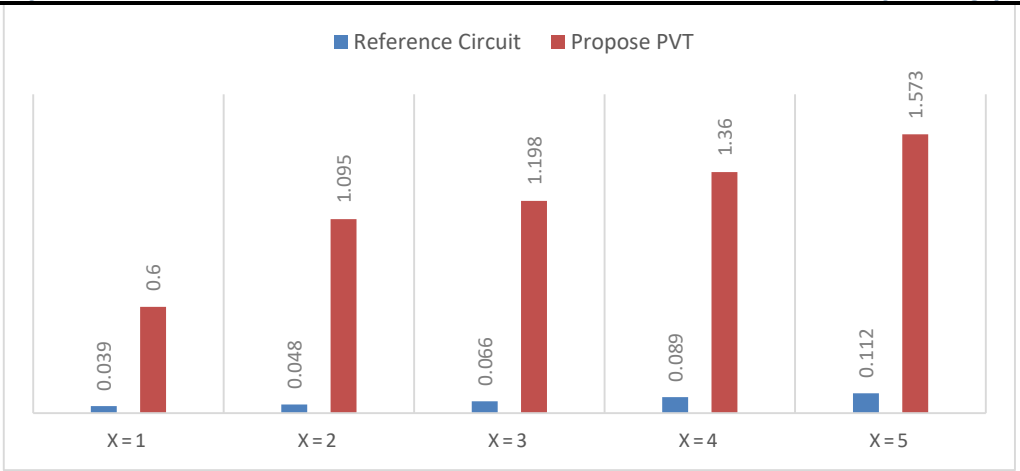


Chart 1: Comparison of V_{REF} w.r.t. Supply variation (Vcc)

In the chart (1) comparison of reference circuit voltage and Propose PVT circuit reference voltage represent. When dc (Vcc) voltage is 1-volt Reference circuit provide only 0.039volt where Propose PVT reference circuit provide 0.6volt that can beneficiary for the load of the circuit response. As we can see when dc volt reach at 5-volt the Reference circuit provide only 0.112 volt where Propose PVT circuit provide 1.573 volt which can sufficient for Digital load circuit. Propose PVT circuit provide better reference output in volts and it also follow the reference circuit concept as supply increases the reference voltage provide approximate constant voltage.

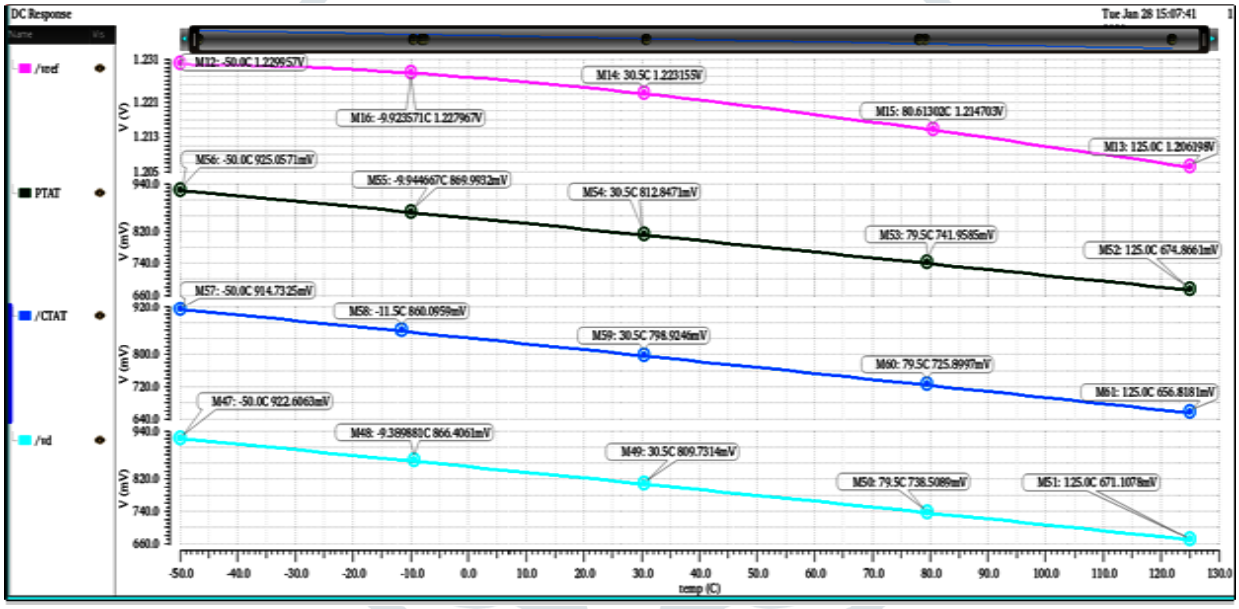


Figure 7: Waveform of Propose PVT circuit with variation of Temperature (-50 to 125^{0}C)

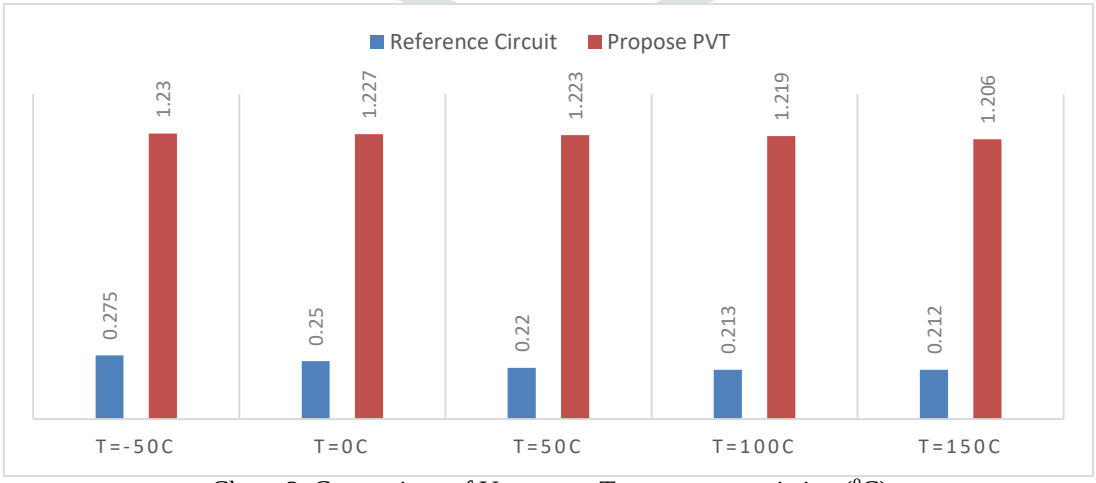


Chart -2: Comparison of V_{REF} w.r.t. Temperature variation (^{0}C)

In the chart (2) comparison of reference circuit voltage and Propose PVT circuit reference voltage represent. When temperature increases the reference voltage provide approximate constant voltage. In this chart as temperature is -50^{0}C the Reference circuit provide 0.275volt where Propose PVT circuit provide 1.23volt. In this chart we can say that both Reference and Propose PVT circuit provide a constant voltage as temperature increases. But at the load point of we require minimum .8volt or high so that a digital circuit work properly. Propose PVT circuit provide a better output in terms of reference voltage for the digital load of the circuit and less vary with temperature variation.

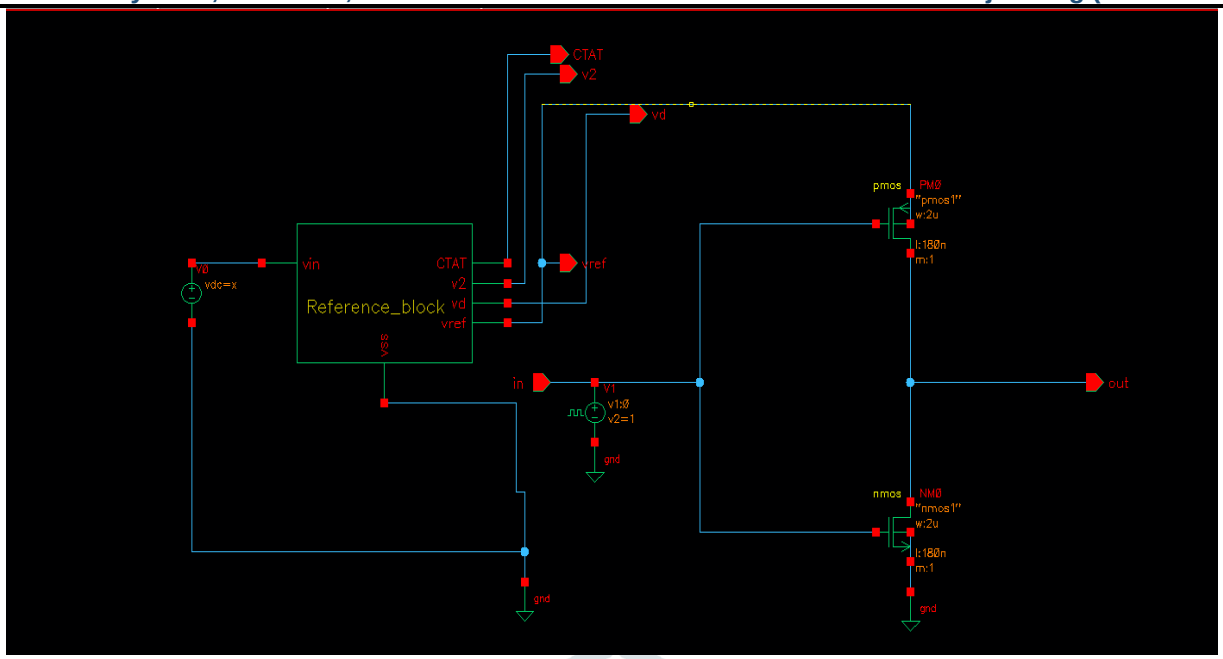


Figure 8: Propose PVT circuit with Load (Inverter)

In figure(8) reference block behave as PVT compensated circuit that provide a refence voltage that will offer a input dc supply to an inverter. By this configuration inverter input dc supply does not affected with supply and temperature variation. As input dc supply constant and minimum that will also reduce the power dessipation of the load circuit that shown in figure (9).

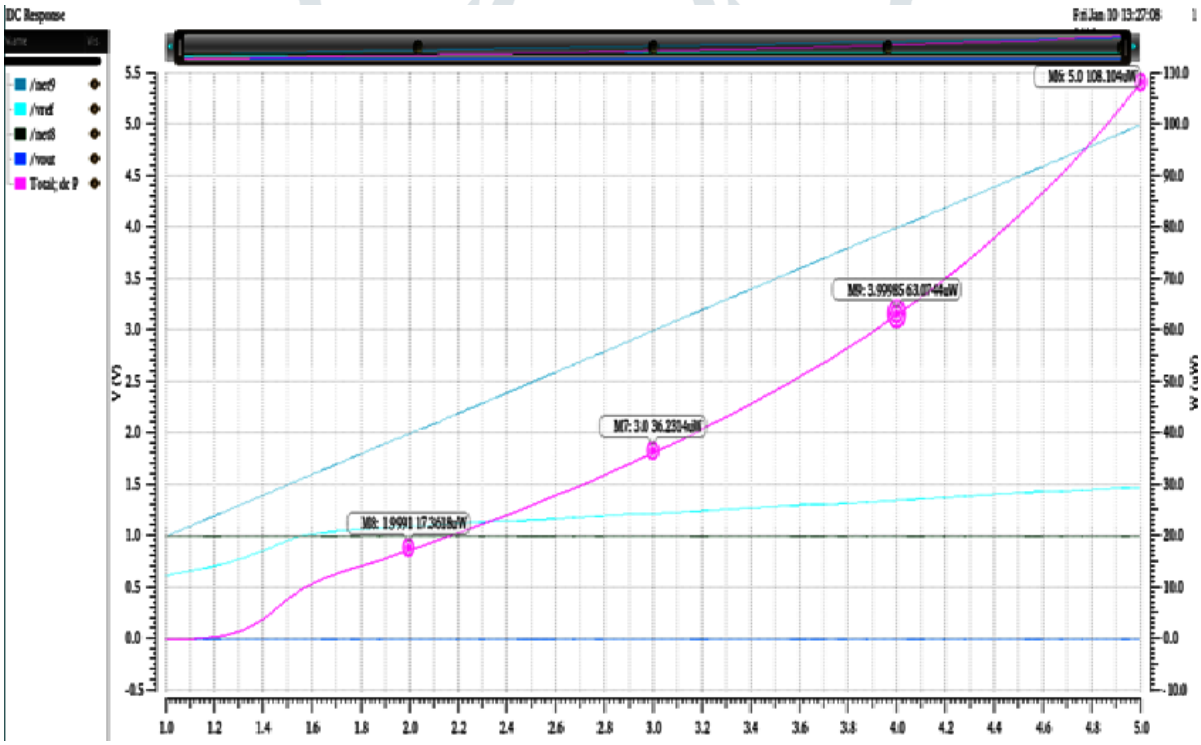


Figure 9: Waveform of Inverter for Static Power (µW)

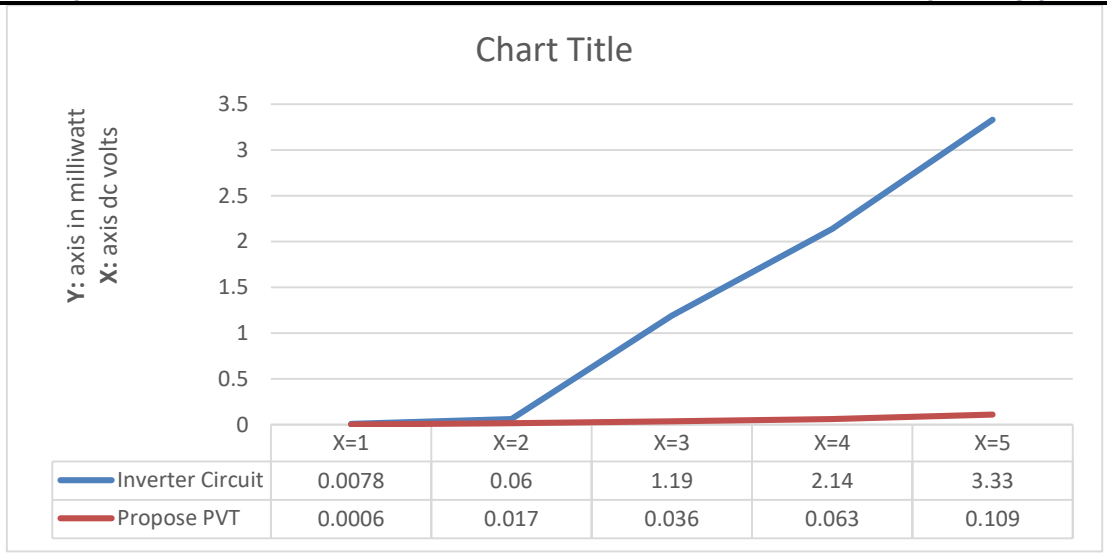


Chart -3: Static Power dissipation comparison (milliwatt)

In chart (3) static power dissipation through single Inverter Circuit and Propose PVT circuit are compare. As the dc volt (Vcc) vary the power dissipation across inverter circuit increases and this inverter are design using 0.18µm CMOS technology. But when we are using Propose PVT circuit the static power dissipation are present in very less amount as compare to a single Inverter Circuit. When input supply (Vcc) is 1-V the Inverter Circuit provide 7.8µW where Propose PVT circuit provide only 0.6µW. When a input supply provide is 5-volt the Inverter Circuit have a power dissipation across inverter is 3.33mW where Propose PVT circuit have only 0.109mW.

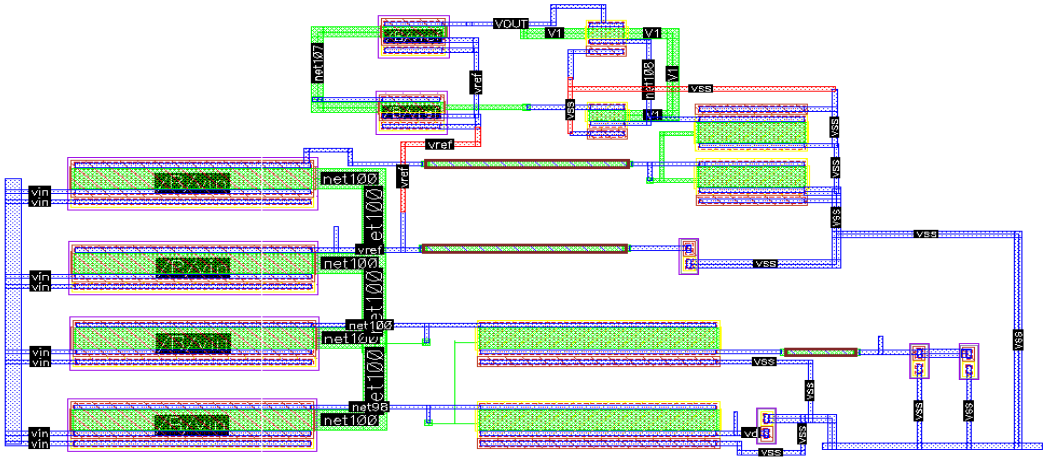


Figure 10: Layout of propose PVT circuit

4. CONCLUSIONS

An Inverter with PVT Compensation circuit is proposed in this paper. Validated in gpdk .18µm library on Cadence Virtuoso tool. Both inverter and PVT layout design on 0.18µm ADEXL window, the simulation and the measurement results have demonstrated that can minimize the static power dissipation for an inverter and approximate constant voltage has been achieved. The measured V_{REF} is 1.43+60mV. It provides a sufficient amount of voltage for circuit operation. The PVT circuit used in many areas like VCO, LDO many more. We can use that circuit for high accuracy of the circuit as well as compensation from supply and temperature. The proposed PVT may therefore be a key technology for low-voltage CMOS circuit design and provide less power dissipation for the load.

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