Performance Analysis of Interleaved Converter with Voltage Multiplier Module for High Efficiency Conversion and High Step-Up Voltage Gain

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Abstract – This paper proposes the performance analysis of interleaved converter with voltage multiplier module. In previous days, the high step-up DC-DC converters were used to produce a high step-up gain. Due to the single switch operation of the converter, the power level is limited and the input current ripple is large. Therefore, it is unsuitable for high power application. In order to overcome this problem, the interleaved boost converter with a PWM scheme was proposed. To achieve a high step-up voltage, gain, the voltage multiplier module is integrated with the interleaved converter. Thus, the voltage multiplier module is based on the concept of the switched capacitor and coupled inductor technique. However, the leakage inductor causes voltage transients across the switches. In order to eliminate the voltage spike, the lossless passive clamp circuit was introduced. Thus, the leakage energy is recycled and reverse recovery problem is eliminated. By selecting the low voltage rated power devices, the cost and voltage stress is reduced with improving efficiency. The proposed converter will be analyzed in PSIM model in continuous conduction mode (CCM) of operation and the converter analysis will be presented.

Index Terms - Coupled inductor, renewable energy sources, high step-up interleaved converter, voltage multiplier module, PSIM.

I. INTRODUCTION

Renewable energy plays an important role in day-to-day life applications. Thus, renewable energy sources causing harmful problems like global warming, the greenhouse effect, and fossils exhaustions are completely avoided. When considering the secure, robust, reliability and pollution - free environment [1-2]. The photovoltaic system becomes the better contribution for generating electricity among the renewable energy sources [3-5]. In general, the front stage conversion process will be the high step-up dc-dc converter. In recent years, the boost converter is widely used to produce high conversion ratio. However, in practical consideration, it is not possible to achieve a high conversion ratio without using a large duty cycle. Due to the larger duty ratio and higher components rating, the series problems like reverse recovery, voltage stress, and conduction losses will occur [6-11]. In order to avoid the large duty ratio, the better solution to use a transformer or coupled inductor [12-14]. Due to the disadvantages of the two switches in a conduction state, a single power device using high step-up dc-dc converter have been developed [15-16]. To achieve a high step-up voltage, gain and conversion ratio, the boost flyback converter with clamp mode coupled inductor was introduced. But the output voltage will be equal to the voltage stress [17-20]. In order to reduce the current ripple and magnetic component size with low cost, the interleaved structure was introduced. Then, the interleaved converter added with some switched capacitor cell was proposed. But the magnetic component size will be larger and volume occupied also increased. Thus, the high step-up boost converter with Winding Cross-Coupled Inductors (WCCI) was developed to extend the step-up voltage with proper turn ratio. In WCCI, the second and third winding will be act as dc input voltage source and are connected in series to the circuit. To overcome this problem, the passive lossless clamp scheme was introduced. Then, the voltage multiplier cell is inserted in between the winding cross-coupled inductor (WCCI) for voltage gain extension. But the circuit is complex and difficult to handle. By simplifying the circuit, the interleaved high step-up dc-dc converter with voltage multiplier cell was introduced. To increase the efficiency of the converter, the voltage multiplier module is added on the interleaved converter. The proposed interleaved converter consists of a voltage multiplier module. It is based on the concept of the switched capacitor and coupled inductor technique. In this converter, the conduction loss is reduced by the current sharing of energy stored in the magnetizing inductor. Then the diode reverse recovery problem also eliminated by making the current flow through the diode will become zero before the switch turned off.

II. PROPOSED TECHNOLOGY

The proposed topology consists of the voltage multiplier module which is integrated with the interleaved boost converter. In this voltage multiplier module, it consists of four diodes and four capacitors with the secondary side winding of the coupled inductor. The proposed interleaved converter consists of two capacitors and two diodes which are added on the coupled inductor secondary side. So, the coupled inductor makes the capacitor to discharge in series and also to charge in parallel. Moreover, there is a problem of using a coupled inductor. Because of the leakage inductor of the coupled inductor may produce high voltage transients on the
power switch. In order to reduce the voltage spike across the switches and to recycle the leakage energy, the lossless passive clamp circuit is proposed. During heavy load conditions, the voltage stress and input current ripple are larger. Further, the reduction of current ripple and voltage stress of the proposed converter introduce the interleaved PWM scheme for gate signal and that makes the components to be rated with low voltage. Thus, by selecting the low voltage rated power devices makes the voltage stress and conduction loss to be lower.

2.1. Circuit Configuration

The circuit configuration of the interleaved converter with voltage multiplier is shown in Fig. 2.1. It consists of dc input voltage source \( V_{in} \), two coupled inductors, two power switches \( S_1 \) and \( S_2 \), two clamp capacitors \( C_{c1} \) and \( C_{c2} \) and two clamp diodes \( D_{c1} \) and \( D_{c2} \), three output capacitors \( C_1 \), \( C_2 \), and \( C_3 \). Thus, the output diodes for boost operation with switched capacitors are represented as \( D_{b1} \) and \( D_{b2} \). Then, the output diodes for flyback-forward operation are represented as \( D_{f1} \) and \( D_{f2} \).

The equivalent model of circuit configuration consists of leakage inductors \( L_{k1} \) and \( L_{k2} \), magnetizing inductors \( L_{m1} \) and \( L_{m2} \), serious leakage inductor \( L_s \) and an ideal transformer instead of coupled inductor. The turn ratio of the coupled inductor \( n \) is defined by the same turn ratio \( N_s/N_p \).

![Figure 2.1. Circuit Configuration of the Proposed Converter System.](image)

In order to achieve the high voltage gain, the switched capacitor technique was proposed in the earlier days. In this topology, the high step-up voltage gain can be achieved without using a large duty cycle. From this switched capacitor technique, that the capacitor can charge in parallel and discharged in series. Based on this technique, the proposed converter introduced the combination of a coupled inductor and switched capacitor technique.

![Figure 2.2 Equivalent Circuit of the Proposed Converter System.](image)

The passive clamp circuit is used to recycle the leakage inductor energy to capacitor \( C_{c1} \) and \( C_{c2} \) and also the voltage spikes occur in the power switches \( S_1 \) and \( S_2 \) can be clamped. So, the voltage stress is reduced when compared to the other conventional boost converter topology. By selecting the low resistance \( R_{ds(ON)} \) of the switch, the conduction loss is reduced significantly. From this concept, we can reduce the voltage stress, cost, and conduction loss. By recycling the energy, the reverse recovery problem is reduced and also high efficiency is achieved. In addition, the high step-up voltage gain is achieved.

2.2. Operational Principle

The operating principle of the proposed interleaved converter describes in different modes of the switching period. To form an asymmetrical interleaved structure, two coupled inductors and two switched capacitors are proposed in the voltage multiplier module. The dashed block of the circuit configuration is a voltage multiplier module. By turn, the power switches \( S_1 \) and \( S_2 \) is in ON state. It will act as a forward converter. When the power switches \( S_1 \) and \( S_2 \) is in OFF state. It will act as a flyback converter. In order to simplify the circuit analysis, the following assumptions are made as follows.

1. By neglecting the leakage inductor like \( L_{k1} \), \( L_{k2} \), and \( L_s \).
2. The proposed interleaved converter utilizing components are made to be ideal.
3. Due to the infinite large capacitor, assume the voltage across all the capacitors should be constant.
The proposed topology will be operated only in continuous conduction mode (CCM) of operation.

### 2.3 Continuous-Conduction Mode (CCM) Operation

The current flow path of operating modes during each switching cycle at CCM will consist of eight modes as shown in Figure 2.3.

![Figure 2.3. Current flow path of operating modes during one switching period at CCM mode-I](image1)

![Figure 2.4. Current flow path of operating modes during one switching period at CCM mode-II](image2)

![Figure 2.5. Current flow path of operating modes during one switching period at CCM mode-III.](image3)

![Figure 2.6. Current flow path of operating modes during one switching period at CCM mode-IV.](image4)
Figure 2.7. Current flow path of operating modes during one switching period at CCM mode-V.

Figure 2.8. Current flow path of operating modes during one switching period at CCM mode-VI

Figure 2.9. Current flow path of operating modes during one switching period at CCM mode-VII

Figure 2.10. Current flow path of operating modes during one switching period at CCM mode-VIII

Mode-I ([t0-t1]): In mode-I operation, the stored energy of the series leakage inductors Ls will be quickly discharged to the load R0 through the output diode of flyback-forward Df2 and makes Ls current to become zero. The dc voltage source Vin charges
magnetic inductor \(L_m1\) and some amount of energy will be transferred to the coupled inductor secondary side. Thus, the current passes through leakage inductor \(L_k1\) and \(L_k2\) will increases and decreases linearly.

**Mode-II (t1-t2):** In mode-II operation, the dc source \(V_{in}\) charges the leakage inductor \(L_k1\) and \(L_k2\); and make \(i_{Lk1}\) and \(i_{Lk2}\) to increase linearly.

**Mode-III (t2-t3):** In mode-III operation, the stored energy of magnetizing inductor \(L_m2\) will transfer its energy to the secondary side coupled inductor. Thus, makes the is to flow through the output capacitor \(C_0\) by output diode \(D_f1\). The output voltage of the boost converter will be equal to the voltage-clamped by clamp capacitor \(C_{c1}\) across the power device \(S1\). The energy of the dc input voltage \(V_{in}\), leakage inductor \(L_k2\), magnetizing inductor \(L_m2\), and clamp capacitor \(C_{c2}\) will be discharged to the load \(R_0\). Thus, the voltage across the capacitor \(C1\ (V_{c1})\) will be twice the output voltage of the boost converter.

**Mode-IV (t3-t4):** In mode-IV operation, due to the current distribution of magnetizing inductor, the current flow through the clamp diode \(D_{c2}\) will become zero by nature. So, the conduction losses are reduced and reverse recovery problems are eliminated. Except for the clamp diode, \(D_{c2}\) all remains the previous state.

**Mode-V (t4-t5):** In Mode-V operation, the stored energy of the series leakage inductors \(L_s\) will be quickly discharged to the load \(R_0\) through the output diode of flyback-forward \(D_f1\) and makes \(L_s\) current to become zero. The dc voltage source \(V_{in}\) charges magnetic inductor \(L_m2\) and some amount of energy will be transferred to the coupled inductor secondary side. Thus, the current passes through leakage inductor \(L_k2\) and \(L_k1\) will be increases and decreases linearly.

**Mode-VI (t5-t6):** In mode-VI operation, the dc source \(V_{in}\) charges the leakage inductor \(L_k1\) and \(L_k2\); and make \(i_{Lk1}\) and \(i_{Lk2}\) to increase linearly.

**Mode-VII (t6-t7):** In mode-VII operation, the stored energy of magnetizing inductor \(L_m1\) will transfer its energy to the secondary side coupled inductor. Thus, makes the is to flow through the output capacitor \(C_0\) by output diode \(D_f2\). The output voltage of the boost converter will be equal to the voltage-clamped by clamp capacitor \(C_{c2}\) across the power device \(S1\). The energy of the dc input voltage \(V_{in}\), leakage inductor \(L_k2\), magnetizing inductor \(L_m1\), and clamp capacitor \(C_{c1}\) will be discharged to the load \(R_0\). Thus, the voltage across the capacitor \(C1\ (V_{c1})\) will be twice the output voltage of the boost converter.

**Mode-VIII (t7-t8):** In mode-VIII operation, due to the current distribution of magnetizing inductor, the current flow through the clamp diode \(D_{c1}\) will become zero by nature. So, the conduction losses are reduced and reverse recovery problems are eliminated. Except for the clamp diode, \(D_{c1}\) all remains the previous state. This mode of operation will be end at \(t=t8\) and the switching period will start to repeat.

From table 1 of CCM operation, we can describe the time interval, switch turn on and off period and also the devices should turn on and off sequences for the certain switching period.

During steady-state circuit analysis, the duty ratio of power switches will be interleaved with a 180° phase shift and greater than 0.5.

<table>
<thead>
<tr>
<th>Stages</th>
<th>Switch (S1)</th>
<th>Switch (S2)</th>
<th>Devices On</th>
<th>Devices Off</th>
<th>Reverse Biased</th>
</tr>
</thead>
<tbody>
<tr>
<td>t0-t1</td>
<td>ON</td>
<td>ON</td>
<td>(D_{f2})</td>
<td>(C_{c1})</td>
<td>(D_{c2})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(c_1)</td>
<td>(c_2)</td>
<td>(c_1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(b_1)</td>
<td>(b_2)</td>
<td>(f_1)</td>
</tr>
<tr>
<td>t1-t2</td>
<td>ON</td>
<td>ON</td>
<td>“</td>
<td>(C_{c1})</td>
<td>(D_{c2})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(c_1)</td>
<td>(c_2)</td>
<td>(b_1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(b_2)</td>
<td>(f_1)</td>
<td>(f_2)</td>
</tr>
<tr>
<td>t2-t3</td>
<td>ON</td>
<td>OFF</td>
<td>(D_{c1})</td>
<td>(C_{c1})</td>
<td>(D_{c1})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(c_2)</td>
<td>(b_1)</td>
<td>(b_2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(D_{c2})</td>
<td>(f_1)</td>
<td>(f_2)</td>
</tr>
<tr>
<td>t3-t4</td>
<td>ON</td>
<td>OFF</td>
<td>“</td>
<td>“</td>
<td>“</td>
</tr>
<tr>
<td>t4-t5</td>
<td>ON</td>
<td>ON</td>
<td>(D_{c1})</td>
<td>(C_{c1})</td>
<td>(D_{c1})</td>
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<tr>
<td></td>
<td></td>
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<td>(c_1)</td>
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<td></td>
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<td>(b_2)</td>
<td>(f_1)</td>
<td>(f_2)</td>
</tr>
<tr>
<td>t5-t6</td>
<td>ON</td>
<td>ON</td>
<td>“</td>
<td>(D_{c1})</td>
<td>(D_{c1})</td>
</tr>
<tr>
<td></td>
<td></td>
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<td>(c_2)</td>
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<td>(b_1)</td>
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<td></td>
<td></td>
<td></td>
<td>(b_2)</td>
<td>(f_1)</td>
<td>(f_2)</td>
</tr>
<tr>
<td>t6-t7</td>
<td>OFF</td>
<td>ON</td>
<td>(D_{c1})</td>
<td>(C_{c1})</td>
<td>(D_{c1})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(b_1)</td>
<td>(b_2)</td>
<td>(f_1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(D_{c2})</td>
<td>(c_2)</td>
<td>(b_2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(b_2)</td>
<td>(f_1)</td>
<td>(f_2)</td>
</tr>
</tbody>
</table>

The waveform of continuous conduction mode (CCM) of operation is shown in Figure 2.11.
III. CONVERTER PERFORMANCE ANALYSIS

To achieve a high step-up voltage, gain with reduced voltage stress and higher efficiency, the following interleaved converter is analysed as follows.

3.1. Voltage Gain

The output voltage of the boost converter is depending on the voltage across the clamp capacitor \( C_c \). So it can be derived in equation (1) as follows,

\[
V_{co} = \frac{1}{1 - D} V_{in} \tag{1}
\]

The output voltage of the boost converter will be twice when one of the power devices is turned off as shown in equation (2),

\[
V_{c1} = \frac{1}{1 - D} V_{in} + V_{cc} = \frac{2}{1 - D} V_{in} \tag{2}
\]

The energy stored in the primary side winding will be charged the output capacitor \( C_2 \) & \( C_3 \).

When the power switch \( S_1 \) is off state and \( S_2 \) in on state, thus the voltage induced on the secondary side coupled inductors \( N_{s1} \) & \( N_{s2} \) will be equal to \( V_{c2} \).

The voltage across the capacitors \( C_2 \) and \( C_3 \) can be derived in equation (3),

\[
V_{c2} = V_{c3} = n V_{in} \left( 1 + \frac{D}{1 - D} \right) = \frac{n}{1 - D} V_{in} \tag{3}
\]

The output voltage can be equated in equation (4) as follows,

\[
V_0 = V_{c1} + V_{c2} + V_{c3} = \frac{2n+2}{1 - D} V_{in} \tag{4}
\]

Then, the voltage gain of the proposed interleaved converter is derived in equation (5),

\[
\frac{V_0}{V_{in}} = \frac{2n+2}{1 - D} \tag{5}
\]

From this equation (5), we can conclude that the proposed converter can extend the voltage gain without using the large duty cycle.

3.2. Switch Voltage Stress

To simplify the converter analysis, the capacitor voltage ripples are neglected. The voltage stress on power switches \( S1 \) & \( S2 \) is clamped and it can be derived as,
To reduce the conduction loss and cost of the power converter by selecting the low voltage rated device with low RDs on is confirmed by equation (6). This feature says that the proposed converter is suitable for high power applications. The curve of the relation between switched voltage stress and turns ratio is shown in figure 3.1.

\[ V_{s1} = V_{s2} = \left(\frac{2}{1-D}\right)V_{in} = \left(\frac{1}{2n+2}\right)V_0 \]  \hspace{1cm} (6)

3.3. Diode Voltage Stress

In order to eliminate the reverse recovery problem of the proposed converter, the following equations (7-12) are derived as follows.

\[ V_{Dc} = V_{Dc1} = V_{Dc2} = V_{C1} \] \hspace{1cm} (7)

\[ V_{Dc} = V_{in}\left(\frac{2}{1-D}\right) = \left(\frac{V_0}{1+n}\right) \] \hspace{1cm} (8)

\[ V_{Db} = V_{Db1} = V_{Db2} = V_{c1} - V_{c2} \] \hspace{1cm} (9)

\[ V_{Db} = \left(V_{in}\left(\frac{1}{1-D}\right) = \left(\frac{V_0}{2n+2}\right) \right) \] \hspace{1cm} (10)

\[ V_{Df} = V_{Df1} = V_{Df2} = V_{c2} + V_{c3} \] \hspace{1cm} (11)

\[ V_{Df} = \left(\frac{2n}{1-D}\right)V_{in} = \left(\frac{n}{n+1}\right)V_0 \] \hspace{1cm} (12)

When turn ratio \( n \) increases with the voltage stress on the diode \( D_f \). The voltage relationship between diode voltage stress and turns ratio \( n \) is shown in figure 3.2.
3.4. Performance Analysis for Phase Shift Interleaved PWM Scheme

For a high step up and high power applications, the input current ripple should be lower. But in single phase operations, the ripple current will be higher and not suitable for high power applications. During a converter analysis, the duty ratio of the power system will be interleaved with 180° degree phase shift for higher duty ratio.

3.5. Current Sharing Performance

When one of the power switches is turned off, the stored energy of the magnetizing inductor will transfer the current through the three different paths. The current sharing performance makes the conduction loss and power capacity to decreases and increases by lowering the effective value and peak value of the current. This feature makes the proposed converter from reverse recovery problems and also reduces the switching loss made by conduction.

3.6. Advantages of the Interleaved Converter

When comparing the advantages and feature of other interleaved converter, the proposed converter is efficient and consists of the following advantages,

1. Low conduction loss and low input current ripple make the lifetime of the converter to increase and it is suitable for high power applications.
2. Mostly the renewable energy sources require the high step-up gain which obtained in the proposed topology.
3. The high-efficiency converters are used for the effective application. So, the leakage energy is recycled by a lossless passive clamp circuit.
4. By selecting the low voltage power device with low $R_{ds(on)}$, the voltage stress is reduced.
5. By using the current sharing performance, the conduction loss and reverse recovery losses are eliminated.

IV. DESIGN SPECIFICATIONS AND SIMULATION RESULTS OF THE PROPOSED CONVERTER

Table 2 - Specification for the proposed converter

<table>
<thead>
<tr>
<th>Attributes</th>
<th>Ranges</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage ($V_{in}$)</td>
<td>24V</td>
</tr>
<tr>
<td>Switching frequency ($f_s$)</td>
<td>50kHz</td>
</tr>
<tr>
<td>Maximum output power</td>
<td>200W</td>
</tr>
<tr>
<td>Magnetizing inductor ($L_m$)</td>
<td>48µH</td>
</tr>
<tr>
<td>Leakage inductor ($L_k$)</td>
<td>0.25µH</td>
</tr>
<tr>
<td>Capacitors $C_1$</td>
<td>56µF/100V</td>
</tr>
<tr>
<td>Capacitors $C_2$/C_3</td>
<td>22µF/200V</td>
</tr>
<tr>
<td>Capacitors $C_0$</td>
<td>180F/450V</td>
</tr>
<tr>
<td>Output voltage ($V_0$)</td>
<td>400V</td>
</tr>
</tbody>
</table>

Figure 4.1. PSIM circuit for CCM operation.
Figure 4.2. PSIM circuit for DCM operation.

Figure 4.3. Typical waveform for proposed converter under CCM operation.

Figure 4.4. Output voltage of the proposed converter
V. CONCLUSION

In this work, we analyzed the interleaved converter using coupled inductors and switched capacitor technique. High step-up interleaved converter voltage multiplier module is presented for high step-up voltage gain and efficiency conversion. The converter is simulated in PSIM package and results are verified. The principle and experimental results for an interleaved converter are presented. The operation principle and modes of operation are discussed thoroughly. The voltage multiplier module is integrated with the interleaved converter to increase the voltage gain and efficiency conversion ratio without using a large duty cycle is presented. Then by using the lossless passive clamp circuit leakage inductor energy is recycled and voltage stress is reduced. Thus the phase shifted interleaved PWM 180° degree the input current is reduced in the proposed topology. The reverse recovery losses and conduction losses are eliminated by current sharing performance and it was analyzed thoroughly. For a full load condition and light load condition, the efficiency obtained will 96.4% and 97.11%. From this topology, high voltage gain and efficiency are achieved. The analysis of the interleaved converter has been discussed in detail. Finally, a 40V – 380V had been achieved.

REFERENCES