FLIP-FLOPS WITH LOW POWER AND LOW GLITCH DESIGN AND IMPLEMENTATION

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Abstract: The usage of C-elements in this paper results in new designs of static dual-edge triggered (DET) flip-flops with specific circuit behavior. Two high-performance designs and designs that improve on conventional Latch-MUX DET flip-flop such that none of their internal circuit nodes follow changes in the input signal are shown. Low energy dissipation owing to glitches at the input is a typical feature of the given flip-flops. Novel DET flip-flops are compared to current DET flip-flops utilizing simulation in a high-performance 180 nm CMOS technology using Microwind and digital schematic SoftWare simulation results. Finally, in terms of delay and power consumption, compare the current and suggested findings for the master-slave dual edge-triggered flip-flop design.

Index Terms - **DET, Microwind, Digital schematic.**

I. INTRODUCTION

Dual Edge Triggered (DET) flip-flops operate at half the clock frequency of single edge-triggered (SET) flip-flops, resulting in lower power consumption in synchronous logic circuits [1]-[2]. DET flip-flops, which typically contain more transistors and internal nodes than SET flip-flops, have a greater circuit complexity due to this decrease. The Latch-MUX DET flip-flop [1], [9] is a popular DET flip-flop design that has two input latches multiplexed to one output. The two latches are level-triggered by clock levels in opposing directions, ensuring that a transparent latch follows every change at the input. Glitches at the input harm the flip-power flop's dissipation as a consequence of this transparency. When errors are infrequent, [2] estimates that Latch MUX DET flip-flops waste less power than SET flip-flops. Pulsed DET flip-flops [1]-[4] are examples of other DET flip-flop designs. In general, a pulsed DET flip-flop operates by making its output latch visible to the input signal for a brief period after each clock edge, long enough to latch the input value safely. The power dissipation of these flip-flops is less reliant on input signal transitions between clock edges, but clock activity causes higher power dissipation.

This article offers C-element-based static DET flip-flop designs. The paper is divided into five parts. The low-glitch-power LG C flip-flop, implicit-pulsed IP C flip-flop, floating-node FN C flip-flop, and two high-performance conditional- toggle CT C, and CTF C flip-flops are shown in Section II. The simulation setup and comparison technique to compare the given flip-flops to each other and six previously published DET flip-flop designs are described in Section III. The results of comprehensive Monte Carlo and voltage scaling simulations are presented and discussed in Section IV.
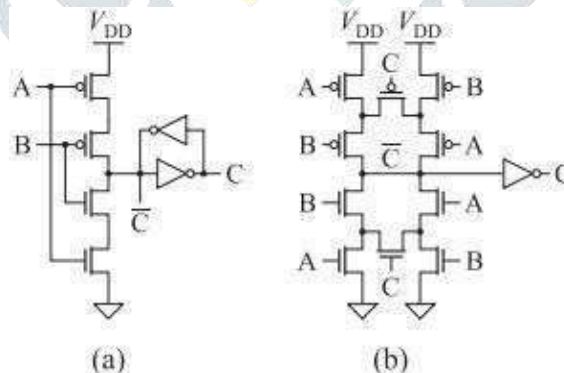

Fig. 1 Transistor-level implementations of a C-element (a) The weak- feedback. (b) The symmetric [6] implementations.

A C-element is a three-terminal device having two inputs and one output, as described in [5.] When all of the inputs are the same, the output changes to that value; when the inputs aren't the same, the initial output value is maintained. This device functions as a latch that may be set and reset using the proper signal levels at the input. Figure 1 depicts the two transistor-level implementations of C-elements utilized in this work. Other implementations were explored, but none outperformed the implementations in Fig. 1 in terms of performance, power, or circuit size. The innovative DET flip-flops described here are made up of C-elements and variants on their circuit topologies.

II. LITERATURE SURVEY

Increasing circuit speed undoubtedly remains a crucial aim in the development of logic architecture in the future. Predictions in technology and performance scaling [1] suggest that technology alone is unlikely to deliver the necessary performance increase. Therefore circuit design improvements are anticipated to supply a part of the performance. More precisely, the storage components' timing overhead is expected to drop from about three fan-out-of-four delays (3 FO4) to around 1.5 FO4. In addition, new clocking

subsystem improvements are required to decrease the clocking subsystem's power usage as a percentage of overall power. In high-performance CPUs, approximately 30% – 50% of power is used on clocking alone, according to the breakdown [2], [3]. These improvements are especially essential since high-end systems' power consumption increases exponentially over time, with less effective heat removal and no obvious technological answer insight.

If the clock frequency continues to follow the path anticipated by the roadmap for the next several years (3–5 GHz), frequency scaling will become more challenging. The significance of clock uncertainties grows when the clock period is lowered to 200 ps, and sophisticated multiple-phase clocking will become unfeasible owing to rising timing uncertainties and power consumption.

Dual-edge triggered (DET) clocking method utilizes DET storage elements (DETSE) to conserve clocking power by capturing the value of the input after both rising and falling clock transitions. DETSE is nontransparent; otherwise i.e., it keeps the captured value at the output. By maintaining the data throughput of single-edge triggered (SET) clocking at half clock frequency, the DET clocking method offers a one-time solution to frequency scaling. However, this method must guarantee that the latency and energy consumption of DETSE are similar to those of SET storage components to effectively utilize the power savings in the clock distribution network (SETSE). Furthermore, synchronizing the operation with both clock edges makes timing-sensitive to the clock duty cycle and increases the clock distribution system's clock uncertainties. In the last decade, researchers have looked at DET systems [4]–[8]. Almost all previously published studies, on the other hand, focused on the circuit design of the storage components. A clear description of timing and energy measurements and an assessment of the impact of dual-edge clocking on system power were missing, making it challenging to compare DET and SET methods fairly.

A flip-flop is an electrical circuit that saves the logical state of one or more data input signals in reaction to a clock pulse. Receiving and maintaining data for a short time period during repeating clock periods, allowing other circuits in a system to continue processing data. Power dissipation is an essential component in VLSI circuit design, and the clock network accounts for a significant portion of it (up to 50%). Because the effective input voltage to the transistors is reduced when the supply voltage is reduced, the speed of the logic circuits may be reduced.

The design for low power problems can seldom be addressed without precise power prognostication and enhancement techniques. In order to determine the power dissipation in a digital circuit, specific techniques must be used throughout the design process in order to satisfy the power restrictions and prevent an expensive redesign effort. The most common synchronous digital circuits are edge triggered flip-flops. D-type flip-flops are the fundamental components of contemporary VLSI systems, accounting for a significant portion of overall power dissipation in digital systems [12]. The entire clock-related power consumption in synchronous VLSI circuits is made up of the power used by the clock circuits, clock buffers, and flip-flops [3]. There are many variables that influence power consumption, such as $P = C f$ [5], where power is proportional to the square of voltage.

Voltage scaling is the most efficient method to decrease power usage. Also, voltage scaling is linked to threshold voltage scaling, which may cause leakage power to rapidly rise. The clock frequency may be lowered substantially by employing double-edge triggered flip-flops (DCETFFs), preferably by half while maintaining the data processing rate. The DCETFF architecture saves energy on both the distribution network and flip-flops by half the frequency. It is desirable to minimize the number of clocked transistors in circuits to lower their clock demands.

III. EXISTING TECHNIQUES

Extensive simulations have been performed to compare the five presented DET flip-flops against each other and also against six previously reported DET flip-flop designs. Two versions of the novel FN_C flip-flop have been considered: The version presented in Fig. 10 and the version with the symmetric C-element of Fig. 1(b) replacing the weak-feedback output C-element. The latter version is denoted as FN_C (sym) in the comparison. For a fair comparison, all flip-flops include input, output, and clock buffering.

Fig. 2 shows transistor-level schematic diagrams of the six previously reported DET flip-flop designs that are considered in this paper for comparison. The designs are as follows: LM, described in [9], is a variant of a standard Latch MUX DET design; EP is a variant of the common Explicit-Pulsed DET flip-flop that was introduced in [4]. LM_C is a Latch-MUX design, introduced in [7], that uses a C-element at the output to perform the function of a MUX. TSP, presented in [10], is the True-Single-Phase Clock DET flip-flop design that follows the Latch-MUX approach but does not use the inverted clock signal. CP, introduced in [1], is the Conditional Precharge DET flip-flop. f) IP, described in [3], is the Implicit-Pulsed DET flip-flop.

The flip-flops were implemented in the 28 nm GF 28HPP CMOS technology. Implementations were optimized for the minimum energy-delay product. The delay metric was the maximum CK-Q delay for the optimization step because it is straightforward to measure. Optimizations were performed by the simulation tool in an automated fashion: The tool varied transistor sizes within the specified bounds and chose the best sizes for each flip-flop after several iterations. The search bounds were chosen so that resultant designs would meet recommended design rules most of the time. Weak transistors were allowed to use minimum width rather than the recommended minimum width as it would otherwise result in poor circuit performance.

Simulations were performed on schematic designs. Conservative estimates of layout parasitic were included in the simulation models at both the optimization and final simulation stages. These estimates were provided by one of the design kit features: The kit can automatically include its own estimation of the RC parasitic interconnect network into schematic simulation models. Parasitic extraction and post layout simulations were also performed on selected designs and were compared to schematic simulations that used automatic estimation of parasitic. Post-layout simulations showed that the kit's estimates for small designs are often conservative. Compact circuits often perform slightly faster in post-layout simulations than in schematic simulations with the automatic parasitic network estimation turned on.

The simulation test bench that is used in this comparison is very similar to the ones used in [3], [11], [12]. The Q output of a simulated flip-flop is connected to a load of four symmetric inverters with their n-type transistors sized at a minimum recommended width. The generated data and clock signals are connected to the flip-flop's inputs through two inverters. The clock frequency is 1 GHz, which results in a 0.5 ns cycle time. Most of the measurements relating to energy and delays were taken from Monte Carlo simulations with full global and local process variations enabled. The simulation junction temperature was set to 70 ∘C. For each flip-flop, 2000 Monte Carlo points were simulated. Variations for a number of metrics are reported as coefficients of variation (CV). The CV input, output, and clock buffering. The flip-flops are (a) LM [9], (b) EP [4], (c) LM_C [7], (d) TSP [10], (e) CP [1], and (f) IP [3]. is also known as the relative standard deviation (RSD) which is defined as the ratio between standard deviation (SD) and mean. In this technology, simulation models make somewhat conservative assumptions about sources of variation when performing Monte Carlo analysis on schematic designs. Variations in physical implementations are expected to be lower than the ones reported from these simulations.
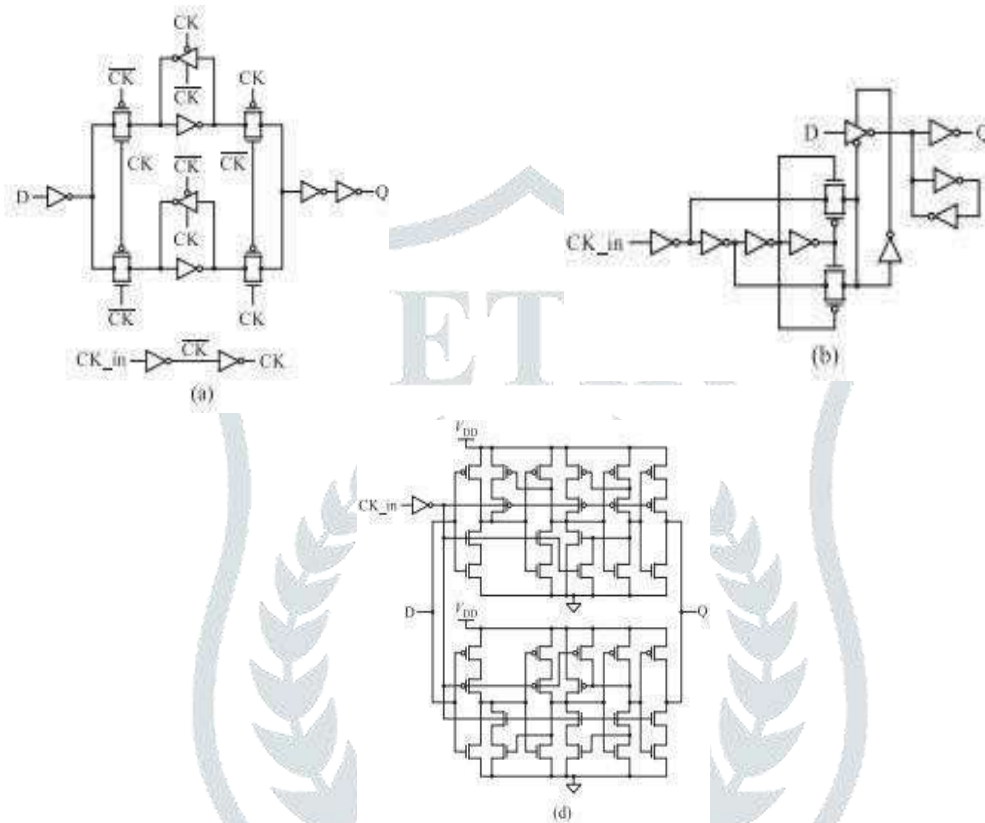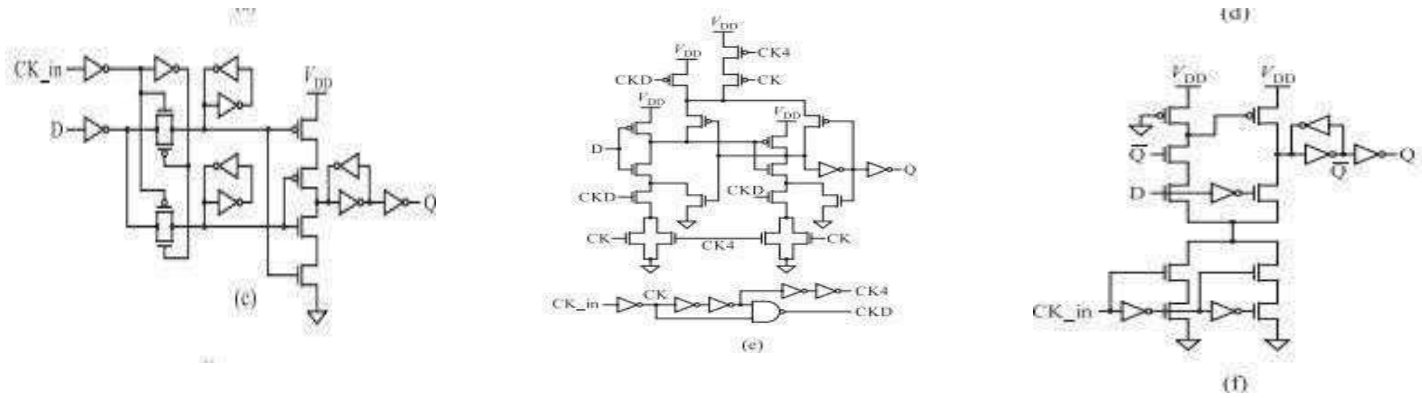
Fig. 2 Transistor-level schematic diagrams of the six previous DET flip-flop designs that are considered in this paper for comparison with the presented novel DET flip-flops. All circuits include input, output, and clock buffering. The flip-flops are (a) LM [9], (b) EP [4], (c) LM_C [7], (d) TSP [10], (e) CP [1], and (f) IP [3].

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The following parameters were evaluated from Monte Carlo simulations.

- Power at 10%, 50%, and 100% switching activities P0.1, P0.5, and P1 respectively.

- Power-delay products PDP0.1, PDP0.5, and PDP1 for each of the three power values with the delay being the D-Q delay.

- Maximum CK-Q delay t_{cq}.

- Worst-case minimum D-Q delay t_{dq}.

The power is measured from the calculated E(t) curve of the total dissipated energy versus simulation time. This curve is computed by integrating simulated power supply, data input, and clock input currents for each simulated flip-flop in the following way:

E (t) = VDD

$$\times \int \left[I_{DD} + \frac{1}{2} (I_D + |I_D| + I_{CK\_in} + |I_{CK\_in}|) \right] dt. \quad (1)$$

In (1), the power supply current is integrated along with the positive currents flowing into the flip-flop's D and CK_in inputs. Currents flowing out of the flip-flop's inputs are discarded. These negative currents are either the result of a weak feedback inverter working against the D input driver, in which case the current is supplied by the flip-flop and is thus already included in IDD or are the result of a driver sinking the voltage at the input's parasitic capacitance, in which case this energy was already counted when the driver previously charged this capacitance with a positive current.

Part of the measured energy is dissipated outside the flip-flop's circuit. This includes energies dissipated by the input drivers on driving the flip-flop's inputs and the energy dissipated by the flip-flop on driving the output load. Although the latter depends solely on the size of the load, the comparison is fair in that the load is the same for all flip-flops. The CK-Q delay is measured as the maximum delay between the CK and Q transitions for the four possible cases of CK and Q. For each case, the D transition happens sufficiently early so as not to affect the timing of the Q transition.

The D-Q delay of a flip-flop is generally considered to be a more important metric than just the CK- Q delay [13]: Some flip-flops (e.g., the EP design) allow input changes to be captured well after a clock transition whereas others do not. In this sense, the D-Q delay is the time the flip-flop takes out of the clock cycle. Thus, the D-Q delay is used for PDP calculations in this paper. For every Monte Carlo point, multiple simulations were performed in order to measure the worst-case minimum D-Q delay for that point. There are four possible cases of CK and Q transitions. For each case, a parametric sweep is run with the sweep variable being the timing of the D transition relative to the CK transition. The minimum D-Q delay is found for each of the four cases. For every Monte Carlo point, the worstcase minimum D-Q delay is then the maximum of these four minimums. Fig. 17 illustrates this procedure for a particular Monte Carlo point of the LM flip-flop. For illustration purposes, the step in the D-CK transition sweep variable was set to 0.04 ps. In final simulations, the step was set to 1.25 ps to reduce the number of simulations. For this example, the difference in delays measured with 0.04 ps and 1.25 ps resolutions of the D-CK sweep variable is less than 0.06 ps. Such a small difference is due to the steepness of D-Q vs. D-CK curves reducing to 0 around their minimums

Independent simulations were performed to measure the hold time th of the flip-flops for the typical process corner. For each flip-flop, for all four cases of CK and Q transitions, th was measured as the minimum amount of time D needs to be unchanged after a clock transition so as not to result in the flip-flop failing to latch the correct value, increase the CK-Q delay by more than 40%, or result in a glitch of more than half the VDD voltage. Timings of D transitions were swept with a 0.05 ps step to record the hold time values with a 0.1 ps precision. A separate set of simulations were performed to assess the impact of glitches on the flip-flops' power dissipation. In these simulations, the Q output is steady across clock cycles. The Q-to-Q and Q-to-Q transitions for one glitch are introduced at the D input in between clock transitions. The total dissipated energy is then recorded after the next clock transition including the energy of restoration of the flip-flop's internal states. Energy dissipation due to one and three glitches is measured. The energies are denoted as G1 and G3 respectively. The recorded numbers are averages for the four possible cases of CK and Q. All energy measurements include leakage currents. More precise leakage simulations were performed using dedicated IDDQ models that are provided with the technology kit. The result is reported as IDDQ. The results are averaged across eight cases of D, Q, and CK. The reported values include leakage through D and CK_in inputs and exclude the leakage through the Q output.

IV. PROPOSED TECHNIQUES

The DET flip flop proposed in [1] is exposed in Fig. 3. This flip-flop is basically a Master Slave flip-flop structure. having two data paths. The upper data path consists of a Single Edge Triggered flip- flop implemented using transmission gates. This works on positive edge. The lower data path consists of a negative edge triggered flip-flop implemented using transmission gates. Both the data paths have feedback loops connected such that, whenever the clock is stopped, the logic level at the output is retained. This flip flop has 20 transistors. In these 20 transistors, 10 transistors are clocked transistors.
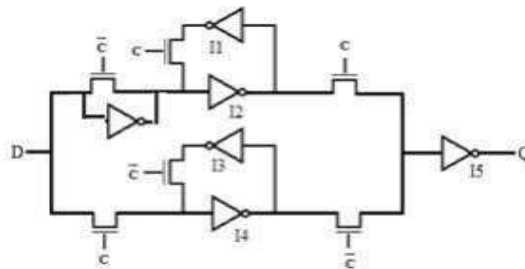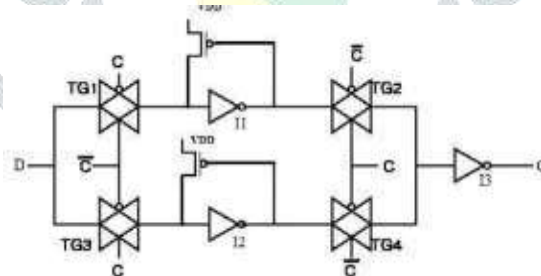

Fig.3: Proposed DEFET in

DET flip-flop proposed in [2] is shown in figure 4. This flip flop is similar to Fig. 1 except that feedback has been changed. On rising edge the upper data path is triggered and on falling edge lower data path is triggered. In the Fig. 4 an inverter and a PMOS transistor are used to hold the logic level when the Transmission gate is closed. When the data value high, the inverter is switch the signal to low, so will be make the PMOS transistor which pull the data up to the high. When value of data is low then the inverter Fig. Fig. 4

Proposed DEFET switch the signal to high, which will isolate the data from VDD and keep the value low. For high output, this type of flip-flop is give static functionality since a PMOS transistor connected to VDD is used in the feedback network, but the static functionality for low output is not provided by this flip-flop. That will make the circuit to behaving like a dynamic circuit.

The proposed Double Edge Triggered Flip-Flop (DCETFF) design is exposed in Fig. 19. The contractual unit of flip-flop is a Master Slave flip flop which consists of two data paths. The proposed flip-flop's operation is same to that of figure 1, but number of clocked transistors is reduced from 10 to 6 by replacing the transmission gates by using n-type pass transistors. The designed circuit using 6 clocked transistors and total 10 transistors. Inverter shown in figure is made by using sub-circuit design. Also W/L ratio is adjusted for making the transistors working in saturation region. Basically, n- type pass transistors give weak high but in figure 3, the n-type pass transistors is followed by an inverter, which results in strongly high. So the proposed DCETFF is free from threshold voltage loss problem of pass transistors in Fig. 5. Therefore the feedback network of Gig. 1 is distorted by replacing the p-type pass transistor by n-type pass transistor since; the area incurred by NMOS is less than that of PMOS transistor in order to compensate the mobility constraint of NMOS and PMOS transistors. Thus the proposed Design has become more efficient in terms of area, power and speed which showing better performance compare to conformist designs.
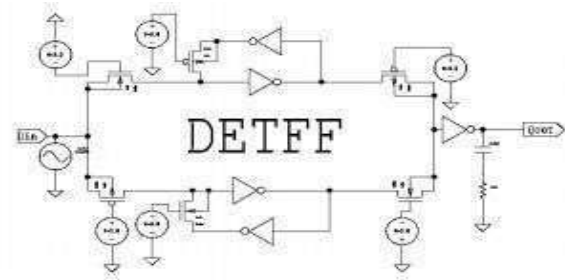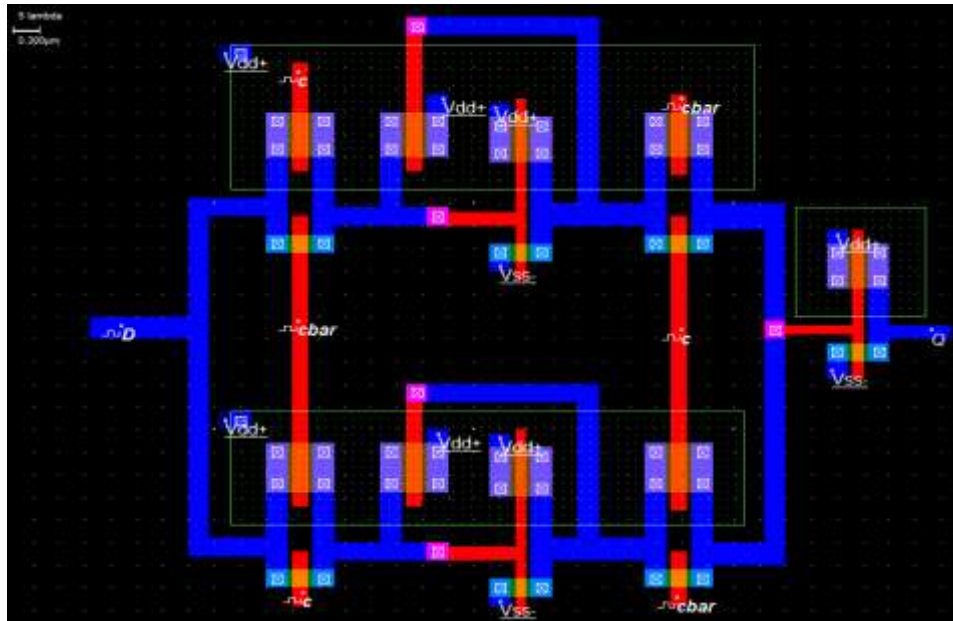
Fig. 5 Proposed DCETFF

V. RESULTS
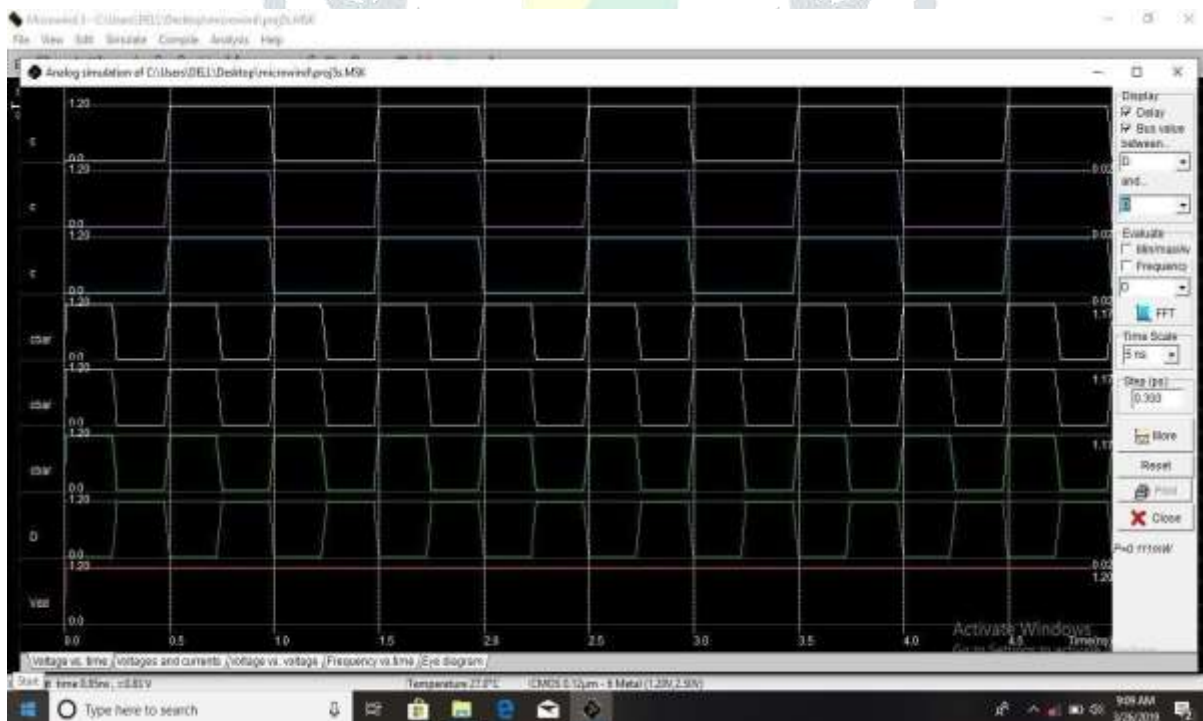

Fig. 6 Layout for Proposed Technique

Fig. 7 PROPOSED OUTPUT

Table 1 Comparison of performance of Existing and Proposed Technique

PARAMETERS	EXISTING METHOD	PROPOSED METHOD
Voltage	1.8000	1.8000
Current	-236.0294u	-2.4366u
Power	424.8529u	4.3859u
Power Description	424.8529u watts	4.3859u watts

VI. CONCLUSION

Five novel DET flip-flop designs have been presented. The new designs were compared to previous DET flip-flops using simulation in the 28 nm GF 28HPP CMOS technology. The novel LG_C design and its derivatives were shown to significantly improve on Latch-MUX DET flip-flop designs in the area of energy dissipation due to glitches at the input, which makes themuseful for designs with large logic depth that are prone to glitching. The novel CT_C and CTF_C designs can be used in high- performance scenarios as they were found to have superior power and power-delay products during periods of high switching activity. Extensive Monte Carlo simulations were carried out to demonstrate that the novel flip-flops are robust under process variations. The new FN_C design was found to be one of designs least susceptible to process variations. Voltage scaling simulations were performed that show that the performance of the presented flip-flops scales very similarly to that of previous DET flip-flops. The DCET flip-flops are simulated with different clock frequencies ranging from 1MHz to 10GHz. Simulation results show that the proposed DCETFF has improvement of 65.61% in terms of average power when compared with DCETFF2. The proposed design also has an improvement of65.61% and 25.85% in terms of power delay product (PDP) as compared to DCETFF1 and DCETFF2 respectively. The proposed design has minimum average power and lowest PDP than existing designs.

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