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Implementation of seven level inverter with power factor correction

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Abstract: - The power electronics plays a major role in our day-to-day life. There is not even a device running in our homes without power converter devices encrypted in them. Thus, the use of power converter devices is greatly increased. In this project, a seven-level modified cascaded multilevel inverter is proposed for industrial drive applications. Apart from selecting the conventional level inverters, Multilevel inverters has been chosen for the industrial drive applications as it reduces the total harmonic distortion. The involvement of higher number of switches increases the complexity of the system, which leads to losses in switching, producing huge harmonics and in the end, it entirely reduces the efficiency of the system. The cascaded multilevel inverter involves only fewer switches, where it reduces the complexity of the system which in turn reduces the harmonics and reduces the complexity of the system and in total it reduces the total harmonics distortion. This paper reduces the cost of system and increases the penetration of renewable energy system into distribution system.

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I. Introduction

Inverter is a device which converts DC power into AC. The power in the battery is in DC mode and the motor that drives the wheels usually uses AC power, therefore there should be a conversion from DC to AC by a power converter, inverter is used for this conversion [1]. The two-level is the simplest topology used for this conversion that consists of four switches. Each switch needs an anti-parallel diode, so there should be also four anti-parallel diodes. There are many other topologies for inverters. A multilevel inverter (MLI) is a power electronic system that produces a sinusoidal voltage output from several DC sources. These DC sources can be fuel cells, solar cells, ultra-capacitors, etc. The major function of multilevel inverters is to generate a better sinusoidal voltage and current in the output by using switches in series. Since many switches are put in series the switching angles are important in the multilevel inverters because all of the switches should be switched in such a way that the output voltage and current have low harmonic distortion (THD). Comparing two-level inverter topologies of the same power ratings, MLIs also have the advantage that the harmonic components of line-to-line voltages fed to the load are reduced owing to its switching frequencies. The multilevel inverters have become increasingly attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width modulated (PWM) inverters. The MLI produces improved output waveforms, low EMI, lower total harmonic distortion (THD) and reduced filter size. Multilevel inverter topology requires the least components for a given number of levels. Multilevel inverters can be classified into three types. Diode clamped multilevel inverters, flying capacitor multilevel inverters and cascaded H-bridge multilevel inverter. The THD is decreased by increasing the number of levels. Though, an output voltage with low THD is desirable, increasing the number of levels leads to more hardware, also the control will be more complicated. It is a tradeoff between price, weight, complexity and a very good output voltage with lower THD. Among these multilevel topologies the

diode clamped inverters (DCMLI), particularly, the three-level structure has a wide popularity in motor drive applications besides other multi-level inverter topologies. But it has got limitations such as complexity and number of clamping diodes for the DCMLIs, as the level exceeds. The Flying Capacitor Inverters (FCMLI) are based on balancing capacitors on phase buses and generate multilevel output voltage waveform clamped by capacitors instead of diodes. Cascaded H-Bridge MLI topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H bridges are connected in series, the DC sources must be isolated from each other. The need of several sources on the DC side of the inverter makes multilevel technology attractive for photo voltaic applications .

The only drawback of the multilevel converter is that it requires a large amount of semiconductor switches. Lower voltage rated switches can also be used in the multilevel converter and as a result the active semiconductor cost is not considerably increased when compared with the two-level cases. On the other hand, each active semiconductor added requires associated gate drive circuitry and adds further complication to the converter mechanical layout. Another disadvantage is that small voltage steps are typically formed by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available and series capacitors require voltage balance. A multilevel converter can be implemented in different ways, each with advantages and disadvantages. The simplest techniques which involve the parallel or series connection of conventional converters is to form the multilevel waveforms. Complicated structures actually insert converters within converters. Whatever approach is being chosen, the subsequent voltage or current rating of the multilevel converter will become a multiple of the individual switches, and therefore the power rating of the converter can exceed the limit imposed by the individual switching devices. The paper is organized as follows: Different multi-level inverter topologies such as Diode-Clamped inverter, Capacitor Clamped inverter, and Cascaded Multi cell inverter are discussed, initially for understanding the features of the multilevel inverters and the seven-level inverter topology for each configuration is discussed. The comparative study of the seven-level inverter of different topologies are studied.

II. THEORY

A. 5-level Multilevel Inverter For 5-level inverter, the topology is presented in Figure 1. This topology consists of a full-bridge inverter, an auxiliary circuit (comprises of one switching element and four diodes) and two capacitors as voltage divider. The multilevel inverter is connected after the dc power supply. The main point of the auxiliary circuit is to generate half level dc supply voltage [3]. It also reduced the layout complexity compared to other multilevel inverter topology such as flying-capacitor topology, diode-clamped topology and hybrid topology, and these topologies can be studied in various papers such as in [4] and in [5]. The operations of the new topology were presented in literature [3], [6] and [7]. The output voltage levels according to the switch on-off conditions were tabulated in Table I. The switch in auxiliary circuit must be properly switched considering the direction of the load current.

B. 7-level Multilevel Inverter The topology of 7-level inverter is similar to 5-level topology, only the auxiliary circuit now was added with an additional circuit. In general, 7-level inverter consists of a fullbridge inverter, two bidirectional switches (the auxiliary circuit), and three capacitors as voltage divider illustrated in Figure 2. To ensure that the power flows from the PV arrays to the grid, high dc bus voltages are necessary. LCL filter is used to filter the current to be injected into the utility grid. Seven output voltage level can be achieved when the switching signal for the IGBTs in the topology were done properly. The required seven levels of output voltage are generated, and the operation was explained in literature [8].

C. Power Factor Power factor is the ratio between real power and apparent power in a circuit. The formula for power factor is

$$\text{Power factor } (\cos\theta) = \frac{active\ power}{apparant\ power} = \frac{P}{S}$$

Where θ is the angle difference (in degrees) between output voltage and output current. Unity power factor is the best. The load with higher power factor will draw less currents, hence decrease the lost in distribution system and therefore wasted energy will be less.

D. Total Harmonic Distortion (THD) THD is a measurement of the harmonic distortion is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.THD is used to characterize the linearity of a systems

and the power quality of electric power systems. According to IEEE standard of THD limits, total harmonic current distortion shall be less than 5% of the fundamental frequency current at rated inverter output.

E. Efficiency In general, efficiency is a measurable concept, quantitatively determined by the ratio of output to input. In this system, input power is the power delivered from PV arrays, while the output power is the power at the grid. PV array's voltage must be higher than of Vgrid to inject current into the grid, or current will be injected from the grid into the inverter. This means that PV arrays must be the one that deliver the power for the grid, so that the grid can consume the power.

III. MODULATION TECHNIQUE

A. PWM Modulation Technique for 5-level Multilevel Inverter The modulation technique used in this inverter topology is sinusoidal pulse width modulation (SPWM) technique. The principle is to generate gate signal by comparing a triangular carrier signal with two reference (sinusoidal) signals, which having same frequency and in phase, but different offset voltages as shown in Figure 3.

Figure 3. PWM switching signal generation for 5-level multilevel inverter

According to the amplitude of the voltage reference, Vref, the operational interval of each mode varies within a certain period. The modes are separated as

Mode 1 : 0<wt<$\theta_1 \& \theta_2 < wt < \pi$

Mode2 : $\theta 1 < wt < \theta 2$

Mode 3 : π <wt<$\theta_3 \& \theta_4 < wt < 2\pi$

Mode 4 : $\theta 3 < wt < \theta 4$

The phase depends on the modulation index. The modulation index of the proposed five-level PWM inverter is defined as

$$M = \frac{A_m}{2Ac}$$

where AM is the peak value of reference voltage and AC is the peak value of carrier wave. The modulation index recommended in this technique is to be between 0.66 and 1.

B. PWM Modulation Technique for 7-level Multilevel Inverter Seven level multilevel inverter's PWM modulation contain three reference signal named Vref1, Vref2, and Vref3. These three reference signals had same frequency, amplitude and phase. The difference is that they had different offset values. The reference signals are positive sine waveform. To produce the signals for the switches, the reference signals need to be compared to a carrier signal (Vcarrier); a triangular wave signal, using a comparator. The reference signals were each compared with the carrier signal. If Vref1 had exceeded the peak amplitude of Vcarrier, Vref2 was then compared with Vcarrier until it had exceeded the peak amplitude of Vcarrier. Then, Vref3 would be compared with Vcarrier until it reached zero. Once Vref3 had reached zero, Vref2 would be compared until it reached zero. Then, onward, Vref1 would be compared with Vcarrier [8] and the process continues. Figure 4 shows the signal generation.

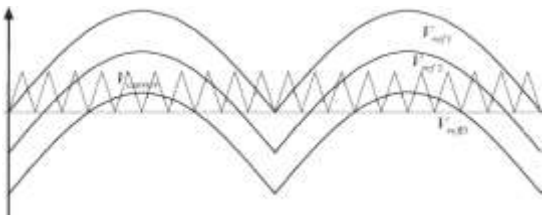

Figure 4. PWM switching signal generation for 7-level multilevel inverter

Six modes were operated in one cycle of this inverter and described as follows [8]

Mode 1: $0 < \omega t < \theta_1$ & $\theta_4 < \omega t < \pi$

Mode 2: $\theta_1 < \omega t < \theta_2$ & $\theta_3 < \omega t < \theta_4$

Mode 3: $\theta_2 < \omega t < \theta_3$

Mode 4: $\pi < \omega t < \theta_5$ & $\theta_8 < \omega t < 2\pi$

Mode 5: $\theta_5 < \omega t < \theta_6$ & $\theta_7 < \omega t < \theta_8$

Mode 6: $\theta_6 < \omega t < \theta_7$

The phase angle depends on modulation index. For dual reference signal used in 5-level modulation technique, equation (1) was used. Therefore, for three reference signals, the modulation index is defining as

$$M = \frac{A_m}{3Ac}$$

.2 Simulation:

6.2.1 Introduction:

SIMULINK is a software package for modelling, simulating, and analyzing dynamical systems. It supports linear and nonlinear systems, modelled in continuous time, sampled time, or a hybrid of the two. Systems can also be multi rate, i.e., have different parts that are sampled or updated at different rates. For modelling, SIMULINK provides a graphical user interface (GUI) for building models as block diagrams, using click-and-drag mouse operations. With this interface, you can draw the models just as you would with pencil and paper. SIMULINK includes a comprehensive block library of sinks, sources, linear and nonlinear components, and connectors. You can also customize and create your own blocks. This approach provides insight into how a model is organized and how its parts interact. After a model is defined, it can simulate, using a choice of integration methods, either from the SIMULINK menus or by entering commands in MATLAB's command window. The menus are particularly convenient for interactive work, while the command line approach is very useful for running a batch of simulations. Using scopes and other display blocks, the simulation results can see while the simulation is running.

6.2.2 Simulation result discussion:

Here in this circuit each h bridge will produce three different output voltage namely +Vdc, -Vdc and 0V. Labels such as got and from are used to give gate signals to the MOSFET dries which will ultimately give a seven-level output voltage which is shown

later. A voltage of 4V dc is applied to each H-bridge configuration to get an output voltage of 12V. The output is viewed using the scope block which is used give the output of the simulated circuit in MATLAB.

A sine wave of amplitude 3 and frequency 2*pi*50 act as the reference signal is used to compare with triangular carrier signal which is produced by repeating sequence block parameter. The modulation index of the reference signal and comparator signal is 0.8. When the reference signal is greater than the comparator signal, we get the output signal which is given to the gate section of the MOSFET ‘s or IGBT ‘s used as switches.

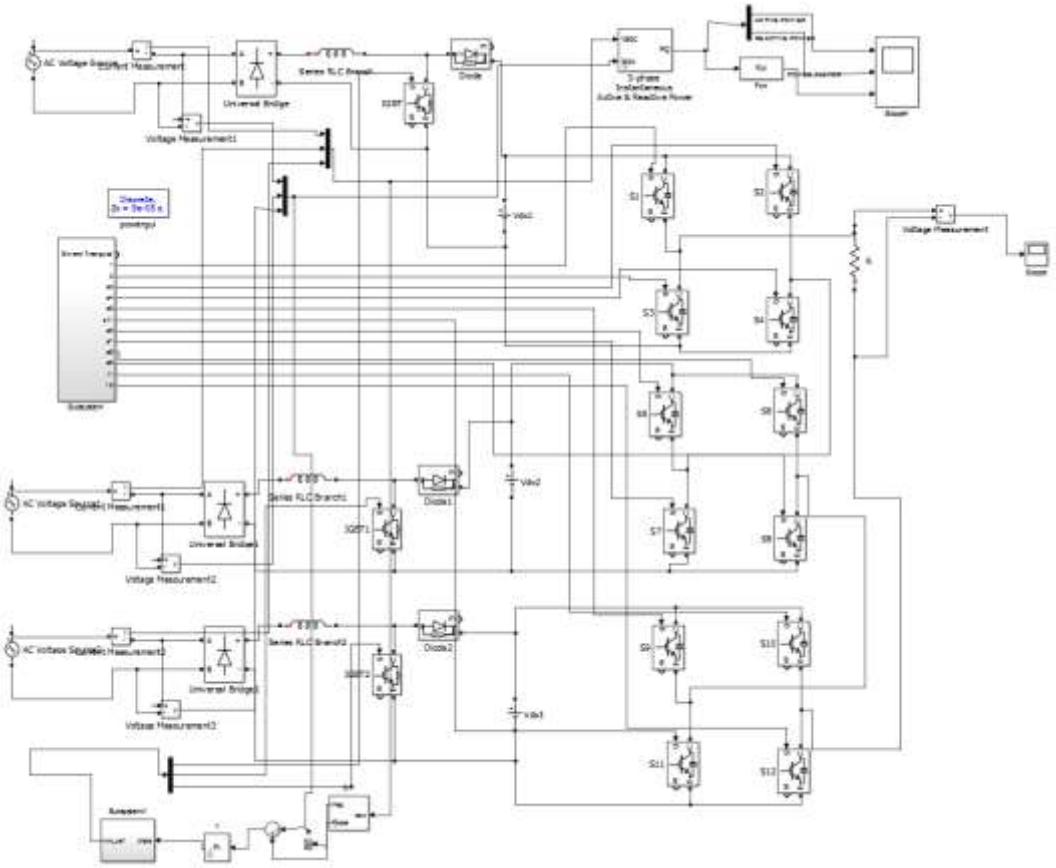

Figure 5 simulation model of 7 level inverter power factor improvment

Output Waveform:

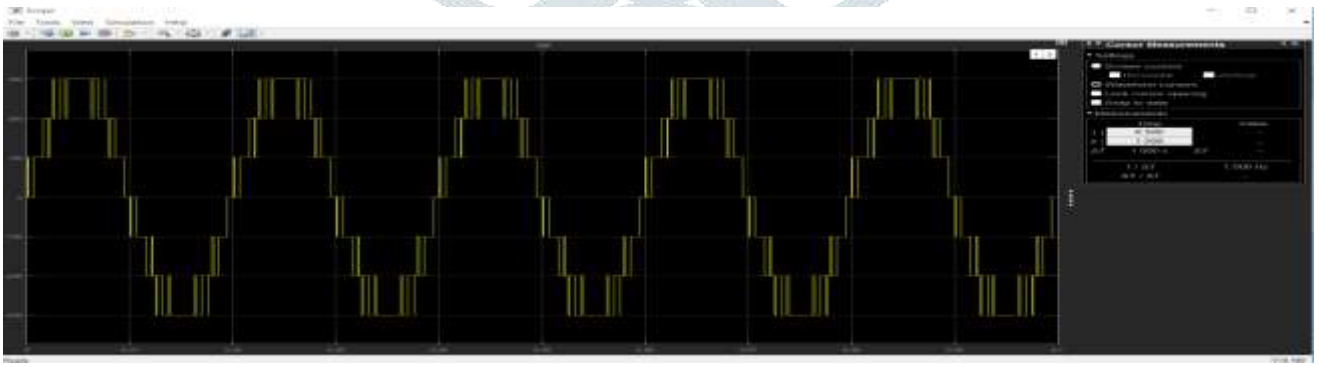

Figure 6 : Output waveform of final simulation

FFT ANALYSIS

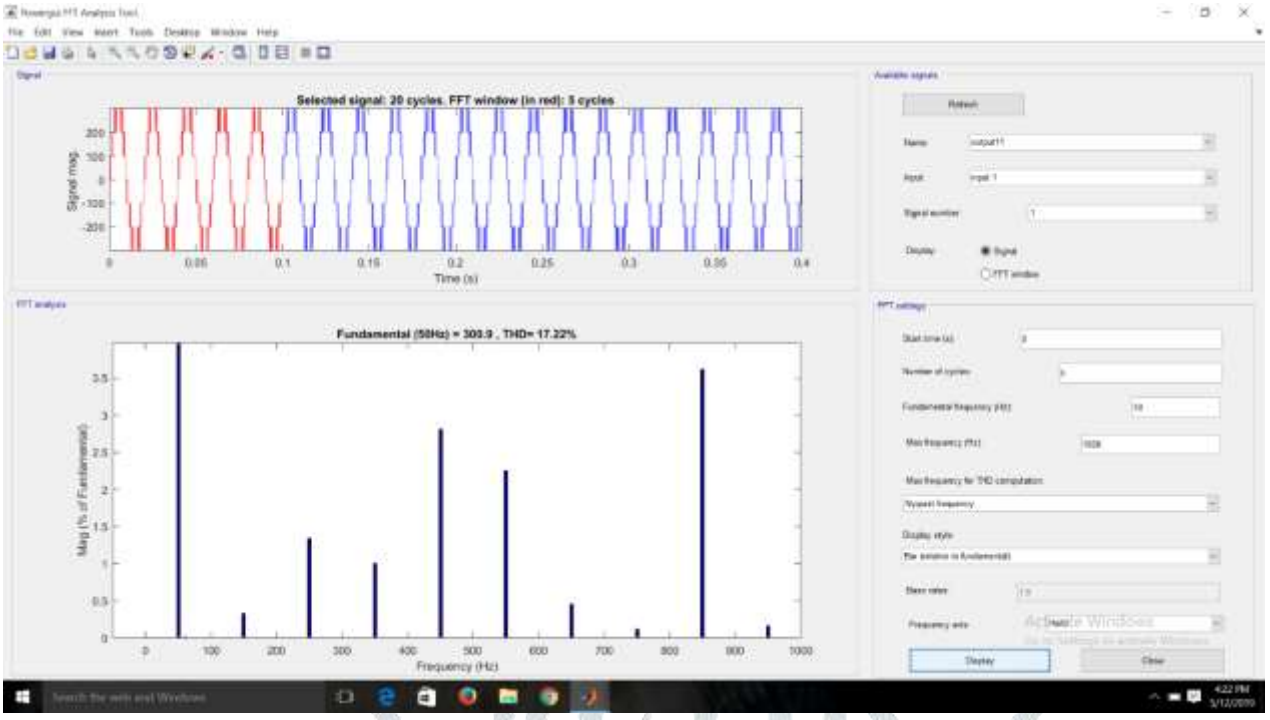

Figure 8: FFT analysis of waveform

I. Conclusion:

In this paper improved power factor seven level inverter is proposed that can meet the requirement of desired power factor. The structure of proposed system consists of H bridge cascaded form, power factor correction circuit. The simulation of seven level inverter with power factor correction is carried out in MATLAB/Simulink to identify level which has comparatively less total harmonic distortion and improved power factor in its output. The feasibility and effectiveness of the proposed system has been successfully evaluated with various simulation studies and practical implementation.