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# MODELLING OF TSFOI DC-DC CONVERTER

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**Abstract:**
*Two-Source Fourth Order Integrated (TSFOI) dc-dc converter is designed to process the power from two sources $V_{g1}$ and $V_{g2}$. This converter facilitate regulation of dc-bus voltage and LVS current. In the power conversion process it performs bucking operation for $V_{g1}$, buck-boost operation for $V_{g2}$. Here, the magnitude of power drawn from each source may not be same. In view of this fact, there will be an interaction(s) among the systems states and these interactions arise due to (i) the power drawn from different sources in each mode is different (ii) the rate at which energy is stored and released in the circuit by the inductive and capacitive elements in each mode are different. These interactions need to be quantified. This can be performed using transfer function matrix. The transfer function matrix (TFM) of the TSFOI converter is obtained .*

**Introduction**

The switched mode dc-dc converters are designed using either with a single source or with multiple sources. Multiple sources are interfaced in dc-dc converters to allow both flexibility and reliability. A single integrated converter that accommodates different types of sources forms a multi-input/multi-port converter (MICs/MPCs). Such a MIC can continue to operate even if one of the dc sources has failed. Different sources that can be used in MICs are wind turbines, fuel cells, photo voltaic (PV) panels, batteries, super capacitor/ultra-capacitor/electric double layer capacitor.

Steady-state analysis of the two-input integrated converters gives deep understanding of multi-input converter design while the dynamic analysis gives the interaction effects, pairing of the input-output variables, controller structure selection and controller design aspects. In case of power processing using two dc sources, a two-input integrated converter is a viable option for power control as it uses less number of components and is simple in structure. The TSFOI DC-DC Converter for the optimal power distribution was proposed, where the modelling aspects were explored in detail. In this work, TSFOI DC-DC Converter is designed to process the power from two different sources $V_{g1}$ and $V_{g2}$. These two converters facilitate regulation of dc-bus voltage and LVS current. The system modelling plays an important role in the design and implementation of the integrated converter control systems. Mathematical modelling of a converter is obtained in several ways for example
(a) state-space averaged models,
(b) sampled-data model PWM switch model, and
(c) dynamic phasors model
Though many modelling methods were reported in literature to define dynamics of the dc-dc integrated converters, but the state-space averaging model is popularly used. PWM switch model using averaging method is reported already in the literature. State-space modelling aspects of multi-input converters have been discussed. Overview of modelling aspects applicable to dc-dc converter systems is reported. An exact small-signal discrete-time model for multiphase converter is proposed. Exact small-signal discrete-time analysis have been used to formulate the model of digitally controlled boost converters, two-input TSFOI converter, two-input integrated converters, and for multi-state dc-dc converter.

**2.2. Significance of Modelling**

Modelling is an essential and most important aspect for such converter systems. It helps the designer in many ways:
(1) To understand the operating principles of a converter in various modes.
(2) For analyzing the dynamics of integrated dc-dc converter.
(3) Thorough steady-state and transient analysis.
(4) Useful for design of converter control system.
If the exact model is not known, the controller designed may not be effective in regulating the integrated converter variables and the resultant system may exhibit poor dynamic performance characteristics.

### 2.3 Modeling of TSFOI DC-DC Converter

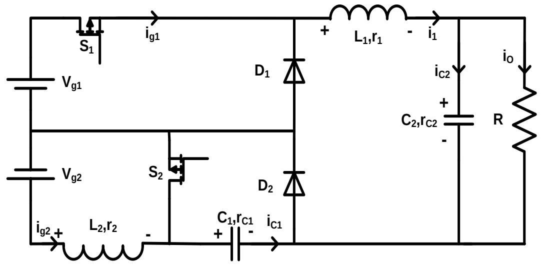


Fig.2.3. (a) Circuit Diagram of TSFOI DC-DC Converter

The TSFOI converter shown in Fig. 2.3 (a) is suitable for power processing from two sources $V_{g1}$, which is a high voltage source (HVS) and $V_{g2}$, which is a low voltage source (LVS). It has two diodes, four energy storage elements, and two switching devices; hence it forms a fourth-order system. During this power conversion process it performs bucking operation for HVS, $V_{g1}$, buck-boost operation for the LVS, $V_{g2}$.

The converter is having the following salient features (a) both sources $V_{g1}$ and $V_{g2}$ are supplying power to down-stream loads by drawing continuous currents from their respective sources and hence the corresponding source ripple currents are low. (b) automatic load transfer on to the first dc source if the second dc source capacity, a weak source with limited power supplying capacity, is less than the load demand, and (c) simple control strategy, with or without overlap of duty ratio signals, as there are only two switching devices need to be controlled.

Based on the current status of the inductors, the converter circuit may be operating in either continuous (CCM) or discontinuous conduction mode (DCM). These modes of operation is also depends on (i) the amount of power processing (ii) switching frequency and (iii) physical location of inductors in the circuit. As this converter is meant for processing higher load demands, where one dc source unable to meet the complete load demands and hence the inductor currents are mostly continuous in nature. Hence, analysis and design of the proposed converter is presented for continuous current mode (CCM) of operation.

The two switches of this converter turns-ON and turns-OFF using the fixed-frequency PWM control signals $d_1$, $d_2$, and the constant switching frequency is $1/T_s$ . The two switches can be synchronized in two ways by using either trailing edge or leading edge digital pulse width modulations. Although both can be used for this converter, but a trailing-edge digital pulse width modulated switching scheme is used in this work.

Depending on the available power and load demand with each dc source, three different cases will arise based on the controlling duty signals, which are: (i) $d_1$ is equal to $d_2$ (ii) $d_1$ is less than d2 (iii) $d_1$ is greater than $d_2$. In the first case the circuit will undergoes only two structural changes in one switching cycle while in last two cases the circuit will undergoes three different structural changes in one cycle. Here, the integrated circuit is analysed by considering $d_1 > d_2$, using the trailing-edge synchronized switching signals.

For $d_1 > d_2$, case the switching sequence in one cycle is:

(i) $S_1$ and $S_2$ both are ON, $D_1$ and $D_2$ both are in off-state
(ii) $S_1$-ON and $D_2$-ON, $S_2$-OFF and $D_1$-OFF
(iii) $S_1$-OFF and $D_2$-ON, $S_2$-OFF and $D_1$-ON.

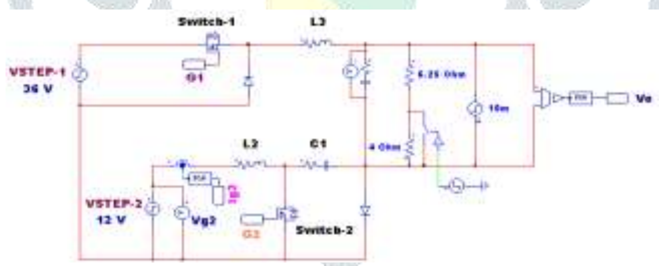


Fig. 1. Circuit diagram of the proposed two-input integrated DC-DC converter.

**Mode-1 operation: ($0 < t < d_2T_s$):**

In this mode the switches both $S_1$ and $S_2$ are in the ON -state and the diodes $D_1$ and $D_2$ both are in OFF-state. The equivalent circuit diagram for mode-1 is shown in the Fig.2.1 (b). In mode-1 operation the inductors $L_1$ and $L_2$ are charging through the voltage sources $V_{g1} + v_{c1}$ and $V_{g2}$ respectively, and the load demand is met by the load capacitor $C_2$. The capacitor $C_1$ is discharged through the switch $S_2$.

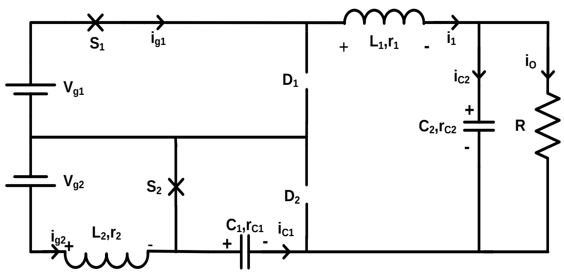


Fig. (b) Mode-1 Circuit Diagram

Applying Kirchhoff's current law at the node that contain $L_1$, $C_2$, R

$$i_1 = I_0 + i_{C_2}$$

$$i_1 = \frac{v_{C_2} + r_{C_2} i_{C_2}}{R} + i_{C_2}$$

Defining $b = \left( \frac{R}{R + r_{C_2}} \right)$

$$i_1 = \frac{v_{C_2}}{R} + \left( \frac{R + r_{C_2}}{R} \right) i_{C_2}$$

$$i_{C_2} = b\left( i_1 - \frac{v_{C_2}}{R} \right)$$

Expressing $i_{C_2}$ in terms of the state variable $v_{C_2}$

$$C_2 \frac{dv_{C_2}}{dt} = bi_1 - \frac{b}{R} v_{C_2}$$

$$\frac{dv_{C_2}}{dt} = \frac{b}{C_2} i_1 - \frac{b}{RC_2} v_{C_2}$$

Applying the Kirchhoff's voltage law through load resistor and the capacitor $C_2$

$$v_0 = v_{C_2} + r_{C_2} i_{C_2}$$

Substituting the eqn. (2.1) in eqn. (2.3a)

$$v_0 = v_{C_2} + br_{C_2}\left( i_1 - \frac{v_{C_2}}{R} \right)$$

$$v_0 = ai_1 + \left( 1 - \frac{a}{R} \right) v_{C_2}$$

$$v_0 = ai_1 + bv_{C_2}$$

Applying Kirchhoff's current law at the node that contain $C_2$, $C_1$, R

$$i_{C_1} = -i_1$$

$$\frac{dv_{C_1}}{dt} = -\frac{i_1}{C_1}$$

Apply the Kirchhoff's voltage law in loop2 which contain the elements $V_{g2}$, $L_2$ along with its parasitic resistances and the conducting switch $S_2$,

$$V_{g_2} = v_{L_2} + r_2 i_2$$

$$v_{L_2} = V_{g_2} - r_2 i_2$$

$$L_2 \frac{di_2}{dt} = -r_2 i_2 + V_{g_2}$$

$$\frac{di_2}{dt} = \frac{r_2}{L_2} i_2 + \frac{V_{g_2}}{L_2}$$

Applying the Kirchhoff's voltage law to the loop1, which contain the elements $V_{g1}$, conducting switch $S_1$, $L_1$, $C_1$, $C_2$ along with its parasitic resistances

$$L_1 \frac{di_1}{dt} + r_1 i_1 - v_{C_1} - r_{C_1} i_{C_1} + v_0 = V_{g_1}$$

$$v_{L_1} + r_1 i_1 - v_{C_1} - r_{C_1} i_{C_1} + v_0 = V_{g_1}$$

$$v_{L_1} = V_{g_1} - r_1 i_1 + v_{C_1} + r_{C_1} i_{C_1} - v_0$$

Substituting equation (3) and $i_{C_1} = -i_1$

$$v_{L_1} = V_{g_1} - r_1 i_1 + v_{C_1} - r_{C_1} i_1 - \left( ai_1 + bv_{C_2} \right)$$

$$v_{L_1} = V_{g_1} - \left( r_1 + r_{C_1} + a \right) i_1 + v_{C_1} - bv_{C_2}$$

Defining $k_1 = \left( r_1 + r_{C_1} + a \right)$

$$\frac{di_1}{dt}=\frac{V_{g_1}}{L_1}-\frac{\left(r_1+r_{C_1}+a\right)}{L_1}i_1+\frac{v_{C_1}}{L_1}-\frac{b}{L_1}v_{C_2}$$

$$\frac{di_1}{dt}=\frac{V_{g_1}}{L_1}-\frac{k_1}{L_1}i_1+\frac{v_{C_1}}{L_1}-\frac{b}{L_1}v_{C_2}$$

The dynamics of power conversion process is in mode-1 of operation described using state model given in (1).

$$\dot{x}=A_1x+B_1u$$

$$\hat{y}[n]=E_{01}\hat{x}[n]$$

$$\hat{y}[n]=\left[\hat{v}_0(z)\quad \hat{i}_g(z)\right]^T$$

$$\begin{bmatrix}\hat{v}_0(z)\\ \hat{i}_{g2}(z)\end{bmatrix}=\begin{bmatrix}E_1\\ P_1\end{bmatrix}\hat{x}(z)=E_{01}\hat{x}(z)$$

Where

$$A_1=\begin{bmatrix}-\frac{k_1}{L_1} & 0 & \frac{1}{L_1} & -\frac{b}{L_1}\\ 0 & -\frac{r_2}{L_2} & 0 & 0\\ -\frac{1}{C_1} & 0 & 0 & 0\\ \frac{b}{C_2} & 0 & 0 & -\frac{b}{RC_2}\end{bmatrix}\qquad B_1=\begin{bmatrix}\frac{1}{L_1} & 0\\ 0 & \frac{1}{L_2}\\ 0 & 0\\ 0 & 0\end{bmatrix}$$

$$E_1=[a\quad 0\quad 0\quad b]\qquad F_1=[0]\qquad P_1=[0\ \ 1\ \ 0\ \ 0]$$

**Mode-2 operation: ($d_2Ts<t<d_1Ts$)**

In mode2 of operation $S_1$ and $D_2$ both are in the ON-state and $S_2$ and $D_1$ are in OFF-state. The equivalent circuit for mode-2 is shown in the Fig.2.1(c). In mode-2 operation the inductors $L_1$ and $L_2$ are charging through the voltage sources $V_{g1}$ and $V_{g2}$ respectively.

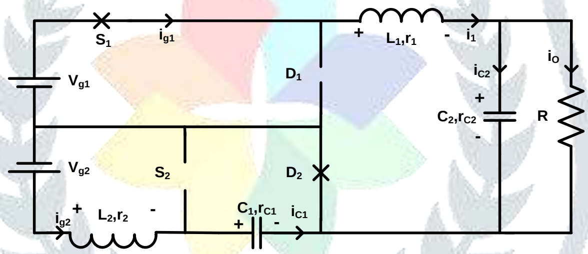


Fig.2.1 (c) Mode-2 Circuit Diagram

Applying Kirchhoff's current law at the node that contain $L_1$, $C_2$, R

$$i_1=I_0+i_{C_2}$$

$$i_1=\frac{v_{C_2}+r_{C_2}i_{C_2}}{R}+i_{C_2}$$

$$i_1=\frac{v_{C_2}}{R}+\left(\frac{R+r_{C_2}}{R}\right)i_{C_2}$$

As defined $b=\left(\frac{R}{R+r_{C_2}}\right)$ , $a=\left(\frac{Rr_{C_2}}{R+r_{C_2}}\right)$ , $a=br_{C_2}$

$$i_{C_2}=b\left(i_1-\frac{v_{C_2}}{R}\right)$$

$$C_2\frac{dv_{C_2}}{dt}=bi_1-\frac{b}{R}v_{C_2}$$

$$\frac{dv_{C_2}}{dt}=\frac{b}{C_2}i_1-\frac{b}{RC_2}v_{C_2}$$

$$v_0=v_{C_2}+r_{C_2}i_{C_2}$$

Applying Kirchhoff's current law at the node that contain $C_1$ and $L_2$

$$i_{C_1} = i_2$$

$$C_1 \frac{dv_{C_1}}{dt} = i_2$$

$$\frac{dv_{C_1}}{dt} = \frac{i_2}{C_1}$$

Applying the Kirchhoff's voltage law to loop-2 which contain the elements $V_{g2}$, $L_2$, $C_1$ along with its parasitic resistances and conducting diode $D_2$.

$$v_{L_2} + r_2 i_2 + r_{C_1} i_{C_1} + v_{C_1} = V_{g_2}$$

$$v_{L_2} = V_{g_2} - r_2 i_2 - r_{C_1} i_{C_1} - v_{C_1}$$

$$i_{C_1} = i_2$$

$$L_2 \frac{di_2}{dt} = V_{g_2} - (r_2 + r_{C_1}) i_2 - v_{C_1}$$

$$\frac{di_2}{dt} = \frac{V_{g_2}}{L_2} - \frac{(r_2 + r_{C_1})}{L_2} i_2 - \frac{v_{C_1}}{L_2}$$

Applying the Kirchhoff's voltage law to loop1 which contain the elements $V_{g1}$, conducting switch $S_1$, $L_1$, $C_2$ along with its parasitic resistances

$$L_1 \frac{di_1}{dt} + r_1 i_1 + v_0 = V_{g_1}$$

$$v_{L_1} + r_1 i_1 + v_0 = V_{g_1}$$

Substituting $v_0 = ai_1 + bv_{C_2}$

$$v_{L_1} + r_1 i_1 + ai_1 + bv_{C_2} = V_{g_1}$$

$$v_{L_1} = V_{g_1} - \left(r_1 i_1 + ai_1 + bv_{C_2}\right)$$

$$v_{L_1} = V_{g_1} - r_1 i_1 - ai_1 - bv_{C_2}$$

$$L_1 \frac{di_1}{dt} = V_{g_1} - r_1 i_1 - ai_1 - bv_{C_2}$$

$$\frac{di_1}{dt} = \frac{V_{g_1}}{L_1} - \frac{(r_1 + a)}{L_1} i_1 - \frac{b}{L_1} v_{C_2}$$

$$A_2 = \begin{bmatrix} -\frac{(r_1+a)}{L_1} & 0 & 0 & -\frac{b}{L_1} \\ 0 & -\frac{(r_2+r_{C_1})}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{b}{C_2} & 0 & 0 & -\frac{b}{RC_2} \end{bmatrix} \qquad B_2 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

$$E_2 = [a \quad 0 \quad 0 \quad b] \qquad F_2 = [0] \qquad P_2 = [0 \quad 1 \quad 0 \quad 0]$$

**Mode3 operation: ($d_1 T_s < t < T_s$)**

In this mode of operation S1 and $S_2$ both are in off-state and the diodes $D_2$ and $D_1$ both are in on-state. The equivalent circuit for mode-3 is shown in the fig below. In mode-3 the load demand is provided by the voltage source $V_{g2}$.

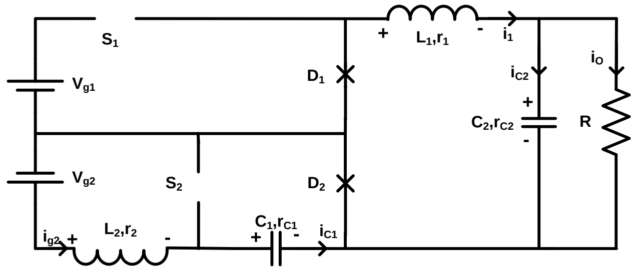


Fig.2.1 (d) Mode-3 Circuit Diagram

Applying Kirchhoff's current law at the node that contain $L_1$, $C_2$, R

$$i_1 = I_0 + i_{C_2}$$

$$i_1 = \frac{v_{C_2} + r_{C_2} i_{C_2}}{R} + i_{C_2}$$

$$i_1 = \frac{v_{C_2}}{R} + \left(\frac{R + r_{C_2}}{R}\right) i_{C_2}$$

$$b = \left(\frac{R}{R + r_{C_2}}\right) \quad , \quad a = \left(\frac{R r_{C_2}}{R + r_{C_2}}\right) \; , \; a = b r_{C_2}$$

$$i_{C_2} = b\left(i_1 - \frac{v_{C_2}}{R}\right)$$

$$C_2 \frac{dv_{C_2}}{dt} = b i_1 - \frac{b}{R} v_{C_2}$$

$$\frac{dv_{C_2}}{dt} = \frac{b}{C_2} i_1 - \frac{b}{RC_2} v_{C_2}$$

$$v_0 = v_{C_2} + r_{C_2} i_{C_2}$$

Substituting the equation (1) in the above equation

$$v_0 = v_{C_2} + b r_{C_2}\left(i_1 - \frac{v_{C_2}}{R}\right)$$

$$v_0 = a i_1 + \left(1 - \frac{a}{R}\right) v_{C_2}$$

$$v_0 = a i_1 + b v_{C_2}$$

Applying Kirchhoff's current law at the node that contain $C_2$, $L_2$

$$i_{C_1} = i_2$$

$$C_1 \frac{dv_{C_1}}{dt} = i_2$$

$$\frac{dv_{C_1}}{dt} = \frac{i_2}{C_1}$$

Apply the Kirchhoff's voltage law to loop1 which contain the conducting diodes $D_1$ and $D_2$, $L_2$, $C_1$ along with its parasitic resistances

$$v_{L_1} + r_1 i_1 = -v_0$$

$$v_{L_1} = -v_0 - r_1 i_1$$

$$L_1 \frac{di_1}{dt} = -v_0 - r_1 i_1$$

$$L_1 \frac{di_1}{dt} = -\left(a i_1 + b v_{C_2}\right) - r_1 i_1$$

$$v_0 = a i_1 + b v_{C_2}$$

$$L_1 \frac{di_1}{dt} = -\left(a + r_1\right) i_1 - b v_{C_2}$$

$$\frac{di_1}{dt} = -\frac{\left(a + r_1\right)}{L_1} i_1 - \frac{b}{L_1} v_{C_2}$$

Apply the Kirchhoff's voltage law to loop2 which contain the elements $V_{g2}$, $L_2$, $C_1$ along with its parasitic resistances and conducting diode $D_2$.

$$V_{g_2} = v_{L_2} + r_2 i_2 + r_{C_1} i_2 + v_{C_1}$$

$$v_{L_2} = V_{g_2} - \left(r_2 i_2 + r_{C_1} i_2 + v_{C_1}\right)$$

$$v_{L_2} = V_{g_2} - \left(r_2 + r_{C_1}\right) i_2 - v_{C_1}$$

$$L_2 \frac{di_2}{dt} = V_{g_2} - \left(r_2 + r_{C_1}\right) i_2 - v_{C_1}$$

$$\frac{di_2}{dt} = \frac{V_{g_2}}{L_2} - \frac{\left(r_2 + r_{C_1}\right)}{L_2} i_2 - \frac{v_{C_1}}{L_2}$$

$$A_3 = \begin{bmatrix} -\frac{(r_1 + a)}{L_1} & 0 & 0 & -\frac{b}{L_1} \\ 0 & -\frac{(r_2 + r_{C_1})}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{b}{C_2} & 0 & 0 & -\frac{b}{RC_2} \end{bmatrix} \quad B_1 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

$$E_3 = \begin{bmatrix} a & 0 & 0 & b \end{bmatrix} \qquad F_3 = \begin{bmatrix} 0 \end{bmatrix} \qquad P_3 = \begin{bmatrix} 0 & 1 & 0 & 0 \end{bmatrix}$$

**Conclusion:**

In this thesis, TSFOI dc-dc converter state-space modeling aspects are discussed. The transfer function matrix of TSFOI converter is derived for each mode of operation.

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