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Design and Implementation of Digitally Controlled Cooler Drive Inverter for Temperature Control

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Abstract : Cooler drives are widely used for cryocoolers, a cryocooler is a refrigerator designed to reach cryogenic temperatures and its main purpose is to cool objects quickly using extremely low temperatures. The main objective is to capture the image from the Space and fed to the FPGA and the signal received is converted to Digital form using Analog to Digital converter (ADC). The proposed inverter drives the cooler drive with 12V/6.5A, 50Hz AC output power via a PID control loop with input voltage range from 24V to 42.5V DC to control the cooling of detector array based upon the temperature signal feedback from the temperature sensor mounted on detector Focal Plane Array. Efficiency of more than 90% is achieved for different range of input DC Voltage and in order to increase the relative accuracy of the thermal sensor, it is supplied with 1mA, 25uA constant current source to bias a temperature sensing diode and is connected to cooler PID control loop for temperature regulation. The voltage measured across the sensing diode is used by the control algorithm in the inverter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature.

Keywords : ATmegaS128 Microcontroller, H-Bridge Inverter, 2N2222A Transistor, ADC, Sine PWM, PID Controller.

I. INTRODUCTION

Power supply unit is an interface between power source and the electric load. The main function of the power supply unit is to modulate or convert the available electrical energy from the power supply into the form required by the load. It is quite rare that the power source directly matches the requirements of a particular load [1]. So, the power supply units find extensive applications in various industries. Input power source may be AC or DC, while the load may be a motor, an electronic equipment, or a computer [8-10]. Since the Input to the cooler drives are AC, H-Bridge inverters are commonly used to convert DC Power into AC power and In order to generate sinusoidal PWM pulses for the single phase H-Bridge inverter, ATmegaS128 Microcontroller is used because it is simpler and more flexible to change the real-time control algorithms without further modification in a hardware with its reduced cost and also it reduces the complexity of the control circuit[1-2].

Cooler drive Inverter is designed to meet demand for the low-cost cooling options for local plane on very short duration. The output is controlled using Duty cycle of the PID Controller and accordingly the PWM waveforms are generated for controlling the output voltage. These applications place high demand on both cooler operating conditions and on the thermal control of the cooler environment because of the extreme temperature variation and because of limited available power. The converter uses Feed forward topology for fast response of closed loop control with changes in the input voltage and Feedback technique is implemented for regulating both output voltage and temperature sensor voltage . Analog to Digital converter is used to convert analog signals to digital signals. The Switching frequency of 22KHz is used to reduce the size of the converter. The converter is provided with two relays i.e., Main relay for Turning the converter ON-OFF and Launch lock relay is used to avoid the mechanical vibrations and secure moving

during launching. The converter is provided with protection circuits such as Over Voltage Protection (OVP), Under Voltage Protection (UVP) and Over Current Protection (OCP).

1.1 ATmegaS128 MICRO CONTROLLER

In microcontroller-based design, ATmegaS128 is operated at 8MHz frequency. It has Internal 10-bit ADC and pre-scalar. So maximum ADC sampling clock is 50KHz to 200KHz, so it supports maximum resolution of 15KSPS only and the features of ATmegaS128 microcontroller are as follows

- Advanced RISC architecture /Up to 8MIPS
- 3V-3.6V / 0 - 8MHz operating voltages & speed grades
- Two 8-bit and two 16-bit timers/counters
- 6 PWM channels
- 8-channel, 10-bit ADC
- TWI/USARTs/SPI serial interface
- Programmable watchdog timer
- On-chip analog comparator
- 128 Kbytes of Flash program memory
- 4 Kbytes EEPROM – 4 Kbytes internal SRAM
- Up to 64 Kbytes optional external memory space.
- SPI interface for in-system Programming (ISP).

II. VOLTAGE FEED FORWARD CONTROL

Block diagram of voltage feed forward control is as shown in Fig - 1 . In this method instead of fixed slope saw tooth ramp, a ramp whose slope varies in proportion to the input voltage variation is used at the PWM modulator input[8-10]. The input voltage is first sensed and attenuated using the voltage divider constituted of resistors R_1 and R_2. It is then inverted before being brought to the input of the integrator. Integrator is reset at the starting of each cycle by an external fixed frequency clock signal. Since in this control technique the slope of the ramp is proportional to the input voltage, and the output voltage of the error amplifier is compared with this ramp to generate duty cycle. Any change in the input voltage causes immediate change in the duty cycle even if the bandwidth of voltage loop is very low.

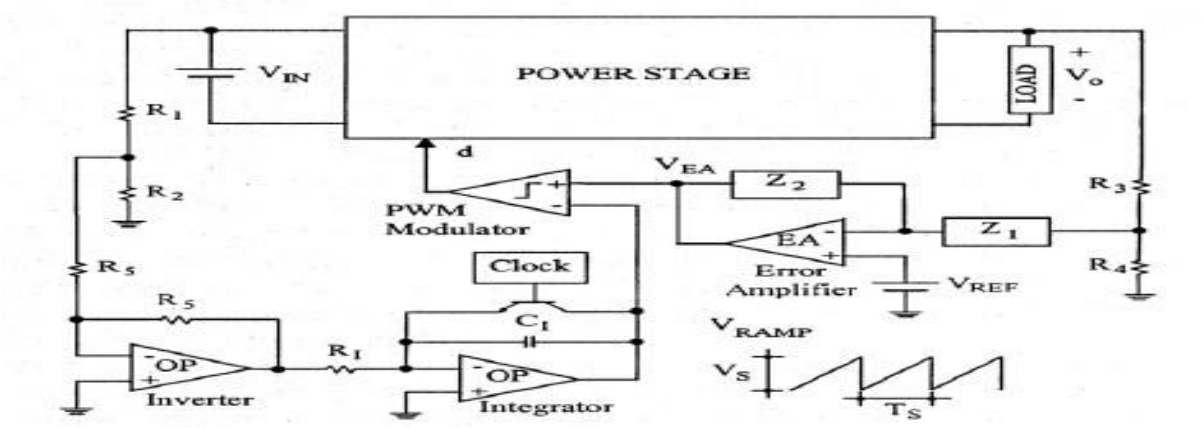

Fig – 1 : Block diagram of voltage feed forward control.

After the input voltage is increased, at $t=T_o$, the slope of the ramp increases causing the duty cycle to reduce immediately so as to maintain the output voltage constant as shown in Fig-2. Because of this instantaneous change in duty cycle, output voltage overshoot caused because of the input step change is decreased. Any increase in input causes the decrease in duty cycle. Thus good line regulation is achieved.

The operation of the feed forward scheme is described by following equations.

$$Vs = \left(\frac{V_{in}}{K}\right) \quad \text{.....(2.1)}$$

$$D = \left(\frac{T_{on}}{T}\right) = \left(\frac{V_c}{V_s}\right) = \left(\frac{KV_c}{V_{in}}\right) \quad \text{.....(2.2)}$$

Where,

D: Duty ratio

K: constant

V_{in}: Input voltage

V_s: Peak-Peak Saw tooth Voltage

V_c: Control Voltage

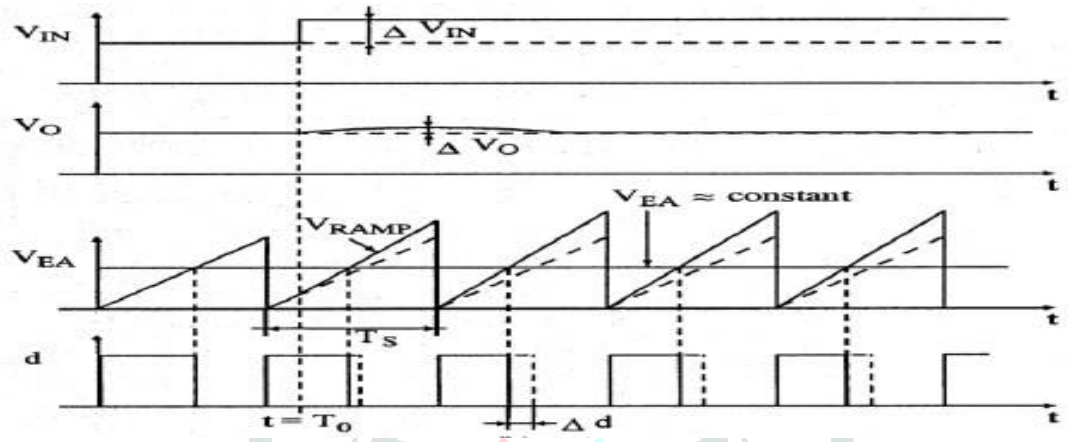

Fig-2 : Key waveforms during step change in V_{in} for voltage mode feed forward control.

III. FUNCTIONAL BLOCK DIAGRAM AND METHODOLOGY

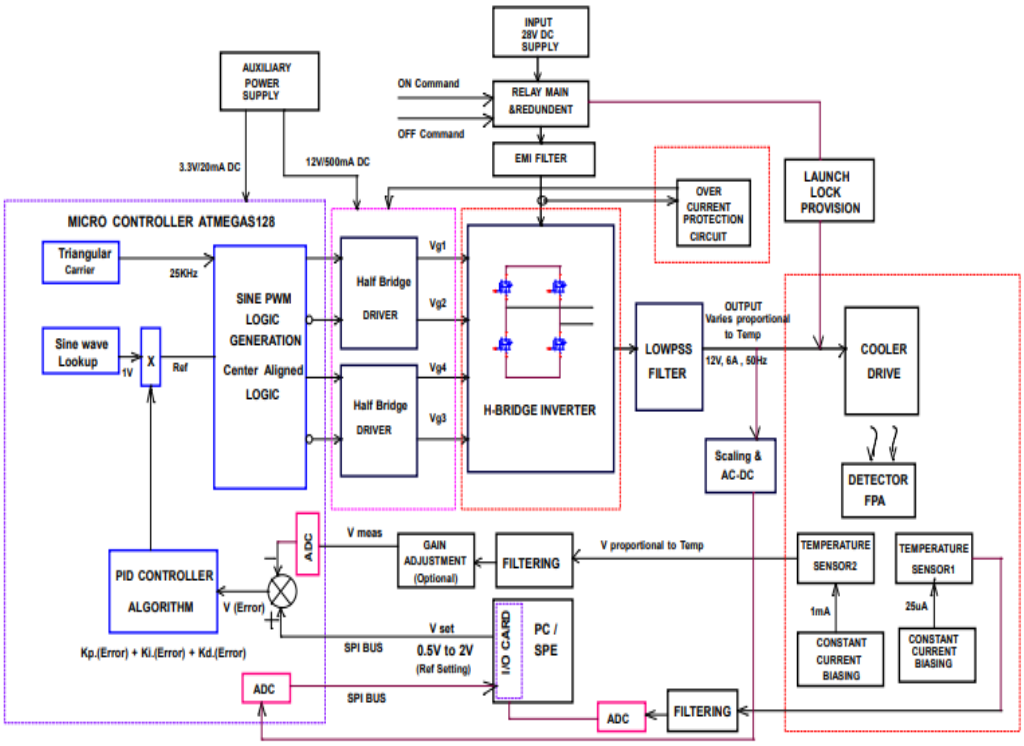

Fig-3 : Functional Block Diagram of the Cooler Drive Inverter

Functional block diagram of the proposed prototype is as shown in Fig-3. The Hardware Prototype interfaces with the cooler by supplying it with an AC voltage. It takes 28V DC as input power supply. The prototype basically generates AC power via a PID control loop to control the cooling on detector array based upon the input from the temperature sensor mounted on detector Focal Plane Array(FPA). Three Latch Type relays(ON/OFF type Relays) are used namely, Relay main, Relay redundant and launch lock relay and their commands are controlled via the Relay command input connector.

Since the input current will be fluctuating , The EMI/EMC filters are used at the input stage to filter out the fluctuations in the input current. The filtered DC input is given to the H-bridge inverter. The ATmegaS128 microcontroller output signal drives an H-bridge, pulse-width modulated (PWM) output stage. Since the output from the H-bridge inverter is sinusoidally variable pulses and to minimize the amount of generated EMI, sufficient output filtering has been used and finally it is given to the output low pass filter to get pure sinusoidal pulses and finally is given to the cooler drive(Pure noise free AC power).

The RMS output voltage is determined by the temperature control loop. Feedback for the control loop is provided by the temperature signal. The converter (DC-AC) has been equipped with a separate 1mA and 25uA constant current source to bias a temperature sensing diode . In order to increase the relative accuracy of the thermal sensor, it is supplied with 1mA, 25uA and is connected to cooler PID control loop.

Temperature sensor is a Base/Emitter silicon junction of a transistor 2N2222A .The voltage measured across the sensing diode is used by the control algorithm in the converter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature. The temperature stability is strongly dependent on the correct measurement of the diode sensor voltage. The value for the diode set-point voltage should be programmed in the converter by means of a software setting.

This voltage “set-point” should be able to be adjusted within a range of 0.5 to 2 Volts. During a cool down, the maximum RMS voltage can be limited depending on the ambient temperature, time after restart or the actual cold tip temperature. The maximum output voltage as well as the limitation criteria are programmed in the converter and can be adjusted according to cooler and system parameters.

IV. SPECIFICATIONS AND DESIGN DETAILS

4.1 SPECIFICATIONS

Table 1 shows the specifications of the Cooler Drive Inverter using ATmegaS128 Micro Controller.

Table 1 : Specifications for the proposed prototype

Sl.no	Parameter	Specifications
1	Input Voltage Range	24V - 42.5V DC
2	Nominal Input Voltage	28V DC
3	Nominal Output Voltage (RMS)	12V AC
4	Maximum Output Voltage (RMS)	15.7V AC
5	Maximum AC Power Output	78 W
6	Topology	H-Bridge Inverter
7	Maximum AC Output Current	6.5 A
8	Nominal Output Current	6A
9	Modulation	Sine PWM
10	Switching Frequency	22KHz
11	AC Output Power	72W
12	Output Frequency	50Hz ,+/- 1%
13	Protections	OCP, UVP and OVP
14	Controller used	ATmegaS128 Microcontroller (10MHz, 8 channel 10-bit ADC, 30k Radiation, 6 PWM channels, 53 GPIO,4KB EEPROM and 64KB External memory).
15	Efficiency (%)	> 90%
16	THD (Total Harmonic Distortion)	Less than 5%

4.2 DESIGN DETAILS

1. Input Power and Current Calculation

Maximum Output Power : $P0_{max} = \frac{V0_{MAX}^2}{RL} = 82.1633W$ at linear load nature……(4.1)

Maximum input Power : $Pin_{max} = \frac{P0_{max}}{\eta} = 91.2926W$……(4.2)

Voltage across switch : $Vsw = Vin_{Max} = 36V$……(4.3)

Peak Switch Current : $Ip = \frac{Vin_{max}}{RL} = 12A$……(4.4)

Average switch current : $IA_{sw} = \frac{Ip}{2} = 6A$……(4.5)

Average input current : $Is = \frac{Pin_{max}}{Vin_{max}} = 2.5359A$……(4.6)

Let Assume maximum output current is peak current for input OCP

$Is_{rms} = 6.5A$……(4.7)

2. Output Filter Design

Output filter consist of inductor and capacitor.

a. Output Inductor

The primary role of the output filter inductor (Lo) is to filter out the switching frequency harmonics. The design of an inductor, amongst other factors, depends on the calculation of the current ripple and choosing a material for the core that can tolerate the calculated current ripple.

When designing filters, the value of inductance is usually designed first. The selection of inductance is related to the ripple current and the power consumption of the system. In general, the ripple current on the inductor is selected to be 15% - 25 % of the rated current.

For this design, the rating is 75 W, the switching frequency is 20 kHz, and the bus voltage is 32 V.Assume that the ripple is 20% and is tolerable by the inductor core,and the minimum inductance required is calculated as:

$Peak\ to\ Peak\ Ripple\ Current\ is$: $\Delta IL = \frac{20}{100} * I0rms_{max} = 1.3A$……(4.8)

Hence Output Inductor Value is

$L = \frac{Vin_{max}}{4*Fsw*\Delta IL} = 3.4615 * 10^{-4}\ H$……(4.9)

b. Output Capacitor Filter

Assume $L0 = 0.5 * 10^{-3}$……(4.10)

Cutoff Frequency : $Fc = \frac{Fsw}{10} = 2000Hz$……(4.11)

$C0 = \frac{1}{4*\pi^2*L0*Fc^2} = 1.2665 * 10^{-5}F$……(4.12)

c. Output Inductor Design

Let $K = 0.3$ $Kw = 0.5$ $Bm = 0.33$ $J = 4$

Using Area Product Method

$Ap_{L0} = Lo * I0rms_{max} * I0rms_{max} * \frac{\left(1+\frac{K}{2}\right)}{Kw*Bm*J*10^{-6}} = 36808.7121$……(4.13)

Requirement of Core selection

An appropriate core will be selected which must have area product greater than the calculated Ap. Area product (Ap) is given as the product of the core cross section (Ac) and the window area (Aw). These data is avalable in ferrite magnetic core design catalog.

Selected Ferrite Toroid Core: ZW-422120,Material:R, AL: 12080mH/1000T

$Ac = 51.1\ mm^2 \quad Aw = 147.9\ mm^2 \quad AL = 12080.10 * 10^{-9} H$

$Ap = Ac * Aw \quad Ap = 7557.69\ mm^4$

Cross sectional area of wiregauge selected $Aw_{28AWG} = 0.111\ mm^2$……..……(4.14)

Number of Turns : $N = \sqrt{\frac{L0}{AL}} = 6.4336$ N=10……(4.15)

Possible number of turns possible in the core

Outer Diameter of selected wire gauge $dw_{CM} = 0.366\ mm$ For 28 AWG Wire Gauge

$Toroid_{inner_{dia_{CM}}} = 13.7\ mm$……..…(4.16)

$Possible_{turns_{for_{core}}} = \pi * \frac{Toroid_{inner_{dia_{CM}}}}{dw_{CM}} = 117.5951$……(4.17)

Required cross sectional Area of wire $Awp = \frac{I0rms_{max}}{J} = 1.625 \quad Awp = 1.625$……..…(4.18)

Number of parallel strand required $nparp = \frac{Awp}{Aw_{28AWG}} = 14.6396$: 6*28AWG……..(4.19)

3. Power Loss Calculations

Copper Loss calculations

AC resistance of wire gauge selected $Rac_{28AWG} = 0.222\ Ohm$……..……..…(4.20)

Length of wire required : $L = \frac{(22.1-13.7)+2.12*7}{1000} = 0.0338\ meter$……(4.21)

$L_N = N * L + 0.02 = 0.358\ meter$……..…(4.22)

Copper loss

$P_N = \left(L_N * Rac_{28AWG} * I0rms_{\max}^{2}\right) * \frac{1}{6} = 0.5596\ watt$……..…(4.23)

Core Loss Calculations

$a = 0.30 \quad c = 1.26 \quad d = 2.60 \quad Ve = 2.77\ cm^3$

$Bm = 0.33$

$B = \left(\frac{Bm}{2}\right) * 10 \quad B = 1.65 \quad f = \frac{Fsw}{1000} = 20$

$Pcore = a * f^c * B^d * \frac{Ve}{1000} \quad Pcore = 0.1332W$……..……(4.24)

Where: 1. Ve is core Volume
2. B is core calcated flux density
3. Pcore is the power loss in the selected core

Total Loss

$P_{L0} = 2 * (Pcore + P_N) = 1.3856\ watt$ (For 2 Inductor)……(4.25)

4. MOSFET Selection and Snubber Design

FQA70N15 , 0.028 Ohm, 70A@ 25 Deg. Vds:150V (Industrial)

$R_{DS} = 0.028\ ohm \quad R_{Gate} = 3.3\ ohm$

$Q_{GATE} = 25 * 10^{-9}C \quad V_{TH} = 6V$

$V_{GATE} = 12V \quad V_{OFF} = 2.5 * Vin_{max} = 90V$

$Coss = 1100 * 10^{-12}\ F$

$$Tr = Q_{GATE} * \frac{R_{GATE}}{V_{GATE}-V_{TH}} = 1.375 * 10^{-8}\text{sec} \quad \text{(4.26)}$$

$$Tf = Q_{GATE} * \frac{R_{GATE}}{V_{TH}} = 1.375 * 10^{-8}\ sec \quad \text{(4.27)}$$

$$P_{CONDUCTION} = 1.25 * R_{DS} * IS_{rms}^2 = 1.4788\ Watt \quad \text{(4.28)}$$

.

$$P_{GATE} = Q_{GATE} * V_{GATE} * Fsw = 0.006\ Watt \quad \text{(4.29)}$$

$$P_{Coss} = Coss * V_{OFF}^2 * \frac{Fsw}{2} = 0.0891\ Watt \quad \text{(4.30)}$$

$$P_{Switching_{ON}} = Vin_{min} * Is_{rms} * (Tr) * \frac{(Fsw)}{3} = 0.0143\ Watt \quad \text{(4.31)}$$

$$P_{Switching_{OFF}} = V_{OFF} * IS_{rms} * (Tf) * \frac{Fsw}{3} = 0.0536\ Watt \quad \text{(4.32)}$$

MOSFET Gate Charge loss takes place in Gate Resistor and this loss is not added in the MOSFET power losses.

RC snubber is connected across MOSFET to reduce switching loss.

Let $Csnubber = 1 * 10^{-9}$F

$$P_{Switching_{OFF_{WITH_{SNUBBER}}}} = \left(\frac{Coss}{Coss+Csnubber}\right) * P_{Switching_{OFF}} = 0.0281\ Watt \quad \text{(4.33)}$$

$$P_{MOSFET_{LOSS_1}} = P_{conduction} + P_{Coss} + P_{Switching_{ON}} + P\_Switching\_OFF\_with\_Snubber \quad \text{(4.34)}$$

$$P_{MOSFET_{LOSS_1}} = 2 * P_{MOSFET_{LOSS_1}} = 3.2205\ Watt\ for\ 2\ MOSFET \quad \text{(4.35)}$$

5. Efficiency Calculations

$$P_{loss_1} = P_{MOSFET_{LOSS_1}} + P_{L0} + P_{EMI} = 5.3273\ Watt \quad \text{(4.36)}$$

$$P_{loss} = 0.2 * P_{loss_1} + P_{loss_1} = 6.3928\ Watt \quad \text{(4.37)}$$

$$P0_{max} = 82.1633\ Watt \quad \text{(4.38)}$$

$$Efficiency = \frac{P0_{max}}{(P0_{max}+P_{loss})} * 100 = 92.7811\ Watt \quad \text{(4.39)}$$

V. HARDWARE IMPLEMENTATION RESULTS AND DISCUSSION

5.1 Hardware Results of output voltage

Table-2 Shows the hardware implemented results of output voltages of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-2 : OUTPUT VOLTAGES (VRMS)

VIN (V)	OUTPUT VOLTAGES (VRMS)		
	(12-15.7 VRMS) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	10.56	10.54	10.66
28	10.74	10.83	10.90
32	10.94	10.77	10.97
36	11.43	11.48	11.59

5.2 Hardware Results of load regulation

Table-3 Shows the hardware implemented results of load regulation of cooler drive inverter at 2.5ohm and 3.5ohm resistive load.

Table-3 : LOAD REGULATION

VIN (V)	LOAD REGULATION % for 2.5 Ohm resistor	LOAD REGULATION % for 3.5 Ohm resistor
24	0.61	-1.37
28	0.23	-1.47
32	0.35	-3.13
36	-0.96	-3.49

5.3 Hardware Results of Line regulation

Table-4 Shows the hardware implemented results of line regulation of cooler drive inverter for 28VDC input voltage.

Table-4 : LINE REGULATION

VIN (V)	LINE REGULATION % for 28VDC input voltage
24	4.02
32	-1.20
36	-6.34

5.4 Hardware Results of Frequency

Table-5 Shows the hardware implemented results of Frequency of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-5 : Frequency

VIN (V)	Frequency(Hz)		
	12VRMS (49.5 - 50.5) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	12VRMS (49.5 - 50.5) at 3.5 Ohm load
24	51.79	51.73	51.72
28	51.82	51.75	51.69
32	51.66	51.69	51.75
36	51.88	51.74	51.83

5.5 Hardware Results of DC offset

Table-6 Shows the hardware implemented results of DC offset(V) of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-6 : DC offset

VIN (V)	DC offset (V)		
	12VRMS at 3.0 Ohm load(< 0.2V)	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	0.095	0.100	0.100
28	0.100	0.100	0.100
32	0.100	0.100	0.100
36	0.100	0.100	0.100

5.6 Hardware Results of THD

Table-7 Shows the hardware implemented results of Total Harmonic Distortion(THD) of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-7 : Total Harmonic Distortion(THD)

VIN(V)	Total Harmonic Distortion(THD) %					
	12VRMS at 3.0 Ohm load		12VRMS at 2.5 Ohm load		12VRMS at 3.5 Ohm load	
	Secondary harmonics	Higher Harmonics	Secondary harmonics	Higher Harmonics	Secondary harmonics	Higher Harmonics
	<10%	<5%	<10%	<5%	<10%	<5%
28	0.425	3.250	0.32	3.510	0.19	3.450

5.7 Hardware Results of Efficiency

Table-8 Shows the hardware implemented results of efficiency of cooler drive inverter.

Table-8 : Efficiency

VIN (V)	Input current (A)	Input power (W)	Output Voltage (Vrms)	Output current (Irms)	Output power (W)	Efficiency (%) > 90% 60W
24	1.674	40.18	10.91	3.40	37.05	92.22
28	1.570	43.96	11.36	3.72	42.27	96.15
32	1.419	45.41	11.50	3.75	43.08	94.86
36	1.419	51.10	12.08	3.94	47.56	93.07

5.8 Hardware Results of Efficiency at 60W Load Condition

Table-9 Shows the hardware implemented results of efficiency of cooler drive inverter at 60W load condition

Table-9 : Efficiency@60W Load condition

At 60W Load Condition						
VIN (V)	Input current (A)	Input power (W)	Output Voltage Vrms	Output current Irms	Output power (W)	Efficiency (%) > 90% 60W load condition
24	2.72	65.28	10.54	5.83	61.46	94.14
28	2.30	64.40	11.03	5.51	60.70	94.26
32	2.00	64.00	11.28	5.37	60.53	94.57
36	1.81	65.16	12.46	5.02	62.57	96.03

5.9 Hardware Results of Ripple Voltage

Table-10 Shows the hardware implemented results of ripple voltage of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-10 : Vripple

VIN (V)	Vripple		
	(12-15.7 VRMS) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	1.30	1.30	1.20
28	1.30	1.20	1.20
32	1.80	1.30	1.50
36	1.70	1.50	1.60

5.10 Hardware CRO waveforms of cooler drive inverter

Fig-4 and Fig-5 Shows the Hardware CRO waveforms of output voltage, output current and Temperature sensor voltage at 28VDC for motor load.
Test method: Measured by dipping Temperature sensor in Liquid Nitrogen Cylinder.

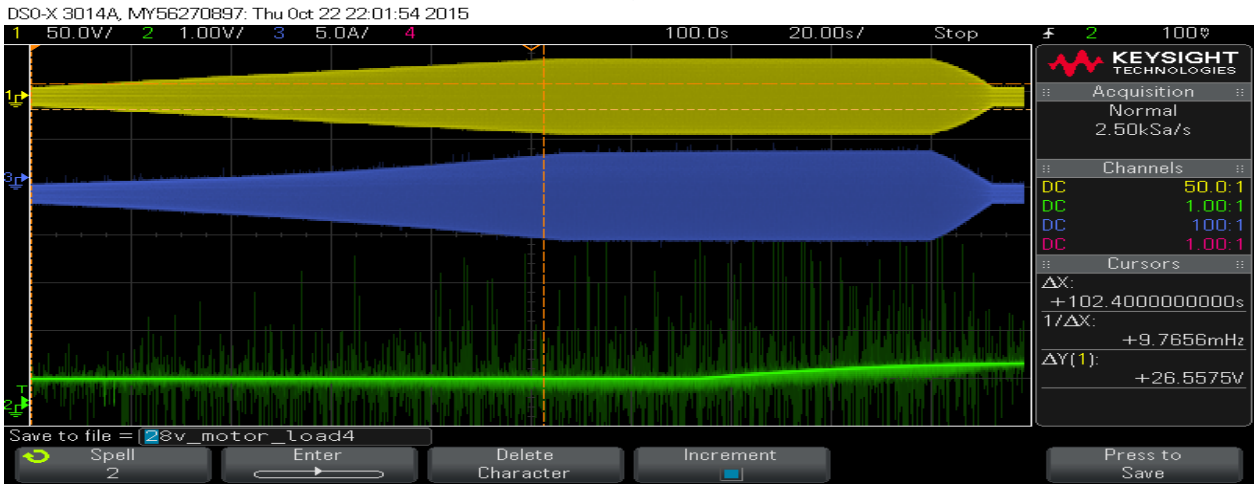

Fig-4 : Output voltage : Yellow, output current : Blue and Temperature sensor : Green at 28VDC for Motor load

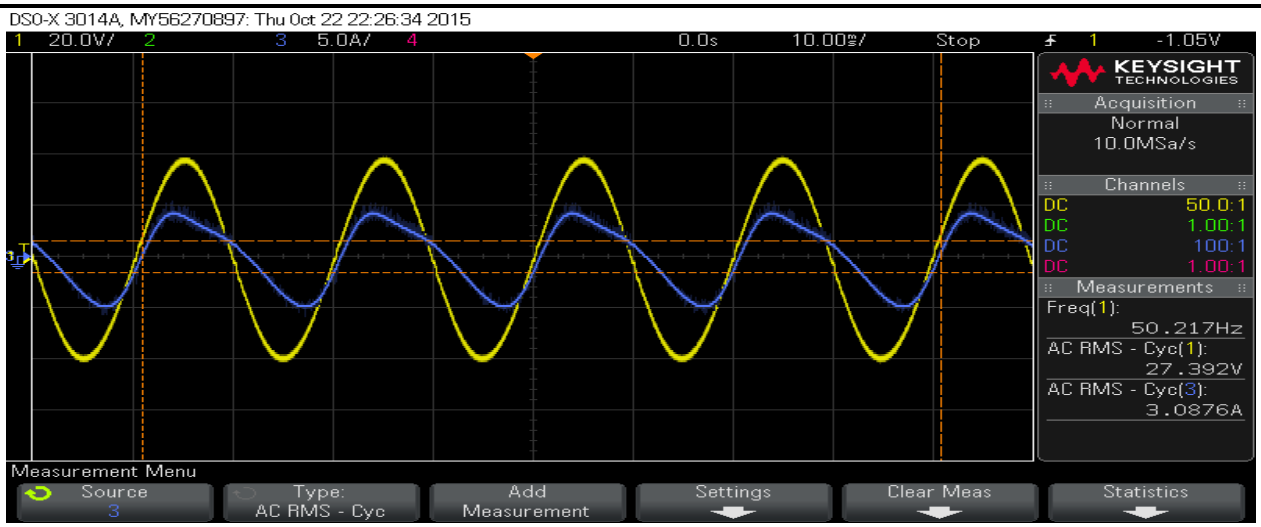

Fig-5 : Output voltage : Yellow and output current : Blue for Motor load

Fig-6 Shows the Hardware CRO waveforms of output voltage, output current and Temperature sensor voltage at 28VDC for 3-ohm Resistive load condition, here The temperature sensor voltage channel was set at high resolution mode to observe the waveform clearly.

Test method: Measured by dipping Temperature sensor in Liquid Nitrogen Cylinder.

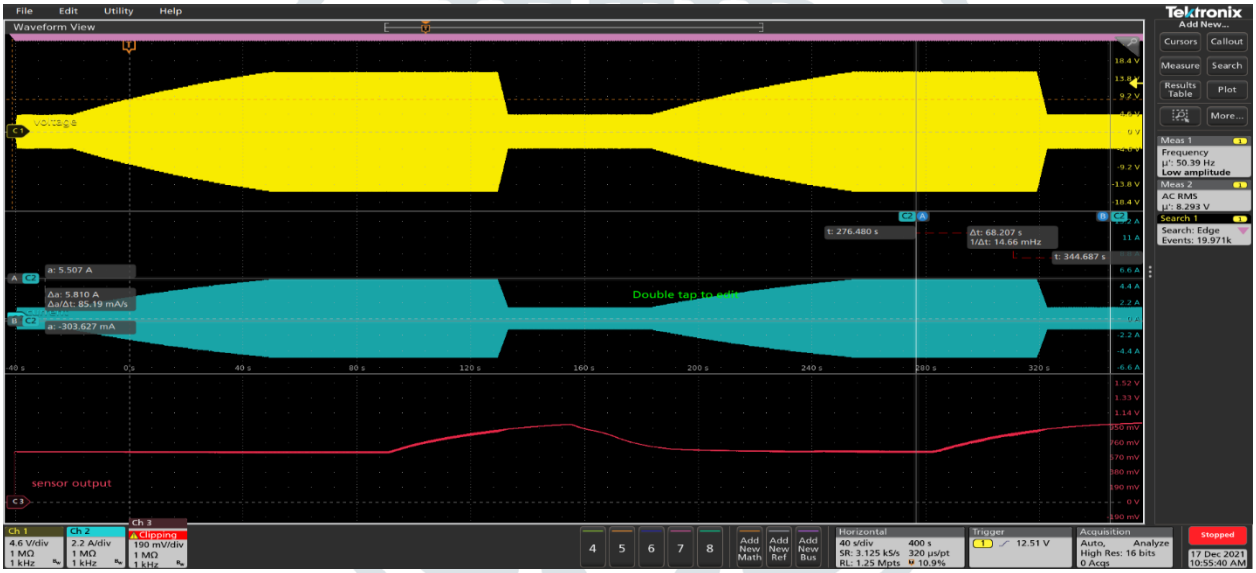

Fig-6 : Output voltage : Yellow, output current : Blue and Temperature sensor : Red at 28VDC for 3-ohm resistive load condition

5.11 Hardware Experimental Setup of Cooler Drive Inverter

Fig-7 Shows the hardware experimental Setup of Cooler Drive Inverter.

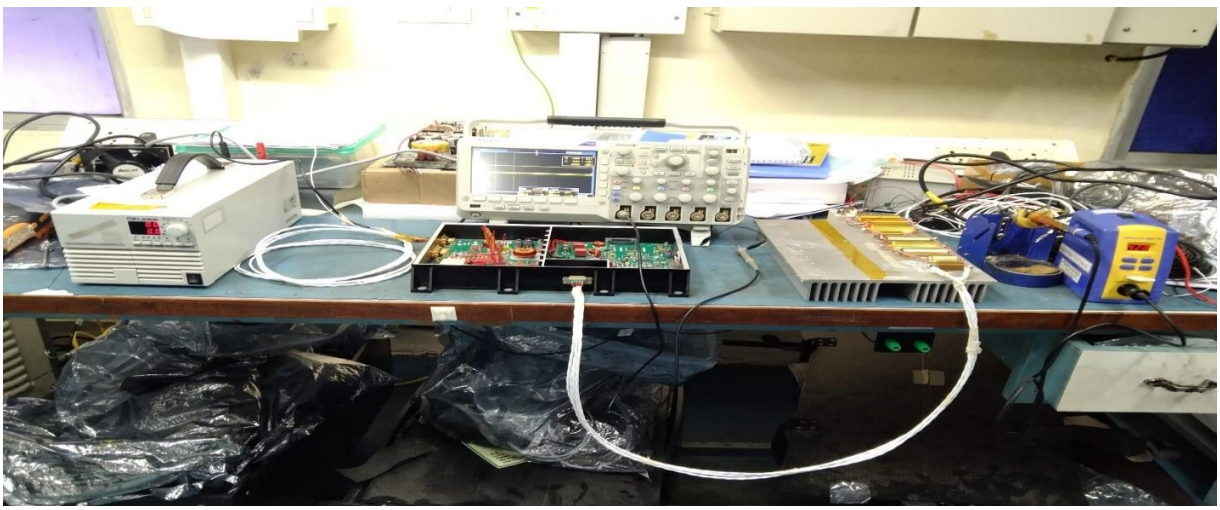

Fig-7 : Hardware Experimental Setup

VI CONCLUSION

Digitally controlled cooler drive inverter with feed-forward control for space application has been designed. The selected topology was H-Bridge inverter. The Main components include ATmegaS128 Micro controller, PID Controller, Protection Circuits, MOSFET Switches, Analog to Digital Converter, Driver Circuit, 2N2222A Transistor and Relays. The Hardware Implementation results shows that the output voltage obtained was 12V and the output current obtained was 6.5A. The obtained efficiency was more than 90% and obtained output ripple, Frequency, DC offset, Total Harmonic Distortion, Load and Line regulation was within the specified limits.

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