Performance and Analysis of Low Power D-type Flip Flop using Power Gating Techniques

Ashish Aman
Department- EC (VLSI)
Shriram College Of Engineering & Management,
Banmore
Gwalior, India
ashish.aman167@gmail.com

Prof. Abhishek Shrivastava
Assistant Professor
EC Department, SRCEM College, Banmore
Gwalior, India
abhishek.amor07@gmail.com

Abstract: Flip-flops are frequently employed in low power VLSI systems to receive and maintain data in specific sequences throughout recurring clock intervals for a brief amount of time necessary for other circuits in a system. In this paper leakage current and leakage power of conventional D-type CMOS flip-flop at 90nm technology has been estimated and circuit systems to decrease Leakage in deep sub-micron such as Sizing of the transistor and Power Gating have been discussed and applied to conventional D-type CMOS flip-flop. By the sizing of the transistors in the D-type CMOS flip-flop, an optimized D-type CMOS flip-flop is obtained and evaluated, and established to be more efficient than the conventional D-type CMOS flip-flop. Then, Power Gating is used on the improved D-type CMOS flip-flop, and it is discovered to be the fastest and most efficient in terms of leakage power and leakage current. The verification results demonstrate that our enhancement, as compared to Power Gating flip-flops, significantly lowers energy consumption at low data switching activity while maintaining tolerable space and setup time costs. Using the Cadence tool at 90nm technology, the proposed design, and the existing design are both simulated.

Key Words: *Leakage Current, D-Flip Flop, Leakage Power, Power Gate Cadence, Delay, CMOS.*

I. Introduction

The performance of digital systems has significantly increased as a result of process improvement, and power consumption is now one of the main constraints on their use. Additionally, IoT devices are widely used due to the Internet of Things (IoT) rapid development [1]. Low-power design is prioritised in these batteries- or self-powered gadgets. [2]–[5]. Flip-flops (FFs) are fundamental devices whose power makes up a significant portion of the digital system's power [6], [7]. This means that digital systems' energy consumption can be greatly reduced by decreasing FFs' power requirements.

Flip-flops, or bi-stable devices, are essentially utilised as one-bit memory cells. logic 0 or logic 1 are the only two stable states for a flip flop. [8] achieve one of two possible stable states for the flip flop, we must provide it with an external pulse as input. Until another pulse is used to alter that state, the output stays in that stable condition. By using appropriate inputs other than the trigger, we can additionally change the flip-flop output. A common feature of most sequential circuits, such as shift registers, counters, and other devices is the employment of flip flops. pause flip flop [9] Applied to its D input is whatever is stored in the input bit pattern. This functionality helps other digital circuit components process data bit-by-bit to find solutions for difficult functions. The positive edge-triggered D type flip flop's gate level diagram is shown in Figure 1. The fundamental drawback of the Set Reset flip-flop is overcome by a D flip-flop (namely, its unanticipated results and timing S=R=1). "delay flip-flop" or "data flip-flop" refers to the ability of the D flip-flop in Fig.1 to "latch" and store data, which enables a circuit to postpone processing data.
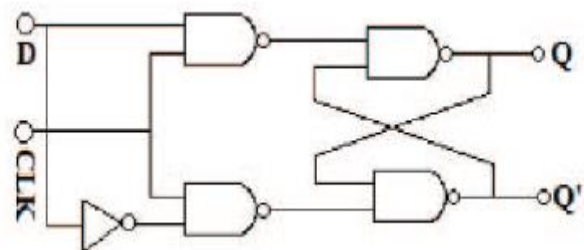

Fig.1 Flip flop of the D-type gate level diagram

To avoid the S=R=1 input combination (which results in confusing output), in order to create a D-type flip flop, an SR type and an inverter are used [10]. This modification prevents the SR flip-indeterminate flop and non-allowed states. By using only one D input while a clock pulse is present, data from the S and R inputs are simply delayed until a later time.

Short-circuit power dissipation, static power dissipation, and dynamic power dissipation are the three major types of power dissipation. Technology advancements have led to an increase in the amount of electricity that is being wasted due to inefficiencies like leakage. It's a difficult design restriction even with the most advanced flip-flops because they tend to only swap states on rising edges of the clock signal and remain constant at all other times during the clock period. Ultrathin devices [11], silicon on insulator (FDSOI) devices [12], and fin-type field-effect transistors (FINFET) devices [13] have all been presented as revolutionary multigate devices that could solve this problem. FINFET appears to be the most viable alternative at this moment for its exceptional electrical and timing qualities. In the past few years, Intel, TSMC, and other multinational foundries have created commercial chips based on FINFETs.

II.   CMOS D-Flip flop Architecture

For computers and a broad variety of other systems, flip-flops are an essential component in digital electronics. Flip flops are employed to store state information in electronic equipment. The output of a D flip-flop can be connected to the input in order to have it operate in the opposite direction. The data line's value is stored in the data field denoted by the letter "D". Flip-flop electronic circuits respond to a clocking pulse simply by keeping an input signal's logic state unchanged. An inverter circuit can be used to set or reset this D flip-flop. Double Edge triggered (DET) and Single edge triggered (SET) are the two varieties of flip-flops that can be used. The SET flip-flop is simple and uncomplicated since it may be configured to function on a clock's ascending or descending limb. A TSPC D flip-flop with five transistors is shown in the diagram below. Figure 2 shows the schematic for a 5-transistor TSPC D flip-flop. It was possible to build this flip-flop utilising three NMOS and two PMOS transistors. This edge-triggered flip-flop has a small footprint and consumes less energy because it employs only five transistors. Clocking logic was called True Single-Phase Clocked Logic in the 5T D Flip Flop. The TSPC circuit technique enhances the performance of a digital system by selecting a single clock phase and eliminating skew concerns. This reduction in skew results in large savings in chip space and power usage [3] Diagram of 5T TSPC D Flip Flop is shown in Figure 2, below. [14, 15]

To increase output, the transistors P1 and N3 are switched off when CLK and input D are high, while the remaining transistors P2, N1, and N2 are turned on. During the ON clock period, the output corresponds to whatever value the input has. Fig. 3 and 4 depict the transient response and leakage current, respectively, of the CMOS D-Flip Flop.
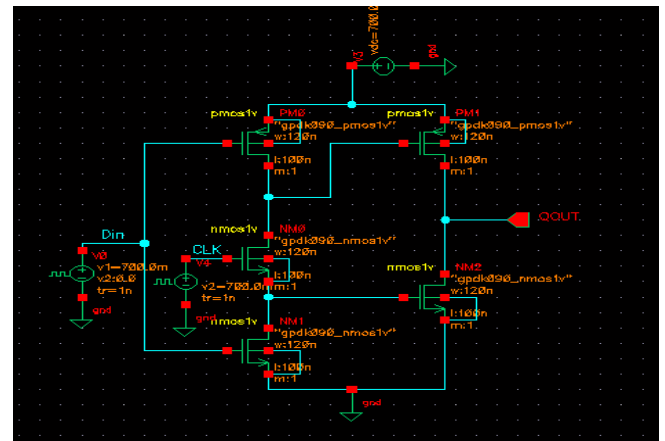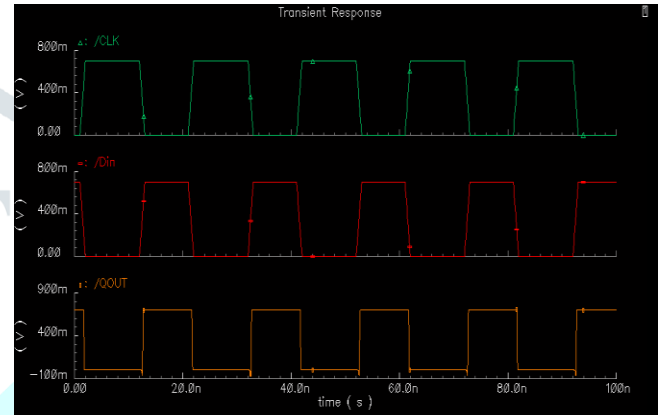

Fig.2 A D-Flip Flop on the CMOS Sensor

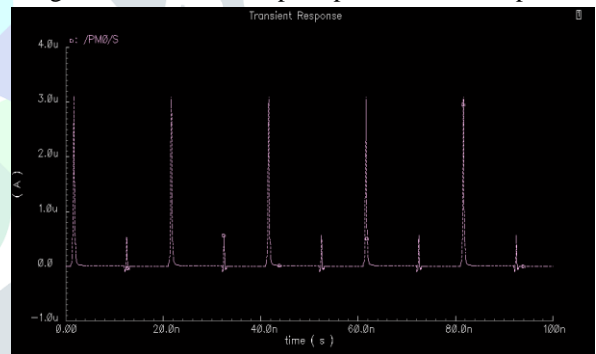Fig.3 The CMOS D-Flip Flop's Transient Response

Fig.4 Leakage Current of CMOS D-Flip Flop

III.   POWER GATING

When the D-type CMOS flip-flop is not in use, a control mechanism cuts off the supply voltage (VDD), preventing leakage current. This greatly minimises the power dissipation of the leakage current. One high voltage transistor is inserted into the supply or ground route of the D-type CMOS flip-flop, and all other low voltage (Low Vt) transistors are simulated. Compared to High Vt transistors, Low Vt transistors have a faster switching speed. Therefore, the D-type CMOS flip-flop functions rapidly. Power usage and latency are both reduced by this arrangement.

D-type gated VDD CMOS flip-flop is depicted in Figure 2. Using the "Gated VDD Control" signal, the D-type CMOS flip-flop is turned on and off. Consequently, this technology is referred to as "Gated". Because of this technology, system performance may be maintained even when supply voltages

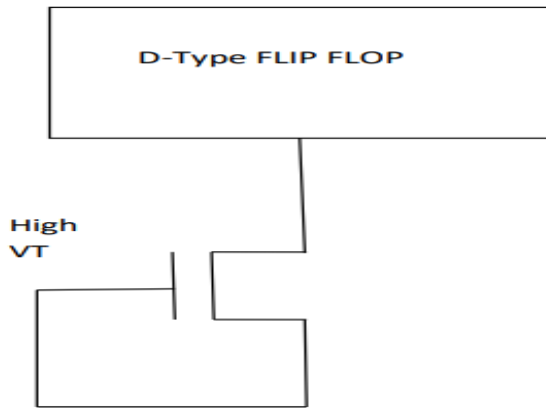and transistor thresholds are reduced, which is the key benefit.

Fig.6 D-type CMOS flip-flop using Power Gating Technique

Figure 5 shows a Gated VDD D-type CMOS flip-flop

IV.   Power Gating Techniques Applied On D-type CMOS flip-flop

For approaches like Gated VDD and MTCMOS that use power gating, shutting off the sleep transistors is necessary in order to create virtual power rails (virtual VDD and ground). Data bits "1" (VDD) and "0" (ground) are always indicative of the presence on both sides of the D-type CMOS flip-flop due to the cross-coupled inverters. This D flip-flop can be set or reset with the assistance of an inverter circuit. Flip flops can be classified as either SET or DET depending on how the edges are activated. The SET flip flop is a basic and straightforward device to construct since it may function on either the rising or falling clock edge. The data bits '1' and '0' on either side of the D-type CMOS flip-flop charge the virtual power rails with the inverters pass transistors after turning off the sleep transistors. VDD will always be lower in voltage than these virtual power rails, they will only be adequate for supporting the cell with more data and will be insufficient for carrying out any operations. There is a progressive dissipation in the sleep mode of the virtual VDD, nevertheless. This issue can be resolved by activating the sleep transistors before the specified time has passed. This prevents data loss by restoring the cell's true VDD and ground. The clock pulse frequency that regulates the sleep transistors must therefore be carefully selected by the designer. It is possible to design a system that automatically sends the clock signal to sleep transistors if an alternative exists. Figure 6 shows a D-type CMOS flip-flop circuit with power gating. As shown in Figures 7 and 8, the transient response and leakage current of the CMOS D-flip-flop are displayed.
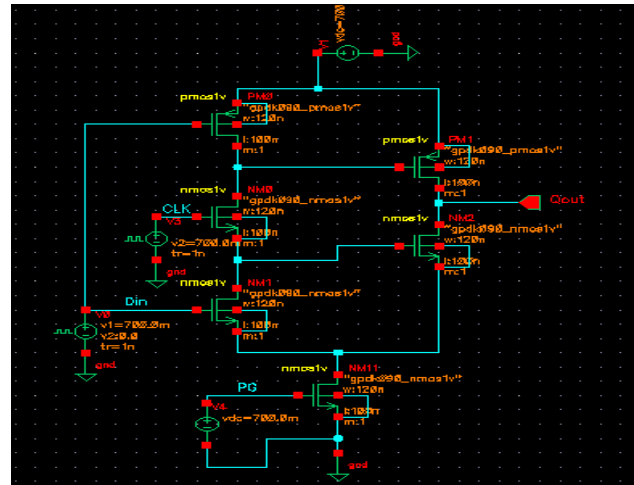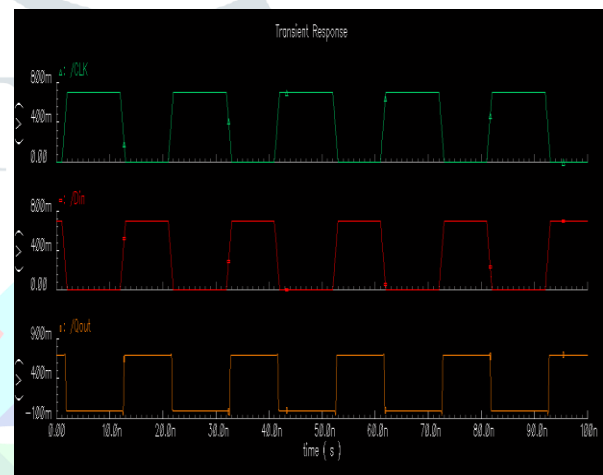

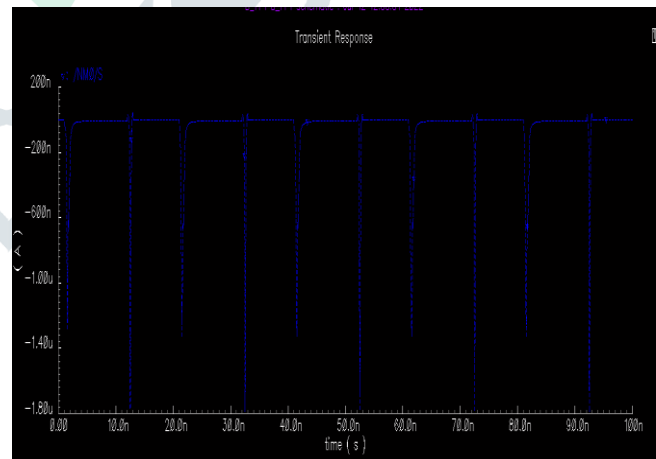Fig.7 CMOS Flip-Flop Transient Response Using Power Gating

Fig.8 CMOS Flip-Flop D-Type Leakage Current Using Power Gating

Simulation Result

In this section, extensive simulations were utilised to investigate the modified D-type CMOS flip-power flop's dissipation and operating speed for further testing and demonstration. When using the cadence tool, the minimum supply voltage for the D type Flip Flop was set to 0.75 V and the 90nm or 45nm technology was used. D-type CMOS flip-flops' look has been preserved but power consumption has been reduced using the Power Gating Technique (PGT). It increases parameters such as Leakage Current, Leakage Power, and Propagation Delay. At 27°C, the only dominant mechanism is gate leakage.

Below the table is a comparison result summary of the power gating technique used on D-type CMOS flip flops based on supply voltage

Table 1 Summary of simulated results

Performance Parameter	D type – CMOS Flip Flop	D type – CMOS Flip Flop with SVL	D type – CMOS Flip Flop with Adapted SVL	D type – CMOS using Power Gating
Supply Voltage	0.7V	0.7V	0.7V	0.7V
Technology Used	90nm	90nm	90nm	90nm
Leakage Power	4.6µW	4.4nW	2.3nW	1.5nW
Leakage Current	3.8µA	2.4nA	1.8nA	2.3nA
Propagation Delay	20µs	86ns	68ns	54ns

Conclusion

Circuit techniques to reduce Leakage in deep sub-micron such as Power Gating has been discussed and applied on conventional D-type CMOS flip-flop for leakage power and Leakage Current reduction and compared with D-type CMOS flip-flop and their circuit speed enhances. Out of all the techniques discussed optimized Power Gating has been found to be the best as it reduces more leakage comparable to Power Gating. It has been found that in conventional D-type CMOS flip-flops utmost reduction in leakage power and leakage current can be achieved using circuit techniques to reduce Leakage in deep sub-micron. Power Gating leakage reduction technique shows large reduction but due to some restrictions in the adapted SVL technique D-type CMOS flip-flop optimized Flip flop circuit by allowing for the other parameters also.

References

1. L. Atzori, A. Iera, and G. Morabito, "The Internet of Things: A survey," *Comput. Netw.*, vol. 54, no. 15, pp. 2787–2805, Oct. 2010.
2. T. Tekeste, H. Saleh, B. Mohammad, A. Khandoker, and M. Ismail, "A nano-watt ECG feature extraction engine in 65-nm technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 8, pp. 1099–1103, Aug. 2018.
3. T. Tekeste, H. Saleh, B. Mohammad, and M. Ismail, "Ultra-low power QRS detection and ECG compression architecture for IoT healthcare devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 669–679, Feb. 2019.
4. A. Pullini, D. Rossi, I. Loi, G. Tagliavini, and L. Benini, "Mr. Wolf: An energy-precision scalable parallel ultra low power SoC for IoT edge processing," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1970–1981, Jul. 2019.
5. J. P. Cerqueira, T. J. Repetti, Y. Pu, S. Priyadarshi, M. A. Kim, and M. Seok, "Catena: A near-threshold, sub-0.4-mW, 16-core programmable spatial array accelerator for the ultralow-power mobile and embedded Internet of Things," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2270–2284, Aug. 2020.
6. J. L. Shin *et al.*, "The next generation 64b SPARC core in a T4 SoC processor," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 82–90, Jan. 2013.
7. L. Moreau, R. Dekimpe, and D. Bol, "A 0.4 V 0.5fJ/cycle TSPC flipflop in 65 nm LP CMOS with retention mode controlled by clockgating cells," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2019, pp. 1–4.
8. Pooja Joshi, Saurabh Khandelwal, and S. Akashe "Implementation of Low power Flip Flop Design in Nanometer Regime" 2015 fifth International Conference on Advanced Computing and Communication Technologies.
9. Vladmir Stojanovic, Raminder Bajwa and Vojin G. Oklobdzija , "A Unified Approach in the Analysis of Latches and Flip-Flops for Low-Power Systems", ISPLED'98, August 10-12, 1998.
10. S.A Lakhotiya and R.V. Tambat, "Design of Flip- Flops for High Performance VLSI Applications using Deep Submicron CMOS Technology", International Journal of Current Engineering and Technology, vol. 4, April 2014.
11. Bill Pontikakis, A Novel Double Edge Triggered Pulse Clocked TSPC D Flip Flop for High Performance and Low Power VLSI Design Applications. Dep't of Electrical and Computer Engineering, Concordia University, Canada, 2003.
12. Choi Y K, Asano K, Lindert N, et al. Ultra-thin body SOI MOSFET for deep-sub-tenth micron era. In: Proceedings of IEEE International Electron Devices Meeting, Washington, 1999. 919–921.

13. Kedzierski J, Nowak E, Kanarsky T, et al. Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation. In: Proceedings of IEEE International Electron Devices Meeting, San Francisco, 2002. 247–250.

14. Hisamoto D, Lee W C, Kedzierski J, et al. FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. IEEE Trans Electron Dev, 2000, 47: 2320–2325.

15. M. A. Hernandez and M. L. Aranda, ―A Clock Gated Pulse – Triggered D Flip-Flop For Low Power High Performance VLSI Synchro nous Systems,‖ Proceedings of the 6th International Caribben Confer ence on devices, circuits and systems, Mexico, Apr. 26-28, 2006.