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Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application

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Abstract: - The **multilevel inverters (MLIs) have gained lots of interest in industry and academia, as they are changing into a viable technology for numerous applications, such as renewable power conversion system and drives. For these high power and high/medium voltage applications, MLIs are widely used as one of the advanced power converter topologies. To produce high-quality output without the need for a large number of switches, development of reduced switch MLI (RS MLI) topology has been a major focus of current research. By a suitable combination of switches, the MLI produces a staircase output with low harmonic distortion. For a better understanding of the working principle, a single-phase RS MLI topology is experimentally illustrated for different level generation using both fundamental and high switching frequency techniques which will help the readers to gain the utmost knowledge for advance research. The proposed work improves the performance of coupled inductor based novel 11-level inverter with reduced number of switches. The inverter engenders the sinusoidal output voltage by the use of split inductor with minimised total harmonic distortion (THD). The voltage stress on each controlled switching devices, capacitor balancing and switching losses can be reduced. The proposed system gives better controlled output current and improved output voltage with moderate THD value. The switching devices of the system are controlled by using multicarrier sinusoidal pulse width modulation algorithm by comparing the carrier signals with sinusoidal signal. The simulation and experimental results of the proposed 11-level inverter system outputs are established using MATLAB/SIMULINK.**

Index Terms **– MLI, 11-level inverter and 9-level inverter and RS-MLI , THD Value etc.**

1. INTRODUCTION

With the increasing development of the world's power grids, topics such as energy conversion, renewable energies, new systems and their applications in different industries and the relation between them, has caused the power engineering to be one of the most important and interesting science of our time. Today we can see the development of power grids overall the world. One of the most important issues in this field is power electronics. Today the power electronics devices are made in many different types for various applications, such as rectifiers, AC-AC regulators, current- and voltage choppers, inverters, power supplies and etc. Among these, inverters are one of the most important and widely used devices.

Inverter is an electronic device which converts Direct current (DC) to Alternating current (AC). The converted AC current can be at any required voltage and frequency which will be controlled by suitable circuits and transformers. Inverters have no moving parts and are used in a wide range of tools. Typical application for power inverters include:

1. Portable devices which use AC current, produced from a set of batteries such as light or kitchen appliances or computers power supply.
2. Power generation systems such as solar panels.
3. Larger electronic systems which need a derivation of AC from DC.

From the nineteenth century through the middle of twentieth century, the process of DC to AC conversion was done using motor generator sets or rotary converters. Early inverters were a bit unreliable and they lost a significant amount of energy in conversion process. In the early twentieth century, vacuum tubes and gas filled tubes began to be used as switches in inverter circuits. The new generation of inverters loses 5% of energy with 95% of the DC current being converted to AC current, but the most important changes in inverters have to do with the quality of energy they produce. The normal AC current is in the form of a sine wave. In the conversion process of DC to AC it is desired to get the output current to be as close to a sine wave as possible to avoid interference. For this reason, since 1975 the idea of "Multi-level Inverters" is introduced. The main idea of multilevel inverters is to have a better sinusoidal voltage and current with a low harmonic distortion in the output by using switches in series.

In general inverters are used to convert the DC power supply to AC power supply. In the application point of view the multilevel inverters are used mostly. The multilevel were implemented in different topologies in respective applications. Basically the inverter should consist of power semiconductor switches and DC voltage sources.

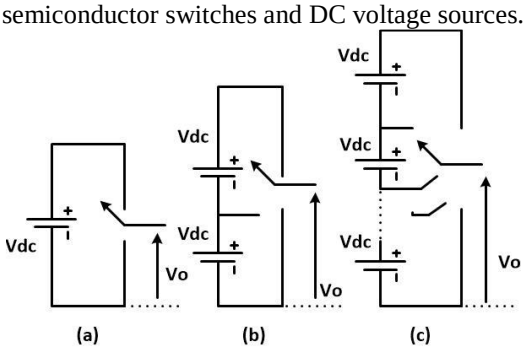


Fig. 1 Basic view of an inverter with (a) two levels (b) three levels (c) n levels

The semiconductor switches in the inverters half controlled in general. The control signals for this semiconductor switches will acquired from the relevant firing circuits. Fig. 1 shows the schematic diagram of one phase leg of inverter with different of levels in which the semiconductor device is represented by an ideal switch with several positions. In the above figure the basic view of the multilevel inverters with different number of voltage sources and voltage levels are shown briefly. From the above figure we can understand that as the number of the voltage sources is increased the number of the levels in the output voltage are also increased.

Some of the salient features of the multilevel inverters are :

- The multilevel inverters can acquire the voltage and current with low THD.
- Efficiency of the inverter depends upon the switching frequency.
- Common mode voltages are reduced and hence the stresses on the motor bearings are reduced.
- The input current drawn by them has low distortion.
- There exists no EMI problem

The organizational framework of this study divides the research work in the different sections. The Literature survey of different MLI is presented in section 2. Further, in section 3 shown Concept of Existing system is discussed and in section 4 shown the concept of 11 Level MLI, Simulation Results work is shown in section 5. Conclusion and future work are presented by last sections 6.

2. LITERATURE SURVEY

1. Y. SAHALI[1], M. K. FELLAH[2] Selective Harmonic Eliminated Pulse-Width Modulation Technique (SHE PWM) applied to Three-level Inverter / Converter [1].

The main interest of this study has been granted to the selective harmonic eliminated pulse width modulation technique, SHE PWM, for the control of single- phase and three-phase full-bridge three-level inverters. This study will be makes for any angle number (even or odd) of switches composed the inverter, for purpose of comparison with the results found for only odd number. We explain the resolution method procedure of the nonlinear equation systems in order to achieve the appropriate switching angles. The method of obtaining the best starting point is also described to overcome the problem of the choice of these points which is one of most difficult tasks associated with the SHE PWM.

2. Zhong Du, John N, Active Harmonic Elimination for Multilevel Converters [2]

This paper presents an active harmonic elimination method to eliminate any number of specific higher order harmonics of multilevel converters with equal or unequal dc voltages. First, resultant theory is applied to transcendental equations characterizing the harmonic content to eliminate low order harmonics and to determine switching angles for the fundamental frequency switching scheme and a unipolar switching scheme. Next, the residual higher order harmonics are computed and subtracted from the original voltage waveform to eliminate them. The simulation results show that the method can effectively eliminate the specific harmonics, and a low total harmonic distortion (THD) near sine wave is produced. An experimental 11-level H-bridge multilevel converter with a field programmable gate array controller is employed to implement the method. The experimental results show that the method does effectively eliminate any number of specific harmonics, and the output voltage waveform has low THD.

3. Damoun Ahmadi, Yi Huang A Universal Selective Harmonic Elimination Method for High-Power Inverters[3]

In medium-/high-power inverters, optimal pulsewidth modulation (OPWM) is often used to reduce the switching frequency and at the same time, realize selective harmonic elimination (SHE). For both two-level and multilevel inverters, most selective harmonic elimination (SHE) studies are based on solving multiple variable high-order nonlinear equations. Furthermore, for multilevel inverters, SHE has been often studied based on the assumption of balanced dc levels and single switching per level. In this paper, the authors further developed harmonics injection and equal area criteria-based four-equation method to realize OPWM for two-level inverters and multilevel inverters with unbalanced dc sources. For the cases, where only small number of voltage levels are available, weight oriented junction point distribution is utilized to enhance the performance of the four-equation method. A case study of multilevel inverter at low-modulation index is used as an example. Compared with existing methods, the proposed method does not involve complex equation groups and is much easier to be utilized in the case of large number of switching angles, or multiple switching angles per voltage level in multilevel inverters.

4. Thomas Ackermann a,*,1, Go¨ran Andersson b , Lennart So¨der a Distributed generation: a definition [4]

Distributed generation (DG) is expected to become more important in the future generation system. The current literature, however, does not use a consistent definition of DG. This paper discusses the relevant issues and aims at providing a general definition for distributed power generation in competitive electricity markets. In general, DG can be defined as electric power generation within distribution networks or on the customer side of the network.

5. Mansooreh Rene Feuillet Hamid Lesani An Approach To Deterministic And Stochastic Evaluation Of The Uncertainties In Distributed Generation Systems [5]

Distributed generations (DGs) can provide electricity to the customers at a reduced cost and higher efficiency, if the location, size, and the penetration level are correctly evaluated. To deal with the inherent uncertainties in the aforementioned three parameters, utility-operated DGs and customerowned DGs are considered as deterministic and stochastic facilities, respectively. A case study is conducted on the IEEE 30-bus system. The system is modeled with all detailed parameters using MATLAB. In this study, the proposed method incorporates Monte Carlo simulation due to its capability to handle the deterministic and stochastic problems together.

6. Ozge Pinar ARSLAN An Application Of Environmental Economic Dispatch Using Genetic Algorithm [6]

Economic load dispatch is one of the important problems in operation of power systems. It minimizes the generation cost while meeting demand and satisfying equality and inequality constraints. However, operation at minimum cost cannot be the only basis for dispatching electric load when the pollution is considered. Thermal power plants cause high concentration of pollutants.

Therefore, emissions caused by electric power plants that use fossil fuel must be considered while operating electric power systems. Environmental economic dispatch, (EED), is the problem which takes into consideration the environmental pollution and aims to reduce emissions with minimum cost. It minimizes both cost and emission together.

7. Komail Nekooei, Malihe M. Farsangi, Hossein Nezamabadi-Pour, and Kwang Y. Lee, An Improved Multi-Objective Harmony Search for Optimal Placement of DGs in Distribution Systems [7]

In this paper a new approach using Harmony Search (HS) algorithm is presented for placing Distributed Generators (DGs) in radial distribution systems. The approach is making use of a multiple objective planning framework, named an Improved Multi-objective HS (IMOHS), to evaluate the impact of DG placement and sizing for an optimal development of the distribution system. In this study, the optimum sizes and locations of DG units are found by considering the power losses and voltage profile as objective functions. The feasibility of the proposed technique is demonstrated in two distribution networks, where the qualitative comparisons are made against a well-known technique, known as Non-dominated Sorting Genetic Algorithm II (NSGA-II).

8. Samir Kouro, Pablo Lezana, Mauricio Angulo, and José Rodríguez, Multicarrier PWM With DC-Link Ripple Feed forward Compensation for Multilevel Inverters [8]

Like most power converter topologies, multilevel inverters are controlled with modulation techniques that are conceptually based on nonlinear waveform synthesis assuming constant dc-link voltages. However, real applications have load and supply dependent dc-links that usually present important low frequency ripple, which is also modulated and transmitted to the load, generating undesirable low frequency voltage and current distortion. This paper introduces a simple but effective dc-link ripple feedforward strategy into traditional carrier-based modulation techniques. The dc-link ripples are measured and used to modify the carriers or the reference directly in the modulation stage. Simulation and experimental results show the accuracy of the proposed method, eliminating low order harmonics in the load current.

9. S. Mohamed Yousuf1 , P. Vijayadeepan2 , Dr. S. Latha3 The Comparative THD Analysis of Neutral Clamped Multilevel Z-Source Inverter using Novel PWM Control Techniques [9]

A multilevel inverter is a power electronic device made to synthesize a desired AC voltage from several levels of DC voltages. These types of inverters are suitable in various high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. Multilevel inverters through a single X-shaped LC impedance network is an important development in recent years. The power quality improvement is achieved by reducing the harmonics present at the output voltage of the inverter. The total harmonics distortion (THD) values of the output voltages of the inverter are measured and compared. This paper presents the comparative analysis of several multicarrier PWM techniques, which is effectively used for harmonic mitigation in the proposed neutral clamped multilevel Z-Source inverter and this work is compared with conventional three level inverter by using MATLAB-SIMULINK.

10. R. Palanisamy[1] , V. Sinmayee[2] , K. Selvakumar[3] , K. Vijayakumar[4] Multicarrier-SPWM Based Novel 7-Level Inverter Topology with Photovoltaic System [10]

In this paper a novel 5 switch seven level DC-AC inverter is being proposed. The proposed multilevel inverter uses reduced number of switches as compared to the switches used in the conventional multilevel inverter. The inverter has been designed to generate a 7 level AC output using 5 switches. The voltage stress on each of the switches as well as the switching losses is found to be less, minimized common mode voltage (CMV) level and reduced total harmonic distortion. The proposed 7-level inverter topology has four dc sources, which is energized through the PV system. Proposed inverter is controlled with help of multicarrier sinusoidal pulse width modulation (MCSPWM).The simulation and hardware results were verified using matlab simulink and dspic microcontroller respectively.

11. R. Palanisamy*, K. Vijayakumar, Komari Nikhil, Madhumathi Iyer and Ramachandar Rao A Proposed SVM for 3-level Transformer-less Dual Inverter Scheme for Grid Connected PV System [11]

This paper elucidates on proposed SVM for grid connected system using dual inverters to get improved output voltage and better current control with less switching loss and THD. Methods/Analysis: The system incorporates PV array, MPPT and boost converter which multiplies the output of the PV array. The split inductor used in this proposed system, which evades the treatment of the conventional transformer and the stepped output is converted into sinusoidal AC output and which gives better synchronization to ac applications. Split inductor reduces the shoot through problem, leakage current problem, reduces the defeat in the scheme and reduces the expenditure of the scheme. The proposed SVM algorithm is used as PWM controller for this dual inverter. This proposed scheme is simulated using Matlab/Simulink and the experimental outcomes are verified using the dsPIC controller.

12. R. Palanisamy, Gaurav Singh, Priyanka Das, D. Selvabharathi, Sourav Sinha, Arnab Nag Design and Simulation of Novel 9-level Inverter Scheme with Reduced Switches [12]

This work recommends the performance of coupled inductor based novel 9-level inverter with reduced number of switches. The inverter which engender the sinusoidal output voltage by the use of split inductor with minimised total harmonic distortion (THD). The voltage stress on each controlled switching devices, capacitor balancing and switching losses can be reduced. The proposed system which gives better controlled output current and improved output voltage with moderate THD value. The switching devices of the system are controlled by using multicarrier sinusoidal pulse width modulation algorithm by comparing the carrier signals with sinusoidal signal.

13. Yong Shi * and Zhuoyi Xu Wide Load Range ZVS Three-level DC-DC Converter: Modular Structure, Redundancy Ability, and Reduced Filters Size[13]

In future dc distributed power systems, high performance high voltage dc-dc converters with redundancy ability are welcome. However, most existing high voltage dc-dc converters do not have redundancy ability. To solve this problem, a wide load range zero-voltage switching (ZVS) three-level (TL) dc-dc converter is proposed, which has some definitely good features. The primary switches

have reduced voltage stress, which is only Vin/2. Moreover, no extra clamping component is needed, which results simple primary structure. Redundancy ability can be obtained by both primary and secondary sides, which means high system reliability.

3. EXISTING METHOD

The ever-increasing electrical energy demand has caused intense depletion of conventional energy sources. This has also resulted extensive research in renewable energy source (RES)-based power generations. Especially Solar and wind energy are the two major renewable sources gaining more and more interest among power electronics as well as power system research community instead of their high dependence on varying environmental conditions. This requires new power converter technologies for desired operation, control, and power management, in order to enhance the power quality and to yield utmost power from RESs.

The essential part of renewable energy power conversion system is an inverter which converts the DC power to AC as required by the grid/loads. A conventional two/three level inverter is mostly used in small scale industries and utility applications. However, the output of these inverters contain more harmonics, hence the usage of expensive and bulky low pass passive filters are desired before feeding the power to the utility grid. Further, high voltage stress and high switching loss forbears the application of these inverters in high power application. Consequently multilevel inverters (MLIs) are evolved as best substitute for medium and high power conversion systems. The key features of an MLI are; output waveform with less distortion and less THD content, operation at both fundamental and high switching frequency PWM, a number of redundant switching states, smaller common-mode voltage, etc. But, one common disadvantage is the need of large number of power semiconductor switches.

Each switch requires a gate driver circuit which adds complexity to the system and the overall system cost. Therefore, design of MLIs using low number of components to produce higher output voltage levels are one of the key research issues. Some lower order dominant harmonics exists in the stepped output voltage waveform produced by an MLI. The major impacts of those harmonics are voltage fluctuation, increase in loss, mal-operation, and it also affects the power quality. With the application of appropriate control scheme for an MLI, the aforesaid issues can be well addressed. Researchers have come with a solution of diverse modulation strategies for controlling the MLI. Overall loss reduction and improvement in harmonic profile are the major objective of most of the control techniques discussed in literature. Among the two basic types of control strategies, fundamental/low-frequency switching can provide superior performance than high-frequency switching techniques. Conventional pulse width modulation (PWM),Sinusoidal PWM and space vector modulation (SVPWM) are high-frequency switching techniques which provide faster transient response. Furthermore, different carrier based PWM techniques are introduced that effectively reduces distortion and lowers the EMI. Carrier based PWM techniques are generally of two types, *i.e.*, phaseshifted PWM (PS-PWM) and level-shifted PWM (LS-PWM)techniques. In a PS-PWM control technique, multiple phase-shifted synchronous carriers are required with synchronization of zero crossing of each carrier and voltage references, whereas in LS-PWM technique only one carrier is enough to implement different voltage levels. The former approach is mostly used to evenly distribute the power among MLI modules and to reduce the harmonic distortion. The LS-PWM technique is again classified into three major categories such as phase disposition PWM (PD-PWM), phase opposition and disposition PWM (PODPWM), and alternative phase opposition and disposition PWM (APOD-PWM). All these PWM topologies have either bipolar or uni polar type carrier arrangements with a focus on improving the fundamental output voltage and reduction in total harmonic distortion (THD).

1. REDUCED SWITCH MLI TOPOLOGIES

Although the aforementioned conventional topologies finds numerous applications, but all these topologies needs excess number of power components. So, in the last couple of decades the focus of research on MLI among the researchers is to reduce the device count. Reducing the total number of switches, diodes, capacitor, voltage source can improve the reliability as well as can reduce the overall cost, loss, etc. In this regard, several new RS MLI topologies have been proposed recently and continuous research is still going on to further reduce the requirement of number of components.

In existing system presents a compressive review on some recently developed topologies which are most suitable in different applications such as machine drives, FACTs, and renewable energy systems. These topologies can be used in grid-tied as well as in standalone applications. RS MLI topologies are broadly categorized into three types, *i.e.*, RSS MLI, RSA MLI, and RSM MLI. The modified type MLI includes all thehybrid and topologies which are not based on H-bridge.

A. Reduced Switch Symmetric H-Bridge Type MLI (RSS MLI)

The term symmetric indicates that, all the dc sources used in the circuit are equal in magnitude.. The basic unit of the existing MLI contains two unidirectional semiconductor switches with one dc source. As compared to the conventional CHB MLI, a significant reduction in switch count has been marked in this topology. But, the reduction in switch count is not competitive when compared to recently developed RSS MLI topologies discussed in this work. Furthermore, higher TSV restricts it in high voltage applications. Fig. 2 (a)depicts the schematic diagram of this topology. A new MLI topology with nine different algorithms for the determining the magnitude of dc voltage source has been proposed in .This MLI type has a basic unit consisting of six unidirectional switches and two dc sources. This MLI topology has been shown in Fig.2 (b). Fig. 2(c) shows a novel MLI topology for low-voltage applications. In this literature, an attempt is made to reduce the number of voltage source requirement. For the multilevel generation in the output, two capacitors are used in each module. The capacitor rating is half the rating of the voltage source used in the MLI and the number of capacitor increases with the increase in number of levels. Although the rating of the capacitor is reduced compared to a single capacitor, but the total numberof components are more for producing higher levels. The complexity in charging and voltage balancing issues may also arise in such a condition. This MLI can operate in both symmetric and asymmetric mode. Involvement of two bi-directional switches in the basic unit causes more standing voltage. A schematic of this topology has been shown in Fig. 2(d).

Basic unit of another symmetrical MLI contains three equal magnitude dc sources with four switches. In order to generate higher number of levels, cascaded connection of desired number of basic units has to be made with one extra

series connected dc source. Negative polarity voltage is obtained with the help of H-bridge. A significant reduction in number of switches and lowering of total voltage stress is a major advantage of this topology, thus it can be recommended for higher power and higher voltage applications. This topology can also be used as analternative to the conventional topology for RES applications, as it uses less number of switches than a CHB MLI & with same number of dc sources. This topology has been illustrated in Fig. 2(e).

The topology shown in Fig. 2(f) effectively reduces the need of large number of switches as compared the conventional CHB MLI and cascaded half bridge topology ,but contains some additional diodes. The proposed topology is basically divided into two stages. First stage is responsible for the level generation and the second stage which is nothing but the H-bridge helps in polarity generation. One attractive feature of this topology is that the first stage contains a spike removal switch which removes the high voltage spikes produced at the base. Again to avoid the fluctuations of dc source in case of renewable application, the author had developed clock phase-shifting one-cycle control strategy. Due to the high voltage rating of spike removal switch and H-bridge switches, the topology is restricted to medium voltage application only.

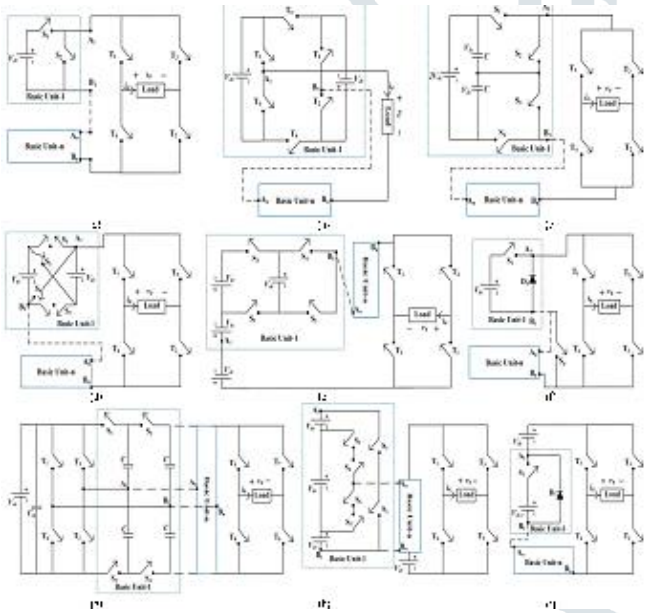


Fig.2. Generalized schematic of the RSS MLI topologies (a) RSS MLI 1. (b) RSS MLI 2. (c) RSS MLI 3. (d)RSS MLI 4. (e) RSS MLI 5. (f) RSS MLI 6.(g) RSS MLI 7. (h) RSS MLI 8. (i) RSS MLI 9.

A novel MLI based upon switched-capacitor modular structure has been shown in Fig. 2(g) and was proposed to be controlled using an optimized SPWM technique such that energy conversion efficiency and power density will be enhanced. a hybrid cascaded MLI containing one H-bridge shown in Fig. 2(h) has been discussed. Reduction in switch count to reduce the cost as well as the THD was significantly achieved and GA-based SHE-PWM approach has been utilized for the control of MLI. This proposed topology can find its suitability in renewable power generation system involving PV and fuel cells. a novel RS MLI is introduced. Compared with the conventional MLI and few recently developed MLIs the proposed MLI shown in Fig.2 (i) has a drastic reduction in number of switches. It requires less than 50% of total switches that are used in the conventional CHB MLI. Lower order harmonics are most dominant in the output of an MLI. Using filters the harmonic profile can be improved, but still there is an impact of lower order dominant harmonics. The author has taken an attempt to eliminate some particular lower order harmonics by calculating optimal switching angles using the SHE technique. To solve the non-linear transcendental equations involved with the SHE technique, author had developed a modified particle swarm optimization technique. As a whole, issues related to large number of switches and harmonic elimination has been addressed by the authors. This topology can find itssuitability in higher voltage or high power application and with renewable energy integration.

B. Reduced Switch Asymmetrical H-Bridge Type MLI (RSA MLI)

An MLI is said to be asymmetric when all the input dc sources used are not equal in magnitude. The main goal of developing the asymmetric MLI is to generate higher number of output voltage levels with the same number of switches and dc sources that are used in symmetric MLI. A variety of relation can be considered for the unequal dc sources. In this paper the relation is taken in a geometric progression manner with the multiplication factor of `3' for a comparative analysis. Fig. 3(a) shows an asymmetrical structure of cascaded H-bridge MLI (ACHB MLI) which presents a new pathway for producing staircase output using non-identical dc sources. A schematic of RSAMLI topologies shown in Fig. 3(b) & 3(c) can operate both in symmetric and asymmetric mode.

In the asymmetric mode the modularization is lost because of unequal dc sources, but still the proposed topology can be extended with a proportional factor. The polarity generation switch faces more voltage stress than the level generation switches and these switches operate at the fundamental switching frequency. Switching pulse generation based on unipolar PWM technique has been outlined in detail. The author had verified that the obtained total harmonic distortion (THD) in asymmetric mode operation satisfies the IEEE-519 standard.

In addition, a considerable reduction in number of switcheshas been observed in comparison with the conventional MLI topologies. The representation of this topology is unveiled in Fig. 3(d).A novel cascaded switched diode topology which can operate in both symmetric and asymmetric mode. The structure of this MLI has been shown in Fig. 3(e) which is the combination of a basic unit and an H-bridge. The basic unit produces a staircase output voltage which is connected to an H-bridge for the polarity generation. The basic unit consists of a dc source, one switch, and onediode. The author has also developed a cascaded structure of this topology. A drastic reduction in number of switch has been observed to generate a particular level of output voltage as compared to a CHB MLI topology. The author has suggested an algorithm for the determination of magnitude of dc sources. Requirement of extra diode puts a limit to the number of level generation by the MLI topology.

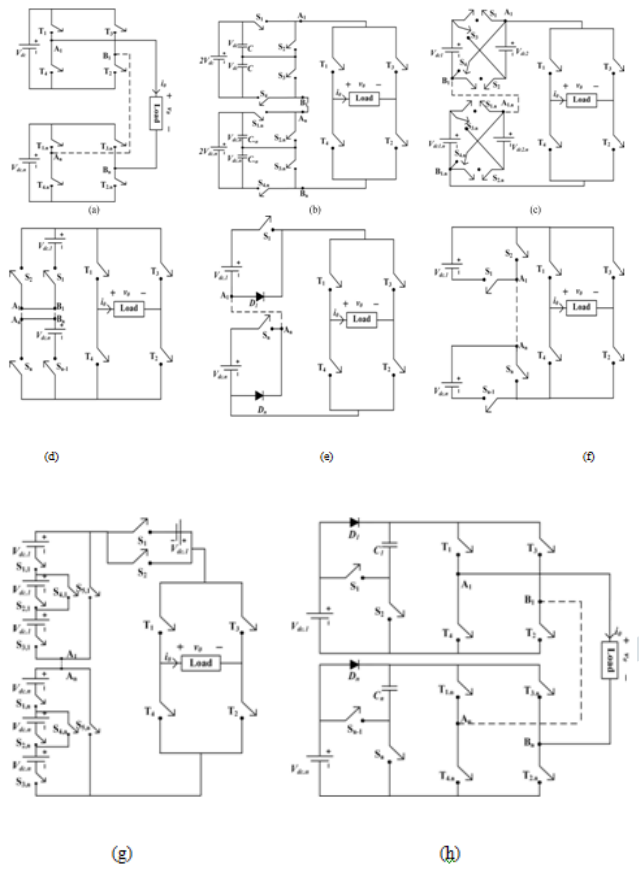


Fig .3.Generalized schematic of the RSA MLI topologies (a) ACHB MLI. (b) RSA MLI 1. (c) RSA MLI 2. (d) RSA MLI 3. (e) RSA MLI 4. (f) RSA MLI 5.(g) RSA MLI 6. (h) RSA MLI 7.

The half-bridge cell consists of an isolated dc source and two switches. This MLI has been derived by the combination of series connected half-bridge cells and an H-bridge. The generalized topology has been shown in Fig. 3(f). Author has suggested that in order to minimize the switching loss, the switches in H-bridge has to be turned off at zero voltage and should be turned on at both zero voltage and zero current. The diode clamped and flying capacitor structure of the same MLI type has also been analysed by the author. The main feature of this topology is the requirement of reduced number of switches; however the high voltage rating H-bridge switches limits its application to medium voltage level.

The MLI structure shown in Fig. 3(g) can be used for medium to high voltage applications. The authors have given an equal attention towards the reduction of both TSV and component count. One additional compact network has been utilized in series with the basic units to further boost the voltage levels. Another MLI topology is based upon the cascadeconnection of H-bridges shown in Fig. 3(h) is very much suitable for high switching frequency distribution system. However, in asymmetrical mode of operation, capacitance sizing and voltage balancing problems may arise. To confront this issue, additional voltage balancing circuit need to be introduced in the aforesaid situation.

C. Reduced Switch Modified MLI (RSM MLI)

Topologies without an H-bridge are considered in this section. Basically H-bridge topologies are more suitable for the low and medium voltage application. A schematic of this topology has been illustrated in Fig. 4(a). The main aim of the topology is to produce a large number of levels in the output by reducing the total component count. Total component count in this MLI is less than the conventional MLI topologies, but due to the use of bi-directional switches, the voltage stress and switching loss is more than few recently developed topologies discussed earlier in this work. Total voltage stresses across the switches, diodes, and the isolated dc sources of this topology are same as a CHB MLI topology. Furthermore this topology possess a limited number ofredundant switching states as compared to the conventional topologies, hence the cells under fault condition can't be bypassed. It can be said that, modularity and the fault tolerant capacity of this topology is less than the CHB MLI topology.

The topology shown in Fig. 4(a) MLI consists of a single dc source and a dc-link capacitor, thus the requirement of dc sources is drastically reduced compared to conventional CHB MLI as the level increases. Number of switches used in this topology is same as the MLI shown in Fig. 4(a) for producing 5-levels in the output. Availability of more redundant switching states is an additional advantage of this topology which reduces the voltage balancing concern. Requirement of sensors for controlling the MLI & maintaining the desired capacitor voltage can also be reduced as suggested by the authors. The topology contains the series connection of fundamental blocks. The combination of six switches, two dc sources and eight diodes makes fundamental block.

Fig. 4(b) depicts the circuit diagram of this topology. Author has validated the topology in both symmetric and asymmetric mode and found that the asymmetric mode produces a high resolution output voltage waveform for the same number of basic block. The proposed topology requires less number of switches as compared to the conventional MLIs, but not compared other recently proposed RS MLIs. Also, it requires large number of extra diodes to form a basic block which can be considered as a limitation of the topology. However, this topology is suitable in medium and high voltage applications.

Fig. 4(c) shows the generalized circuit topology of this MLI. The power circuit of this cascaded MLIconsists of two dc sources, two different bridges and one auxiliary bi-directional current steering circuit. One among the two dc sources is split in two equal half by the auxiliary circuit, so in overall three dc sources are used in each power circuit. A novel hybrid T-type topology was proposed for high efficiency application. An attempt was made to reduce the switching loss by reducing the requirement of large number of switches. The topology requires only one voltage source as shown in Fig. 4(d). A number of capacitors are connected for the multiple level generations in the output. Availability of redundant switching states avoids the capacitor voltage balancing problem and improves the faulttolerant capability. An interesting control method based on phase-disposition PWM (PD-PWM) method has been analysed for controlling the operation of MLI through capacitor voltage balancing. The proposed controlled scheme can be easily generalized for high power MLIs. Fig. 4(e) depicts the generalized structure of the topology. Author had applied SHE-PWM technique to control the MLI by calculating optimum switching angles which results in low THD.Lower voltage stress on the switch and lower THD makes this topology suitable for high voltage and high power applications.

Fig. 4(f) shows the generalized structure of this topology. Four dc sources and twelve switches constitute a module and each module generates a seventeen level output voltage. To achieve more levels the cascaded connection of modules can be made. A nearest level control method is used for generating switching pulses which reduces computational burden of the processor. Moreover the ability of generating more levels, less THD with a demand of less number of switches and dc sources makes the topology

superior among other topologies developed .One semi half-bridge cell is composed of one dc source, one diode, and one switch. To generate higher levels, more semi half bridge cells can be connected in series fashion.

The generalized structure is formed by connecting the string of series connected semi half-bridge cells in crisscross manner through the switches as shown in Fig. 4(g). The proposed topology achieves its purpose of staircase output by using reduced number of switches and having less standing voltage. However, the requirement of extra diodes increases with the addition of output voltage levels.

In fig. 4(h) The generalized structure consists of series connected cells, six main switches and one dc source with a proper arrangement. The combination of one dc source and two switches forms a sub-cell of this configuration.

Fig. 4(i) unveils the proposed topology. Although the superiority of this topology is found over conventional CHB MLI in terms of reduced number of switches, but the standing voltage of the proposed topology is more as compared to CHB MLI restricting the application to low and medium voltage applications.

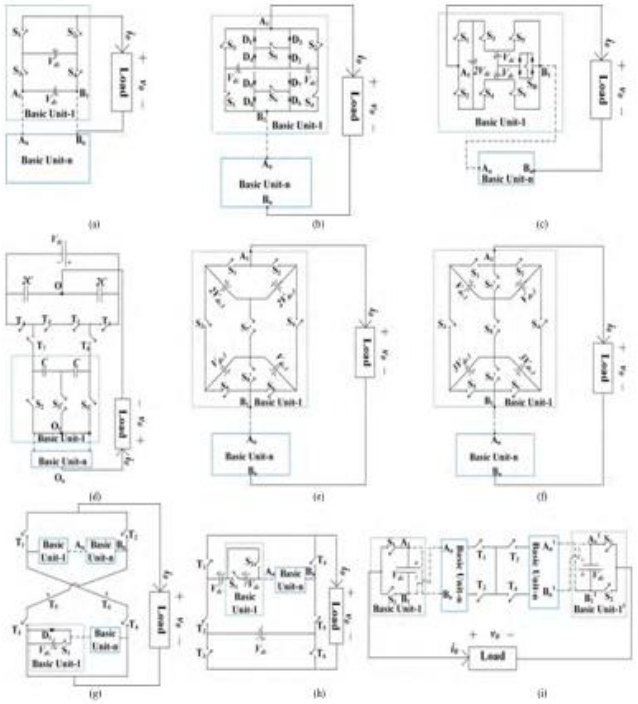


Fig 3. Generalized schematic of the RSMMLI Topologies (a) RSMMLI1. (b)RSMMLI2. (c)RSMMLI3. (d)RSMMLI4. (e)RSMMLI5. (f) RSMMLI6. (g)RSMMLI7. (h)RSMMLI8. (i) RSMMLI9

4. PROPOSED METHOD

This work recommends the performance of coupled inductor based novel 11-level inverter with reduced number of switches. The inverter which engender the sinusoidal output voltage by the using split inductor with minimised total harmonic distortion (THD). The voltage stress on each controlled switching devices, capacitor balancing and switching losses can be reduced. The proposed system gives better controlled output current and improved output voltage with moderate THD value. The switching devices of the system are controlled by using multicarrier sinusoidal pulse width modulation algorithm by comparing the carrier signals with sinusoidal signal. The simulation and experimental results of the proposed 11-level inverter system outputs are established using MATLAB/SIMULINK.

An inverter is an electronic device or circuitry that changes direct current (DC) to alternating current (AC). The input voltage, output voltage and frequency, and overall power handling depend on the design of the specific device or circuitry. Nowadays many industrial applications have begun to meet the power demand. These high-power motor drives and utility applications require medium voltage. A multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input.

Nowadays the requirement of power equipment's is increasing rapidly, which increases the harmonic content within them . Various models and thesis have been proposed to reduce them. Levels of inverters are increased to reduce the harmonics. Some of them use greater number of switches to increase the level of the inverter. Contradicting this fact this inverter topology uses less number of switches and uses multicarrier sine waves as an interrupt. Unlike it does not use triangular wave with phase disposition technique. Multicarrier pulse width modulation works with a constant carrier frequency not synchronized with fundamental stator frequency. Multi carrier pulse width modulation gives an optimal utilization of switching frequency permitted, therefore PWM carrier frequency may be chosen to a value of two times the permitted switching frequency.

Multicarrier PWM strategy is the widely-adopted modulation strategy for multi-level inverter. It is similar to that of the SPWM strategy except for the fact that several carriers are used. In this technique, several triangular inputs is compared with a sine wave. The number of carriers required to produce m-level output is m-1. All carriers have the same peak to peak amplitude Ac and same frequency fc except for variable frequency PWM. The point of intersection of the triangular wave with sine wave gives step input as output. The reference sine wave is continuously compared with each of the triangular waves and whenever the reference is greater than the carrier signal, pulse is generated.

The proposed simulation uses multicarrier sinusoidal pulse width modulation technique to generate 11-level output voltage. It also uses lesser number of switches as compared to the previous proposed models. This reduces the dv/dt loss and thus reducing the harmonics. For a particular output voltage, it uses only two switches. The voltage stress on each controlled switching devices, capacitor balancing and switching losses can be reduced. The proposed system gives better controlled output current and improved output voltage with moderate THD value. The simulation and experimental results of the proposed 11-level inverter system outputs are established using MATLAB/SIMULINK.

A. Working of 11-Level Inverter

In Figure 5 shows power circuit of 7 level inverter consists of dc link capacitor C1, C2, C3, C4 and C5 across the applied dc source. Power semiconductor switches S1, S2, S3, S4, S5, S6, S7 and S8 and freewheeling diodes D1, D2, D3, D4, D5, D6, D7 and D8 are used to combine the voltages to acquire the 11 level voltages. And which contains conventional 2 level VSI circuit is added with front circuit, which consists of power switches S9, S10, S11, and S12 and coupled inductor is used connect with load circuit.

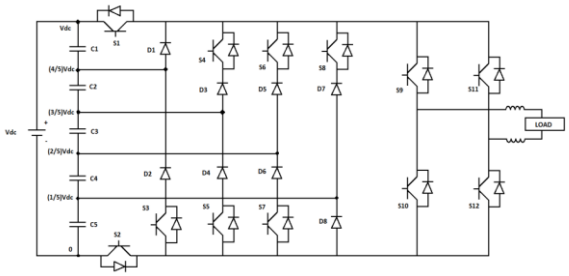


Fig 5. Circuit of novel 11-level inverter

B .Modes of Operation

From the power circuit of 11-level voltage inverter has the following eleven switching mode combinations is shown in Figure 6.

Mode 1: to attain the output voltage level as +Vdc, the switches S1, S2, S9, and S12 are kept in ON condition. Here none of the freewheeling diode is in ON condition, which is shown in Figure 6(a).

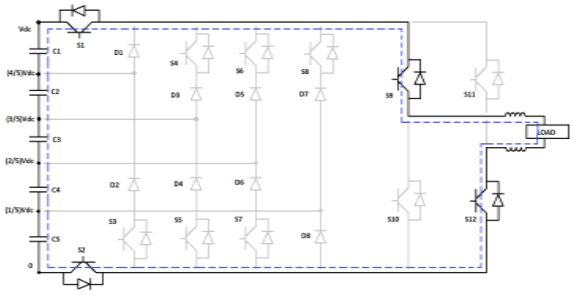


Fig .6(a) Mode 1

Mode 2: to obtain the output voltage level as + 4/5Vdc, the switches S1, S9, and S12 are kept in ON condition. And here freewheeling diode D8 is in ON condition, which is shown in Figure 6(b).

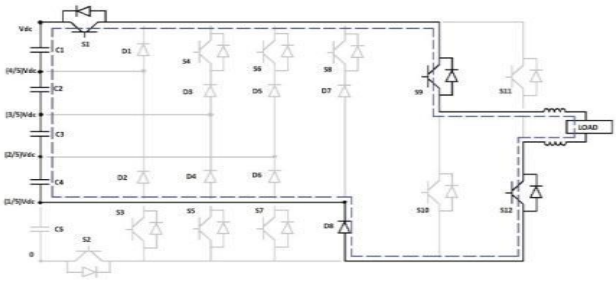


Fig. 6 (b) Mode 2

Mode 3: to acquire the output voltage level as + 3/5Vdc, the switches S1, S9, S12 and S7 are kept in ON condition. And here freewheeling diode D6 is in ON condition, which is shown in Figure 6 (c).

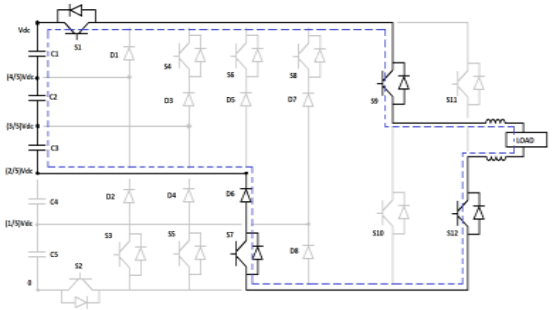


Fig.6 (c) Mode 3

Mode 4: to generate the output voltage level as + 2/5Vdc, the switches S1, S9, S12 and S5 are kept in ON condition. And here freewheeling diode D4 is in ON condition, which is shown in Figure 6 (d).

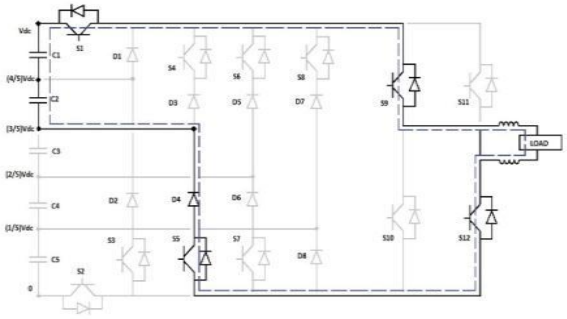


Fig.6 (d) Mode 4

Mode 5: to generate the output voltage level as + 1/5 Vdc, the switches S1, S9, S12 and S3 are kept in ON condition. And here freewheeling diode D2 is in ON condition, which is shown in Figure 6(e).

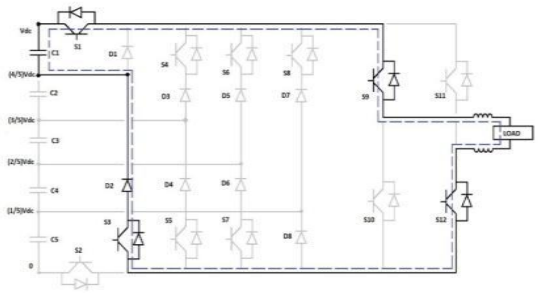


Fig. 6 (e) Mode 5

Mode 6: to obtain the output voltage level as – Vdc, the switches S2, S10, S11 and S1 are kept in ON condition. And none of the freewheeling diodes is in ON condition, which is shown in Figure 6(f).

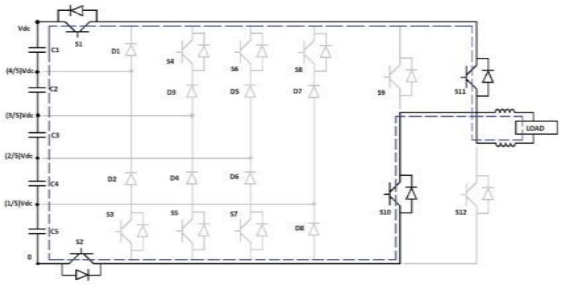


Fig .6 (f) Mode 6

Mode 7: to obtain the output voltage level as – 4/5Vdc, the switches S2, S10, and S11 are kept in ON condition. And here freewheeling diode D1 is in ON condition, which is shown in Figure 6 (g).

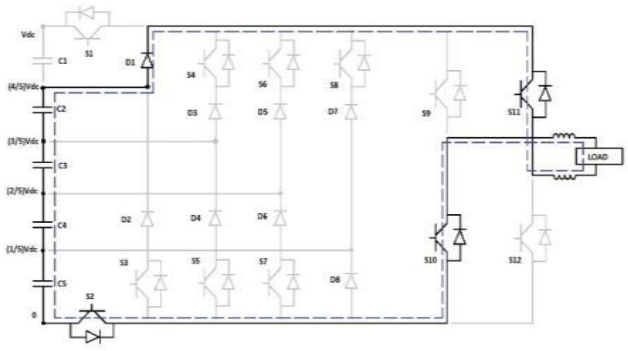


Fig.6 (g) Mode 7

Mode 8: to obtain the output voltage level as – 3/5Vdc, the switches S2, S10, S11 and S4 are kept in ON condition. And here freewheeling diode D3 is in ON condition, which is shown in Figure 6(h).

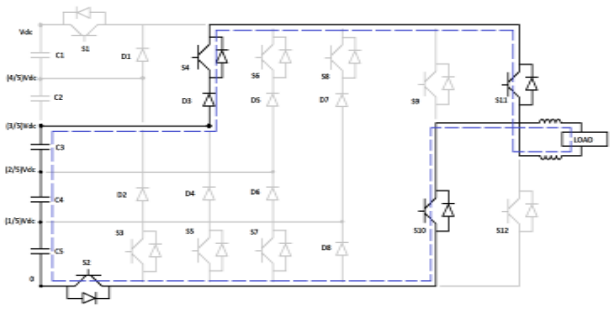


Fig. 6 (h) Mode 8

Mode 9: to obtain the output voltage level as – 2/5Vdc, the switches S2, S10, S11 and S7 kept in ON condition. And here freewheeling diode D5 in ON condition, which is shown in Figure 6(i).

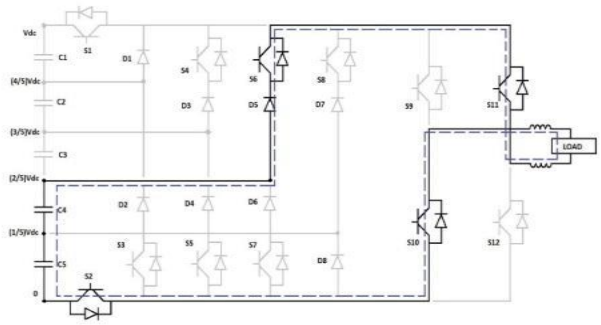
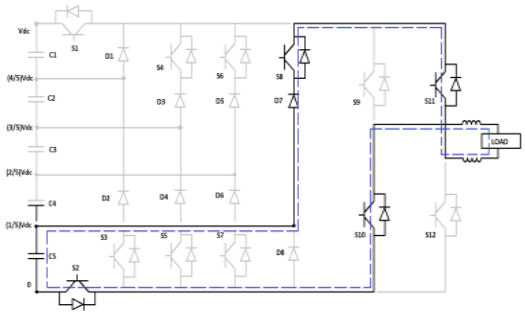


Fig.6 (i) Mode 9

Mode 10: to obtain the output voltage level as – 1/5 Vdc, the switches S2, S10, S11 and S8 are kept in ON condition. And here freewheeling diode D7 is in ON condition, which is shown in Figure 6(j).



Fi.6 (j) Mode 10

Mode 11: to gain the output voltage level as 0, the switches S9 and S11 are kept in ON condition. And here none of the freewheeling diode is in ON condition, which is shown in Figure 2.2(k) and also modes of operation with position of components shown in Table 1.

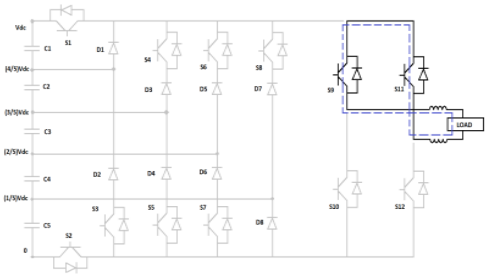


Fig.6 (k) Mode 11

TABLE 1 Modes of operation with position of components

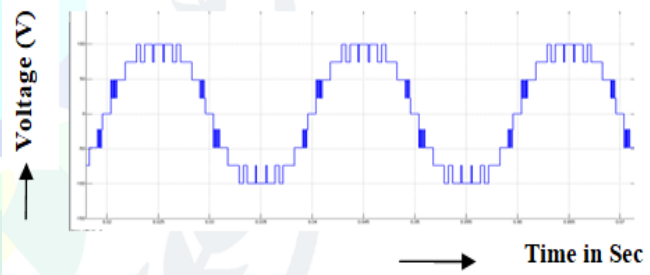
Output voltage level	Capacitor ON	Switches ON	Freewheeling diode ON
$+V_{DC}$	C_1,C_2,C_3,C_4,C_5	S_1,S_2,S_{10},S_{11}	-
$+\frac{4}{5}V_{DC}$	C_1,C_2,C_3,C_4	S_1,S_9,S_{12}	D_8
$+\frac{3}{5}V_{DC}$	C_1,C_2,C_3	S_1,S_7,S_9,S_{12}	D_6
$+\frac{2}{5}V_{DC}$	C_1,C_2	S_1,S_5,S_9,S_{12}	D_4
$+\frac{1}{5}V_{DC}$	C_1	S_1,S_3,S_9,S_{12}	D_2
0	-	S_9,S_{11}	-
$-V_{DC}$	C_1,C_2,C_3,C_4,C_5	S_1,S_2,S_{10},S_{11}	-
$-\frac{4}{5}V_{DC}$	C_2,C_3,C_4,C_5	S_2,S_{10},S_{11}	D_1
$-\frac{3}{5}V_{DC}$	C_3,C_4,C_5	S_2,S_4,S_{10},S_{11}	D_3
$-\frac{2}{5}V_{DC}$	C_4,C_5	S_2,S_7,S_{10},S_{11}	D_5
$-\frac{1}{5}V_{DC}$	C_5	S_2,S_8,S_{10},S_{11}	D_7

5. SIMULATIONS RESULTS

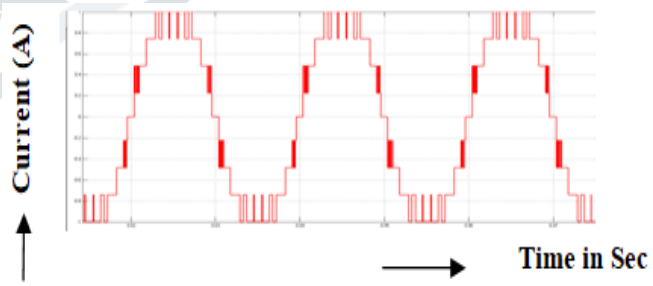
I. EXISTING SYSTEM

1. 9-level MLI with SPWM control technique

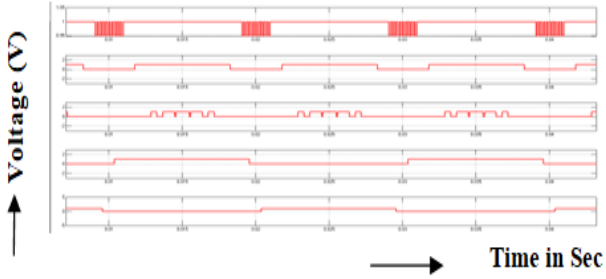
A. Load voltage waveform



B. Load current waveform

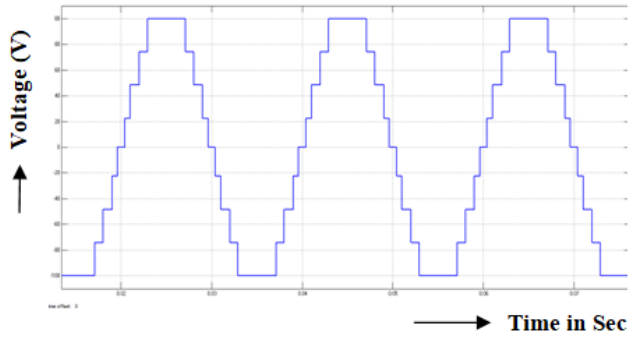


C. Gate pulse waveforms

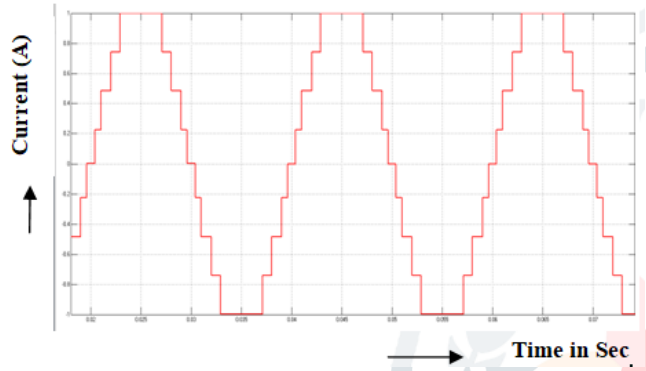


2. 9-level MLI with SHE control strategy

A. Load voltage waveform



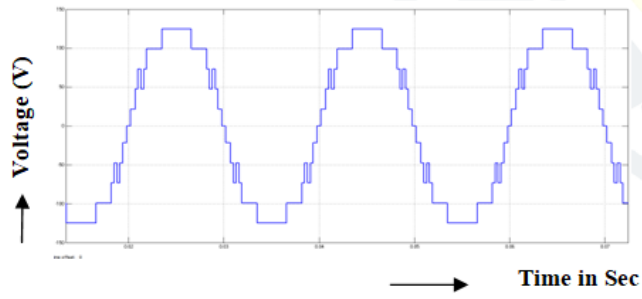
B. Load current waveform



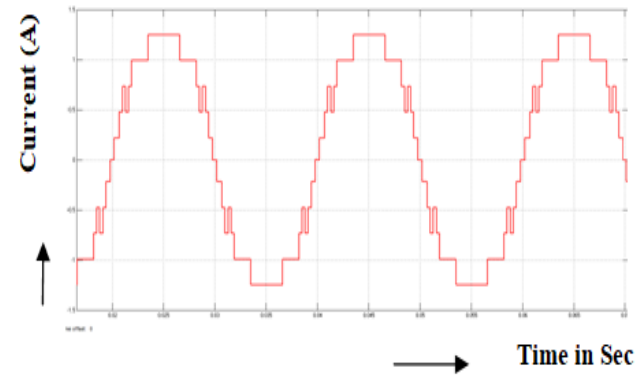
II. PROPOSED SYSTEM

1. 11-level MLI with SPWM control technique

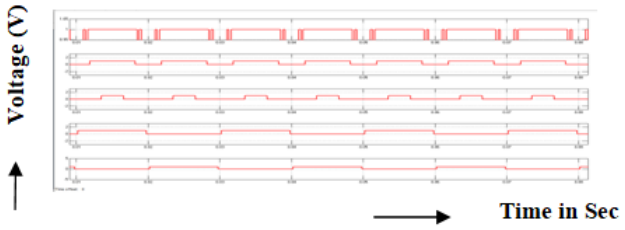
A. Load voltage waveform



B. Load current waveform

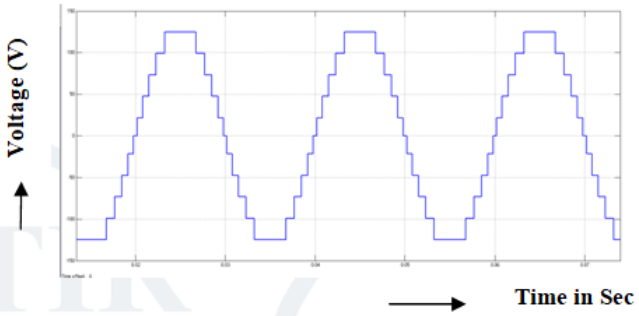


C. Gate pulse waveforms

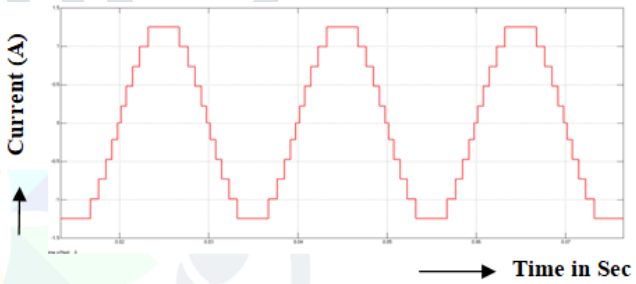


2. 11-level MLI with SHE control strategy

A. Load voltage waveform



B. Load current waveform



3. COMPARISION TABLE

Control Strategy	MLI	THD
SPWM	9-Level MLI	9.30%
	11-level MLI	7.44%
SHE	9-Level MLI	9.30%
	11-level MLI	7.44%

6. CONCLUSION

The objective of the review is to cover most of the recently proposed MLI and the useful information has been effectively detailed through this review. A comparison of 9 Level and 11 Level MLI based on the types of controller used, different switching techniques and significant remarks are also included. The MLI topology should be chosen carefully keeping in view of the optimal performance parameters. Key parameter deciding the performance, cost, and control complexity of an MLI for PV integration and drives application are discussed. To illustrate the working of MLI, experimental results are included taking a RS MLI topology for different level generation. In this aspect, both fundamental switching frequency (SHE-PWM) and high switching frequency (SPWM) control techniques are implemented. The main aim of implementing both the

switching techniques is to provide preeminent knowledge to the readers regarding different control approaches. This paper is promising for early stage power engineers working in this area, in the aspects of selecting the suitable topology for the definite application with accurate switching scheme.

Future Scope

. In future scope to develop with 13 levels MLI in both fundamental switching frequency (SHE-PWM) and high switching frequency (SPWM) control techniques

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