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# Efficient Design of Rounding-based Approximate Modified Karatsuba Multiplier

**[1]T. Hemasundari,[2]D.Naresh Kumar**
[1]PG Scholar,[2]Professor
[1,2]Department of Electronics and Communication Engineering,
[1,2]Lendi Institute of Engineering and Technology (A), Jonnada , Andhra Pradesh ,India

***Abstract:*** Arithmetic operations are significant in many applications, such as image processing. These operations are the most widely used multipliers, such as the Wallace tree and Karatsuba multipliers. But in all these multipliers, we have many problems, which are area consumption, delay etc., with an increase in the size of the multiplier. Hence, this paper proposed a modified Karatsuba multiplier using the rounding method. The simulation results reveal that the Proposed Multiplier (PM) provides better performance in terms of area and delay compared to existing designs .The proposed and existing designs are coded Verilog HDL and synthesized and simulated using Xilinx Vivado 2016.4 environment**.**

***Index Terms*** **- Karatsuba multiplier, Wallace Tree multiplier, rounding, adders, Shifters, Approximate computing.**

## I. INTRODUCTION

Approximate computing (AC) is one of the techniques for reducing energy usage and/or increasing speed. AC can be used in error-resilient applications because the computing result may not be correct. These applications include audio and image processing, machine learning, and data mining. A considerable amount of the energy consumption in many signal processing applications is due to arithmetic operations (e.g., up to nearly 75% of the total energy consumption of a rapid Fourier transform architecture). Multiplication, employed frequently, is a high-latency and energy-consuming process among these. As a result, approximation multipliers are excellent candidates for use in error-tolerant signal processing units. Generally, a multiplication operation consists of three steps. In the first step, the partial products are generated based on the input operands. The partial products are accumulated in the second step until only two rows remain. In the final step, a (fast) adder summons the remaining two rows. One may apply the approximation to each of these steps.

In the field of electronic industry, digital filters are used extensively. The noise ranges gradually increase by using analog filters, for better noise performance can be obtained using digital filters compared to analog filters. At every intermediate step in digital filter transformation, able to perform noiseless mathematical operations. Our design includes the optimization of bit width and hardware resources without any impact on the frequency response and output signal precision. Addition (or subtraction), multiplication (generally of a signal by a constant) Time Delay, i.e., delaying a digital signal by one or more sample periods, are three basic mathematical operations used in digital filters. The coefficients are multiplied by fixed-point constants using additions, subtractions, and shifts in a multiplier block. In VLSI Signal Processing, two digital filters are most widely used: FIR (finite impulse response) and IIR(infinite impulse response).

FIR indicates that the impulses are finite in this filter, and phase is kept linear to noise distortions, and no feedback is used for such a filter. As compared to IIR, FIR is straightforward to design. Such types of FIR filters are used in DSP processors for high speed. In Digital Signal Processing, Multiplication and addition are of times required. A high-speed addition is done by parallel prefix adder, and the better version of the truncated multiplier with fewer components reduces delay. In Digital Signal Processing, FIR filters define less number of bits which are designed by using finite precision.

One of the arithmetic operation multiplications is tiresome, so multipliers are the main components in arithmetic, signal, and image processors. Signal and image processing consists of multiplying functions like multiply, accumulate, convolution, and filtering. The operation rate of the multiplier unit impacts the execution time of a particular process. In Digital signal processing (DSP) algorithms, multiplication takes more time than other operations, so the critical delay path is calculated for complete operation based on the delay required for multiplication unit, and it measures algorithm performance. The most widely used operations in computer arithmetic are addition and multiplication in case of approximate computing full-adder calls extensively analyzed for addition operation [1-3]. All DSP algorithms would need some form of Multiplication and Accumulation Operation. Most of the DSP algorithms need multiplication and accumulation operation. MAC consists of an adder, multiplier, and accumulator. Usually, DSP adders are RCA and CSA. Generally ,the multiplier multiplies the input values and passes the result to the adder, then the adder adds to the previous accumulator result.

The rest of the paper is organized as follows: Section 2 discusses the previous designs. Section 3gives a clear explanation of the proposed design. Section 4constitutes the performance. Finally, in Section 5, the conclusion is given.

## II. Literature Review

This section discusses the existing multipliers related to the proposed design.

A Dynamic Range Unbiased Multiplier for Approximate Applications is highly scalable, allowing designers to configure it to trade power and accuracy. Also, its unbiased nature reduces errors when used for computations within applications [4].With high accuracy, rounding-Based Approximate Multiplier (RBAM) was based on rounding the inputs in $2^n$. In this way, the computationally intensive part of the multiplication was omitted, improving speed and energy consumption at the price of a small error [5]. A low energy truncation-based approximate multiplier worked based on finding scientific binary representation of the operands and truncating the intermediate results used to calculate the final result [6].A low-energy and area-efficient approximate multiplier in which the input operands were truncated with two different lengths, t and h, and then rounded to the nearest odd numbers to reduce the error resulting from the truncation operation [7]. The Karatsuba Multiplier (KM) is proposed with three small-size multipliers to reduce the area consumption and increase the overall performance [8]. Finally, the Karatsuba multiplier was modified using a rounding approach, but the suggested design was better for small-size multipliers [9].

P. Lohray et al. [10] proposed multiplier can decrease the design complexity with increased performance and power efficiency for error-avoid applications. In this paper, partial products of the multiplier are altered to introduce varying probability terms. The proposed AM is utilized in two variants of 16-bit multipliers. Synthesis results reveal that two proposed AM achieve power savings of 72% and38%, respectively, compared to an EAM. They have better precision when compared to EAM. Mean relative error figures are a slow as 7.6% and 0.02% for the proposed AM, which are better than the previous works. The performance of the proposed AM is evaluated with an image processing application, where one of the proposed models achieves the highest peak signal-to-noise ratio.

M .Pradeep Kumar et al. [11] proposed HS RBAM using a high-performance Han-Carlson adder, which multiplies only signed numbers. This paper first explains the existing ROBAM and then designs the Proposed RBAM. The design of Existing and proposed ROBAM using Xilinx 14.7 increased the speed of proposed RBAM by 4% compared to Existing ROBAM .From the review of existing designs, it is observed that delay increases with increasing the bit size.

The Existing RBAM used a ripple carry adder at the addition stage. Still, the proposed RBAM used a hybrid adder at the Modified or Hybrid adder is the faster addition technique generated by merging two adder designs: carry select adder and kong stone adder[12]. The carry-select adder is simple but rather fast. The carry select adder consists of two Ripple Carry Adder circuits and Multiplexer [13]-[18].Hence, the following proposes the modified Karatsuba multiplier using a rounding approach with a high-speed adder.

## III. Proposed Karatsuba Multiplier

The PM main objective is to reduce the number of multiplier blocks compared to the KM [8] and to reduce the circuit complexity compared to RBAM [4]. The recommended design also boosts performance by ameliorating the multiplier's size.

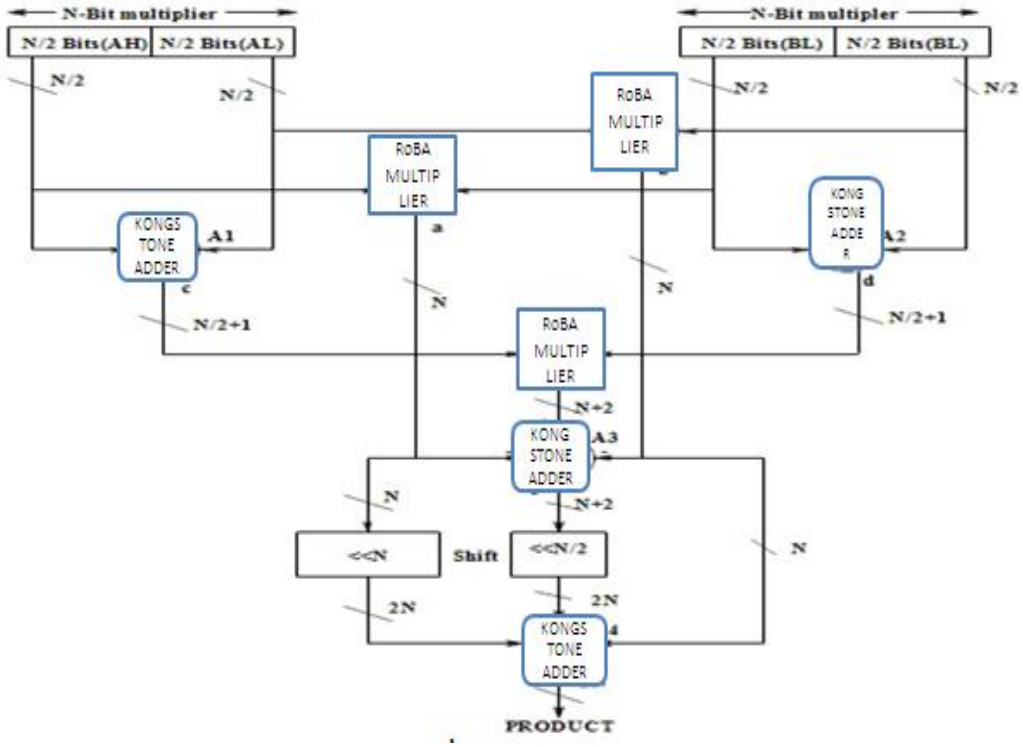
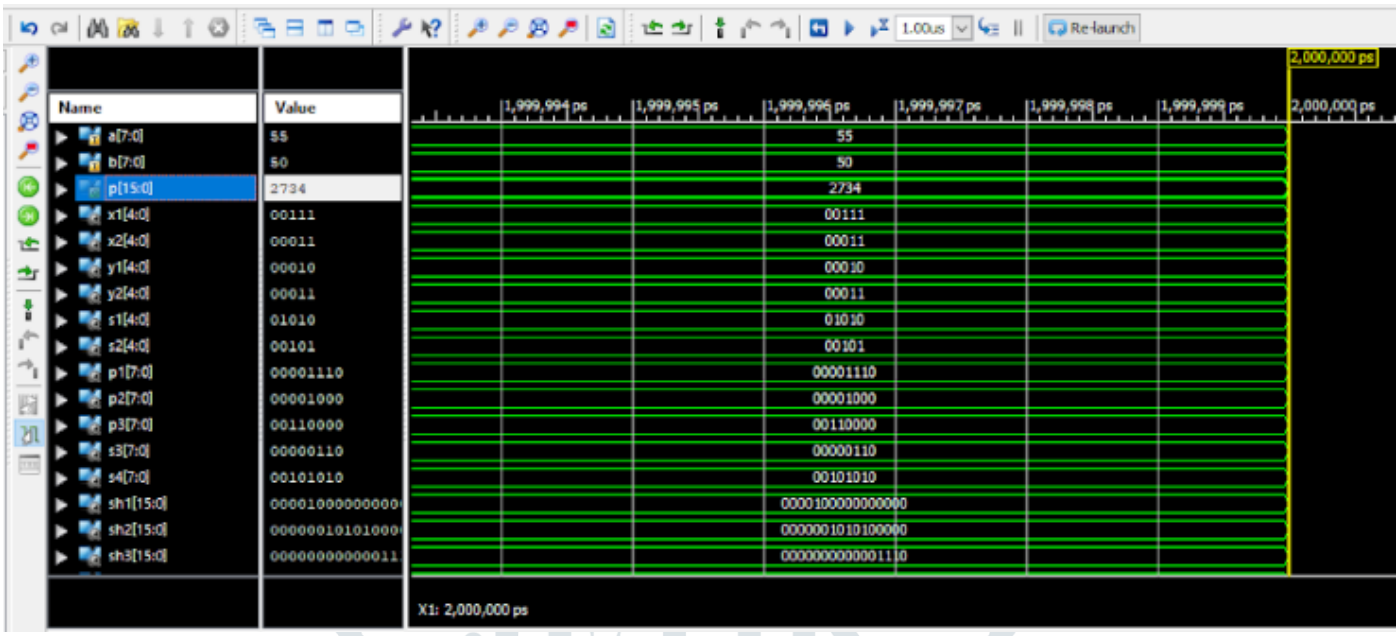



Fig. 1 Block Diagram of Proposed Modified Karatsuba Multiplier using Rounding approach and Kong Stone Adder

The PM Architecture is shown in Fig. 1. Initially, *A* and *B* are divided into $A_H$, $A_L$, $B_H$, and $B_L$ using four *n/2*-bit selectors. Later, $A_H$ and $A_L$ are added using the Kong Stone adder (A1), and $B_H$ and $B_L$ are added using another adder Kong Stone adder (A2). Then, $A_H$, and $B_H$ is further multiplied, $A_L$ and $B_L$, and $A_H + A_L$ and $B_H + B_L$ are multiplied using rounding-based multipliers [4]. Following the shifter unit, the approximate products of three multipliers are left-shifted with n, n/2, and n bit. Finally, the n-bit PM is found from the final 2n-bit adder output after applying these shifters outputs using Kong Stone adder.

## IV. RESULTS AND DISCUSSION

Fig. 2 shows the Simulation result for the proposed design using the rounding approach. The simulations are performed by using the Xilinx Vivado simulator.

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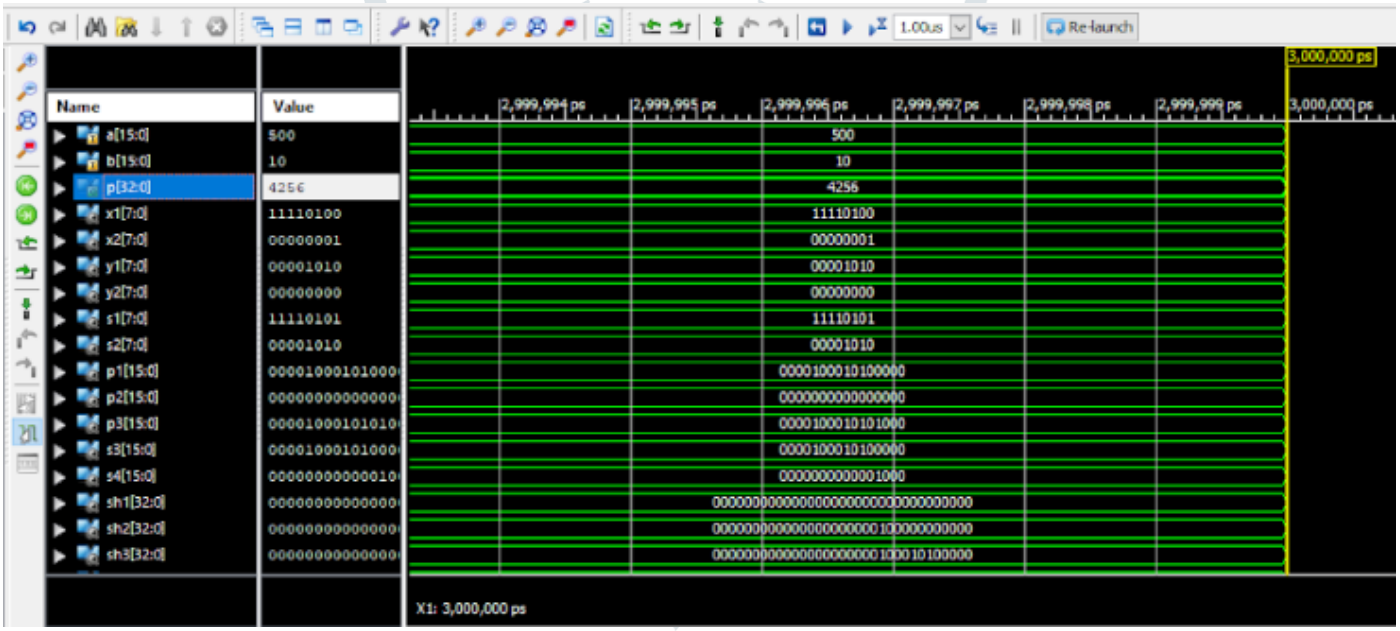



(b)

Fig. 2Simulation results of the 8-bit and 16-bit PM

When comparing the results of Proposed and Existing RBAM and KM with respect to area and delay following observations are made. From Tables 1 and 2, the number of slices occupied by the PM was very small compared to the Existing RBAM and KM. This is because the multiplication process has been significantly simplified by rounding the values to the nearest power of two. Even though this results in a small error in the output value, the area of the multiplier has been drastically reduced. This reduced area results in faster multiplication which is more suitable for error-tolerant applications. Performance Comparison Proposed and Existing Multipliers in terms Number of Slices and Delay are depicted in Fig. 3. The comparison graph clearly shows that the proposed design provides better performance compared to the existing designs.

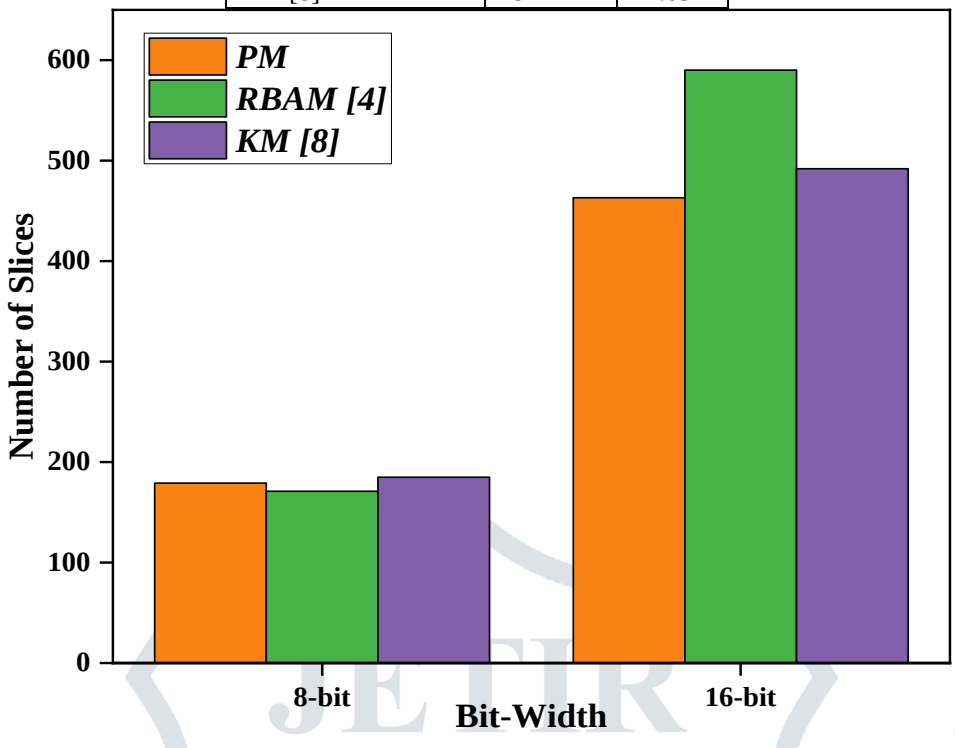
Table1: Comparison of 8-bit Proposed and Existing Designs

| Name of the Design | Number of Slices | Delay (ns) |
|---|---|---|
| PM | 179 | 8.01 |
| RBAM [4] | 171 | 9.25 |
| KM [8] | 185 | 8.52 |

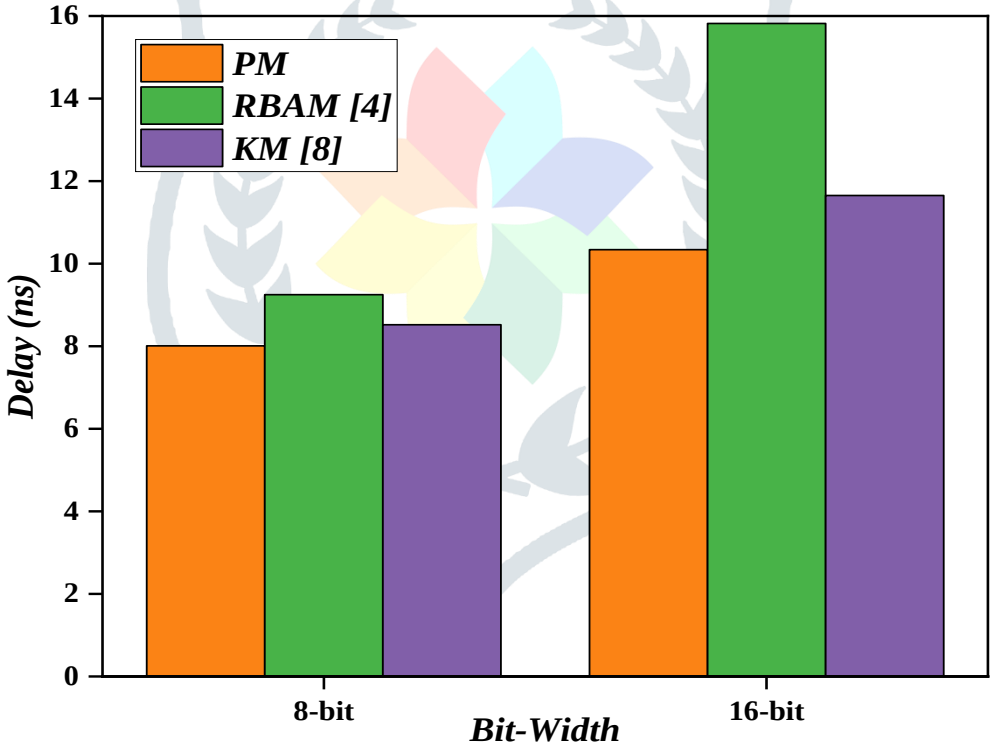
Table2: Comparison of 16-bit Proposed and Existing Designs

| Name of the Design | Number of Slices | Delay (ns) |
|---|---|---|

| | | |
|---|---|---|
| PM | 463 | 10.34 |
| RBAM [4] | 590 | 15.82 |
| KM [8] | 492 | 11.65 |




(a)




(b)

Fig. 3 Performance Comparison Proposed and Existing Multipliers in terms of Number of Slices and Delay

## V. Conclusion

A modified Karatsuba multiplier using the rounding method was proposed in the paper. The results show that the PM performs better in terms of area and delay. The proposed design simulation results show better speed reduced an occupying the Existing RBAM and KM area. The above results were obtained after simulating the proposed and existing multipliers using Xilinx Vivado at an operated voltage of 1.0V.

## References

[1] V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, "IMPACT: IMPrecise adders for Low-Power Approximate Computing", Proc. of Int. Symp. On Low Power Electronics and Design (ISLPED). 1-3 Aug. 2011

[2] S. Cheemalavagu, P. Korkmaz, K.V. Palem, B.E.S. Akgul, and L.N. Chakrapani, "A Probabilistic CMOS Switch and its Realization by Exploiting Noise," in Proc. IFIP-VLSI SoC, Perth, Australia, Oct 2005

[3] H.R. Mahdiani, A. Ahmadi, S.M. Fakhraie, C. Lucas, "Bio-Inspired Imprecise Computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications", IEEE Trans. on Circuits and Systems I: Regular Papers, Vol. 57, No. 4, pp. 850-862, April 2010

[4] Hashemi S, Bahar RI, Reda S, "DRUM: A dynamic rangeunbiased multiplier for approximate applications",In: Proc. OfIEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, pp. 418–25,2015
[5] R. Zendegani, M. Kamal, M. Bahadori, A. Afzali-Kusha and M. Pedram, "RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 2, pp. 393-401, Feb. 2017
[6] Vahdat S, Kamal M, Afzali-Kusha A, Pedram M, "LETAM:A low energy truncation-based approximate multiplier", Computer Electrical Engineering 63:1–17, 2017
[7] Vahdat S, Kamal M,Afzali-Kusha A, Pedram M,"TOSAM:An energy-efficient truncation-and rounding-based scalable approximate multiplier", IEEE Transact Very Large Scale Integration (VLSI) Systems 27(5):1161–1173, Dec. 2019
[8] Jain R, Pandey N, "Approximate Karatsuba multiplierfor error-resilient applications", AEU-International Journal Electronic Communication, 130:153–579, 2021
[9] Jagadeeswara Rao E, K. Tarakeswara Rao, K. SudhaRamya, D. Ajaykumar, R. Trinadh, "Efficient Design of Rounding-Based Approximate Multiplier Using Modified Karatsuba Algorithm", Journal of Electronic testing, vol. , Oct. 2022
[10] P. Lohray, S. Gali, S. Rangisetti and T. Nikoubin, "Rounding Technique Analysis for Power-Area & Energy Efficient Approximate Multiplier Design," 2019
[11] IEEE 9th Annual Computing and Communication Workshop and Conf. (CCWC), Las Vegas, NV, USA, 2019, pp. 0420-0425.
[12] M.Pradeep Kumar, A.S.Aparna, P.Pavan Kumar, D.SivaGangadhar Rao and N.M.Ramalingeswara Rao," Rounding Based Approximate (Roba) Multiplier", Journal of Emerging Technologies and Innovative Research (JETIR) (UGC Approval), vol.6, No. 4, pp. 448-454, April 2019
[13] AritraMitra, Amit Bakshi, "Performance Improvement of a Modified Carry Select Adder", 24th IRF International Conference, Chennai, India, ISBN: 978-93-85465-07-9,pp 69-77, 3rd May 2015.
[14] ShivaniParmar, Kirat Pal Singh, Design of high speed hybrid carry select adder ", 3rd IEEE, International Advance Computing Conference (IACC), pp:1656 – 1663,2013.
[15] PallaviSaxena, Urvashi Purohit, Priyanka Joshi," Analysis of Low Power, Area- Efficient and High Speed Fast Adder", International Journal of AdvancedResearch in Computer and Communication Engineering , ISSN : 2278-1021,Vol. 2, Issue 9,pp 3705- 3710,September 2013.
[16] TheegalaRavinder Reddy, P.Anjaiah ," Design of High Speed Hybrid Carry Select Adder", International Journal & Magazine of Engineering,Technology,Management and Research, ISSN No: 2348-4845, Volume No: 2 , Issue No: 7 ,pp 1151-1156,July 2015.
[17] AritraMitra ,Amit Bakshi, Bhavesh Sharma ,NileshDidwania "Design of a High Speed Adder",International Journal of scientific and EngineeringResearch, Volume 6,Issue 4,April 2015.
[18] Jasmine Saini, Somya Agarwal, Aditi Kansal," performance, analysis and comparison of digital adders", IEEE, International Conference on Advances inComputer Engineering and Applications (ICACEA)IMS Engineering College, Ghaziabad, India,2015.