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Implementation and Comparison of Carrier Shift PWM Technique for Multilevel Inverter

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Abstract: This article relates different multilevel inverter topologies with PWM techniques and the implementation of level shift PWM techniques to five-level cascaded H-bridge (CHB) inverters. Multilevel inverters are found suitable for high voltage and high power applications as the voltage stress on a switching device gets reduced in it. The output of the multilevel inverter is having low THD which makes them suitable for renewable energy integration and drives applications in industry.

In the proposed five-level Cascade multilevel inverter (MLI) phase disposition, phase opposition disposition, and alternate phase apposition disposition PWM methods were implemented. The comparative analysis has been done by using the Simulink platform of MATLAB software and the result validation has been performed through the prototype model. The base of comparison is taken as a THD and ease of implementation. Prototype results were analyzed by using DSO and Power Analyzer.

Index Terms **- Multilevel Inverter, PWM Techniques, Mathematical Modeling, THD analysis**

I. INTRODUCTION

Development and utilization of multilevel inverter has been done for higher voltage levels [1]. Power system stability of a distribution network get disturbed because of high penetration of renewable energy sources [2]. The conventional two level inverter functions at high switching frequency and requires high dimensional filters as the output voltage is in square wave shape [3]. Hence an additional cost is required to reduce power losses and bring total harmonic distortion (THD) in prescribed limit [4]. To get better output quality and efficiency multilevel inverters (MLIs) are act as a dominant solution [5]. For grid integrated application MLIs are having some advantages like, 1) nearly sinusoidal staircase output waveform, 2) comparatively small size filter required, 3) voltage stress on switch i.e. dv/dt reduces, 4) operates at low switching frequency so that switching losses reduced and get high efficiency and 5) reduces issues created by magnetic interference.

Multilevel inverter basically categories into three forms which includes neutral point clamped (NPC) [6], flying capacitor (FC) [7], [8] and cascade H-bridge (CHB) [5]. These topologies perform active as well as reactive power flow control and generate near about sinusoidal output waveform. However, clamping diodes required in large number for NPC-MLI which make it bulkier and costly. In addition to that NPC-MLI is having additional conduction losses and complexity which weakens power quality enhancement advantage. In a same way large number of capacitors are required in FC-MLI and of their charging and discharging control system becomes impractical. To get higher power and voltage level it is proven that CHB-MLI is more flexible than other topologies [9], where it is a series linking of output terminals of several H-bridges [10] [11]. CHB-MLI is having modular property because of that it is easy to fast to replace inverter cell having a fault [12] with an appropriate control technique.

On the other hand, there is an increasing demand of modulation method as a result of that various modulations techniques have been invented. Every modulation technique is having its own merits and demerits based on converter topology. [13] presents various modulation topologies of multilevel inverter on the basis of switching frequency. Pulse width modulation (PWM) technique is best suitable and appropriate for CHB-MLI [14], There are two types of PWM techniques based on carrier signal i.e. phase shift and level shift technique. To get a high quality output level shift PWM technique is widely used for different applications. The carrier signal used in this technique is of triangular and saw tooth shape on the other hand the reference signal is considered as a sinusoidal or trapezoidal shape is selected [15-17].

This paper proposes a cascade H-bridge multilevel inverter (CHB-MLI) having 5 levels in its output. The paper presents mathematical modeling of all three types of MLIs with circuit configuration and switching sequences. In addition, three carrier level shift PWM techniques i.e. In-Phase Nature (PD), In-Phase Opposition Nature (POD) and Alternate In-Phase Opposition Nature (APOD) are presented and implemented for 5 level CHB-MLI. The proposed CHB-MLI is built in MATLAB by using Simulink platform for 5 levels output of 20V. Output voltage and current total harmonic distortion (THD) get compared for different carrier level shift PWM techniques. The paper organized such that Section II contributes mathematical modeling of MLIs and their comparison, Section III presents simulations with result analysis of the proposed system. It also presents modulation

strategies and comparative analysis based on THD. Section IV shows the Hardware implementation and comparison of the proposed system with various PD level shift PWM techniques. section V is having conclusion continued with references

II. MATHEMATICAL MODELING OF MULTILEVEL INVERTERS

a. Classification of MLIs

Power electronic network which is used to change direct current (DC) in alternating current (AC) is called as inverter. Circuit configuration of basic three type of MLI is shown in Fig. 1. Where a) represents 5 level diode clamped MLI, b) Flying capacitor 5 level MLI and c) cascade H-bridge 5 level MLI. Primary classification of MLI is done on the basis of components present in its circuit.

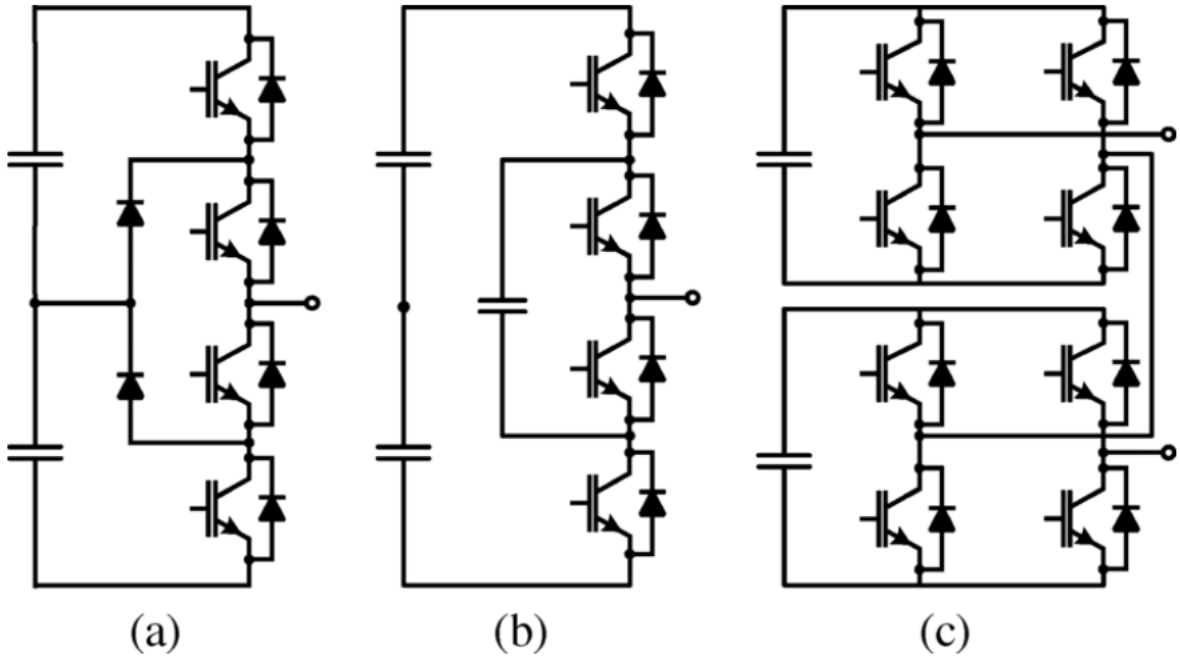


Figure No. 1 Circuit configuration of multilevel inverter topologies

As it is clearly shown in fig 1 a) that diode clamped MLI is having diodes to transfer specific amount of voltage to reduce stress on power switches. It is also called as neutral point clamped MLI. It is having a main drawback that it can give half of output voltage than the input voltage. Diode clamped MLI is used in compensation devices, electrical drives and system interconnections [6]. On the other hand, fig 1 b) shows flying capacitor MLI which is having capacitors which are connected in series to clamping switches. These capacitors handover controlling amount of voltage to switches. Here also the output voltage is half of the input voltage which act as a drawback of this type of MLI. FC-MLI is used in motors direct torque control application [7], [8]. Similarly, fig 1 c) shows 5 level cascade H bridge MLI which is having series connected H bridges. CHB MLI is also classified as symmetric and asymmetric based on DC source amplitude. If the DC sources are having same value, then it is called symmetric CHB-MLI and if it is having integral multiple dc source value then it is called asymmetric CHB-MLI [5].

b. Mathematical modeling of MLIs

Mathematical modeling gives details about required components in MLIs circuit configuration. Most of MLIs consist of controlled switching devices like thyristor, IGBT and MOSFET along with diodes and capacitors here capacitors act as a source of voltage. Normally diode clamed and flying capacitor MLIs having only one DC source this DC source get divided into small amount of voltages by using capacitors. Number of controlled switches, capacitors and diodes required for n level diode clamped MLI is calculated by using equation 1,2 and 3 respectively.

$$No.of\ Controlled\ Switches = (2n-2) \quad (1)$$

$$No.of\ Capacitors = (n-1) \quad (2)$$

$$No.of\ Diodes = [(n-1)*(n-2)] \quad (3)$$

Similarly flying capacitor MLI consist of auxiliary capacitors, controlled switches and capacitors as a sources. Required count of components for n levels is calculated by using equation 4, 5 and 6 respectively.

$$No.of\ Auxiliary\ Capacitors = \frac{[(n-1)*(n-2)]}{2} \quad (4)$$

$$No.of\ controlled\ Switches = (2n-2) \quad (5)$$

$$No.of\ Source\ Capacitors = (n-1) \quad (6)$$

Cascade H-bridge MLI consist of H-bridges. Every H bridge is having controlled switches and DC source. For designing a CHB-MLI it should be known about how many bridge, switches and sources required. Equation 7,8 and 9 gives an idea about number of bridges, controlled switches and DC sources count respectively for n levels.

$$No.of\ H-Bridge = \frac{(n-1)}{2} \quad (7)$$

$$No.of\ Controlled\ switches = 2*(n-1) \quad (8)$$

$$\text{No of DC sources} = \frac{(n-1)}{2} \quad (9)$$

Appraisal of MLI topologies based on its circuit configuration is presented in Table 1. It gives brief about number of components required for 5 Level MLI. From Table 1 it gets clear that to generate same level of output component requirement is less in cascade H-bridge MLI as compare to other two topologies.

In addition to that CHB-MLI don't have capacitor voltage balancing issue. In addition to that it is also found that CHB-MLI generate output double than that of the input DC source which is exactly opposite that of the two other MLI topologies. CHB-MLI is having simple circuit configuration and because of the its manufacturing and troubleshooting becomes easy and fast.

Table 1 Comparison of MLI topologies for 5 Levels

Parameter/ Topology	Diode Clamped MLI	Flying Capacitor MLI	Cascade H-Bridge MLI
No. of switches	08	08	08
No. of Diodes	12	00	00
No. of Capacitors	04	10	00

III. Simulation & Results

a. Modulation strategies

Pulse width modulation (PWM) is most widely used modulation technique in inverters. In this strategy a sinusoidal signal of frequency as required for output signal frequency is compared with repeating triangular signal having high frequency to generate switching pulses. Modulation strategies used for MLIs are categorized based on switching frequency such as, Fundamental converting frequency and high converting frequency.

Fundamental switching frequency PWM techniques include Space Vector Control PWM and selective harmonics elimination PWM techniques. On the other hand, high frequency PWM techniques include sinusoidal PWM of phase shift and level shift. In phase shift technique carrier signals get shifted on time axis and in level shift carrier signal get sifted on amplitude axis [13-15]. Level shift PWM technique is very easy for implementation and effective. Types of level shift PWM techniques is shown in Fig 2. It is shown that level shift PWM technique is having three types based on the nature carrier signal after shifting by an amplitude and form a shape.

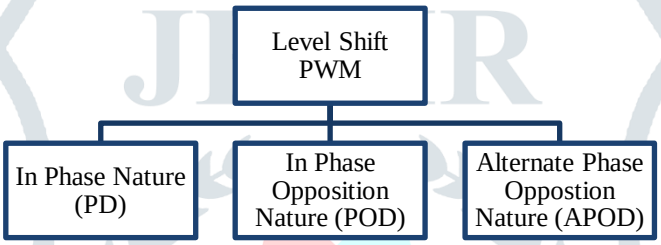


Fig. 2 Types of level shift PWM techniques

In this paper these three techniques applied to a 5 level CHB-MLI and check about its output voltage and current THD.

b. Simulation

The simulation of proposed 5 level CHB-MLI is done by implementing all three level shift PWM techniques in MATLAB-23 by using Simulink platform. THD analysis of MLI under various PWM techniques is produced. The proposed simulation model is shown in Fig. 3 (a) having two cascade H-bridges with two separate equal DC sources of 10 volts each. Therefore 5 level 20-volt output will be there which is shown in a fig. 3 (b). An output of 100-ohm resister is connected as a load to a proposed CHB 5 level MLI.

Applied modulation techniques such as PD, POD and APOD to generate pulses of the 5 level CHB-MLI are shown in fig 4 a, b, c respectively. This figure clearly shows that nature of carrier signal and its crossing with a reference sinusoidal signal which help to understand the switching pattern and sequence. Table 2 presents switching sequence and respective output voltage of the proposed 5 level CHB-MLI. Eight switches present in a circuit get switched according PWM produced sequence.

Table 2 Switching sequence and output voltage

S1	S2	S3	S4	S5	S6	S7	S8	O/P
1	1	0	0	1	1	0	0	+2V
1	1	0	0	0	0	0	0	+1V
0	0	0	0	0	0	0	0	0V
0	0	1	1	0	0	0	0	-1V
0	0	1	1	0	0	1	1	-2V

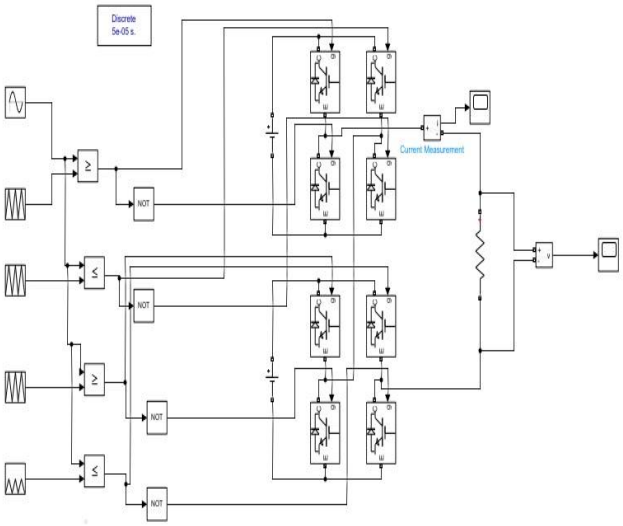


Fig. 3 (a) Proposed 5 level CHB-MLI

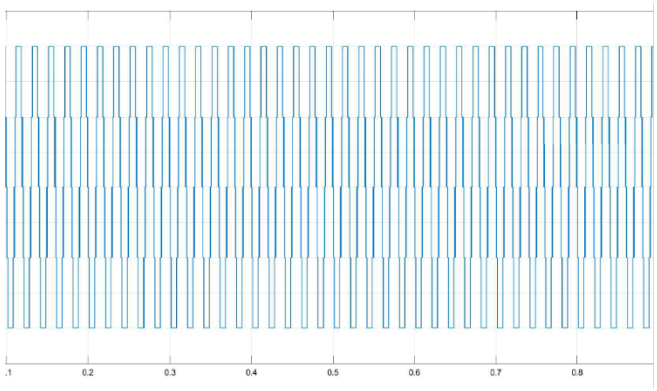
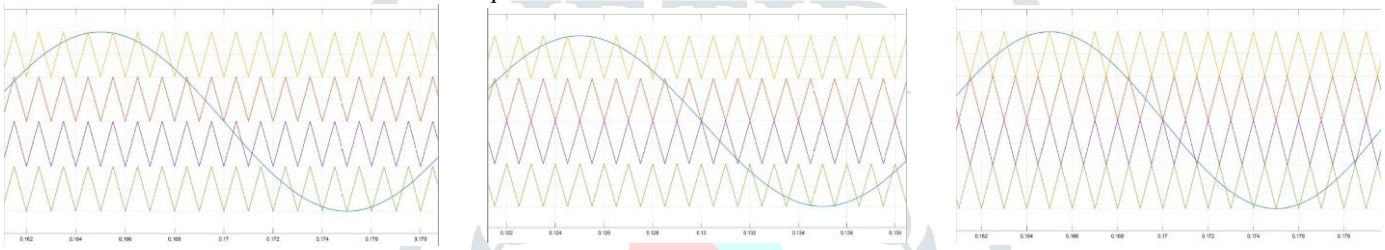


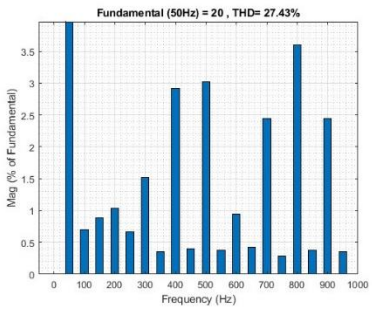
Fig. 3 (b) Output voltage waveform 5 level CHB-MLI

Total Harmonic Distortion (THD) analysis window in a MATLAB/Simulink is shown in fig 5. for output voltage and current of 5 level CHB-MLI with three modulation techniques.

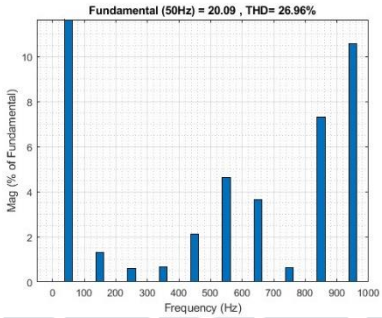


(a) PD (b) POD (c) APOD

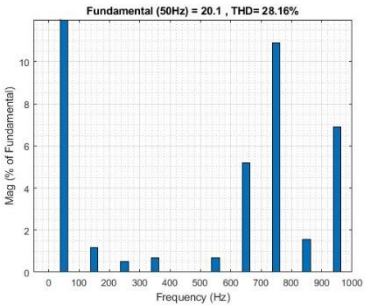
Fig. 4 Carrier level shift PWM techniques



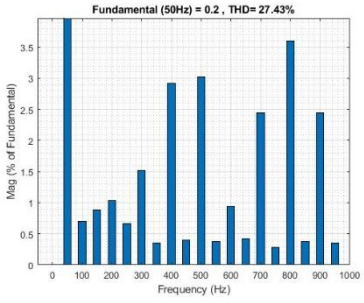
(a) PD Technique Voltage THD



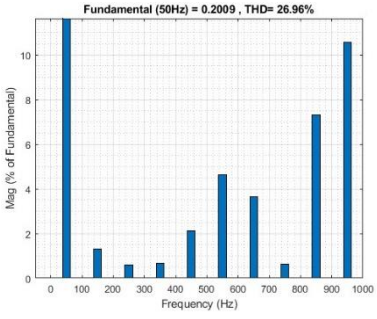
(b) POD Technique Voltage THD



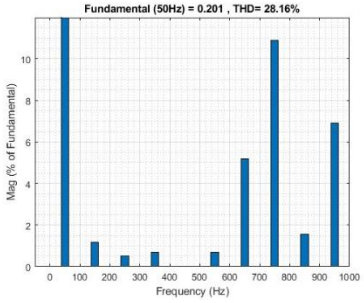
(c) APOD Technique Voltage THD



(d) PD Technique Current THD



(e) POD Technique Current THD



(f) APOD Technique Current THD

Fig. 5 THD Analysis of 5 Level CHB-MLI

It gets clear from the Fig. 5 that the THD of 5 level CHB-MLI with PD, POD and APOD technique is not in a IEEE prescribed limit. To bring it down in a limit it is essential to use a filter to convert stare case output waveform into sinusoidal waveform another alternative is to increase number of levels in an output signal. Table 3 shows comparative analysis of three level shift modulation techniques. From this comparative analysis it gets clear that POD technique is having low THD i.e. 26.96% in output as compare to PD and APOD as it is having 27.43% and 28.16% respectively. It is also observed that there is no difference in THD of voltage and current it is because of resistive nature of load. From implementation point of view PD-PWM is found easy to understand and implement as same waveform need to be level shifted only on the other hand other techniques are having different shape charrier with level shift.

Table 3 comparative analysis of level shift modulation techniques

Particular/Technique	PD	POD	APOD
Voltage % THD	27.43%	26.96%	28.16%
Current % THD	27.43%	26.96%	28.16%

IV. EXPERIMENTAL VALIDATION

A prototype model of proposed 5 level CHB-MLI is developed in a laboratory by using NPN transistor as a static switches and control pulses given through an Arduino Uno board. Performance of prototype tested at open circuit condition. The output voltage waveform is recorded by using digital storage oscilloscope (DSO). Fig 6 (a) shows prototype model of 5 level CHB-MLI with Arduino Uno board and driver IC. Fig 6 (b) shows the output voltage waveform in DSO. In an experimental circuit pot is used to adjust modulation index. Switching devices used here are TIP122 NPN transistors. DC4047BD IC is used to send pulses to switches. It can set width of pulse by using external register and capacitor. Driver circuit is having pot as a register and 100 V 1nF capacitor of 102J100. To limit current 100 ohms and 1k ohm registers are used. Center tap transformer is used to combine the output and step up in a proportion of 1:2. To generate a pulses reference signal is taken from an Arduino UNO. This reference signal gets compared with carrier signals by using IC DC4047BD which is having inbuilt multiplier.

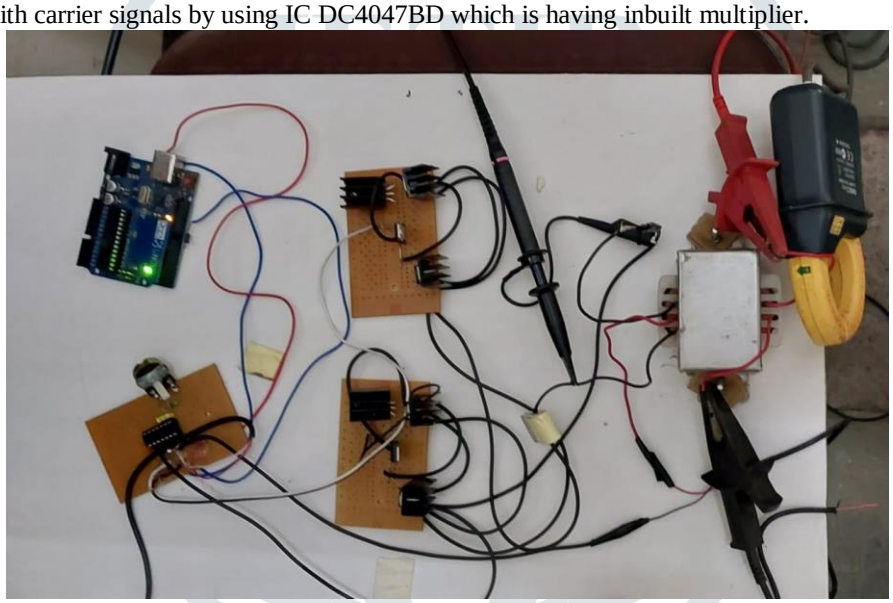


Fig. 6 (a) prototype model of 5 level CHB-MLI

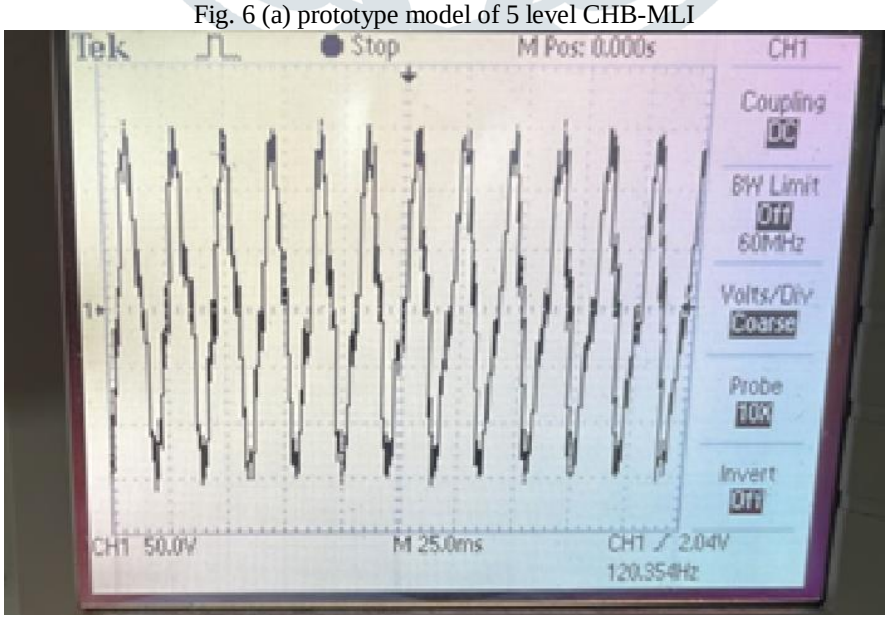


Fig. 6 (b) Output voltage of 5 level CHB-MLI

The output voltage is of about 50-volt amplitude as it gets stepped up from 24 volts. It is easy to see steps presents in a waveform. Thus the validation of results done by implementing a PD-PWM technique to 5 Level CHB-MLI.

V. CONCLUSION

This paper presents implementation and analysis of five level CHB-MLI with various carrier level shift PWM techniques. The proposed five level CHB MLI effectively tested for PD, POD and APOD modulations techniques by using MATLAB Simulink platform. Where the THD analysis is presented for all three modulation techniques on five level CHB MLI. It is found that POD technique is having low THD i.e. 26.96% in output as compare to PD and APOD as it is having 27.43% and 28.16% respectively. Simulation results validated by using a prototype model. From implementation point of view PD-PWM is found easy to understand and implement

Results of the MLI is in the form of stair-wave, thus to make it sinusoidal filter is required which is considered here as a future scope of this paper. Due to less component required CHB-MLI is become widely used for different industrial application and because of ease of implementation PD carrier level shift PWM technique is found best suitable CHB MLI. Detailed comparison has been presented in this paper about MLI topologies and PWM techniques and based on that comparison a prototype has be implemented for five level CHB MLI. From results it can be validated that the CHB MLI with PD modulation technique is best suitable for different applications

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