JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue

JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)

An International Scholarly Open Access, Peer-reviewed, Refereed Journal

CMOS VCO DESIGN FOR ADVANCE COMMUNICATION SYSTEM

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Abstract: Advance communication-based system requires very low power, current, voltage and wide frequency range for system design. This paper presents a design in the field of advance communication system. It presents 3 stage voltage controlled ring oscillator design on latest VLSI tools and reports transient, DC analysis of the system. The performance of voltage controlled oscillator (VCO) is of great achievement for advance communication system. Voltage controlled oscillators (VCOs) using three-transistor NAND gates have been designed in which new delay cell with three-transistor NAND gate has been used for designing the ring based VCO circuits. 3- Stage and 5 Stage VCO have been designed and compared on the basis of voltage and current. Output frequency has been controlled with variation from 1.8V to 2.4V. Three stage VCO shows output frequency variation in the range of 3.5GHz to 5.23 GHz whereas power consumption varies in the range of 545.45μW to 667.4 μW. Five-stage VCO depicts frequency in the range of 1.807GHz to 2.654 GHz with power consumption variation from 556.018μW to 990.3027μW. Power consumption, output frequency, and current have been obtained using latest 22nm technology.

Index Terms: VLSI, DC, VCO, MOSFET, EDA

I INTRODUCTION

Oscillators are the most important block in various advance communication based application. Every step of these technology data rates of transmission system are increasing day by day. In modern high performance device phase-locked loops (PLLs) are the commonly used circuit component with wide application in frequency synthesis, clock, and data recovery [1–3]. PLL block contains a phase detector, a charge pump, a loop filter, and voltage controlled oscillator circuit. VCO is very essential part of PLL circuit and design performance is affected here in terms of power consumption and phase noise. CMOS ring based oscillators accepted in PLL systems which can be implement using 3 stage and 5 stage ring form. These are also easier to integrate and provide wide tuning range. It is specialized oscillators in which the oscillation frequency varies with a control voltage. VCOs are used in many communication applications such as frequency modulation, in the phase locked loop (PLL) for signal tracking and FM demodulation. The paper focuses on the design of VCO for advance communication system. This work is based on the controlled oscillator circuit. Two important types of controlled oscillator are useful in electronics industries.

(A) Voltage Controlled Oscillator with a voltage control signal.

(B) Current Controlled oscillator with a current control signal.

VCO design for 22nm technology are based on incoming data signal with a clock recovery circuit to track clock rate. Its design is based on various parameters like center frequency, tuning range, sensitivity, spectral purity [5]-[8].

II PROPOSED DESIGN

Three stage voltage controlled ring oscillator using delay stages are shown in figure 1. Its last stage output is connected as a feedback input to the first stage. With a finite frequency range this oscillator circuit is generating periodic or analog signals. It is formed using 3 stage inverter circuit with oscillation phenomenon whereas oscillation formed using odd no. of stages. It is the basic condition for DC signal conversion. 360^0 phase shift of ring kind of VCO circuit is used here for designing and its voltage is also unity for alteration occurrence. The odd number of delay stages are must here for DC inversion of single-ended oscillation circuit. For VCO circuit design oscillation frequency for N stage would be $F_0 = 1/2Nt_d$, where total delay element is represented by t_d.
Basic building block to design the VCO circuit and improved design of this delay device can affect the total recital of the whole circuit [11]. In this reported work a new delay element has been implemented the significance of intake power of overall design, voltage, current, and frequency range.

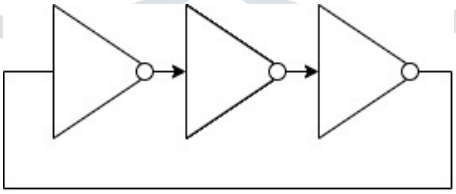

Figure 1 Three Stage Voltage Controlled Ring Oscillator

Figure 2 shows a CMOS VCO design using the current starved method. M4 & M8 are working as an inverter, M1 and M11 are using as a current source which limits the available current on M1 and M8. The MOSFETs M7 and M14 drain current are the same and set as an input control voltage [12]. These two MOSFETs are mirrored in each inverter. Here all PMOS transistors are connected to the gate of M7. All NMOS transistors are taking source voltage as an input voltage. Figure 3 shows five stage current starved VCO design method which is same as ring oscillator and functionality of it is also consistent to that in circuit PMOS13 and PMOS14 act as current source. The Oscillation frequency of current starved VCO (5 Stage) is given in eq.1

$$f_{osc} = \frac{1}{2NT_d} \qquad (1)$$

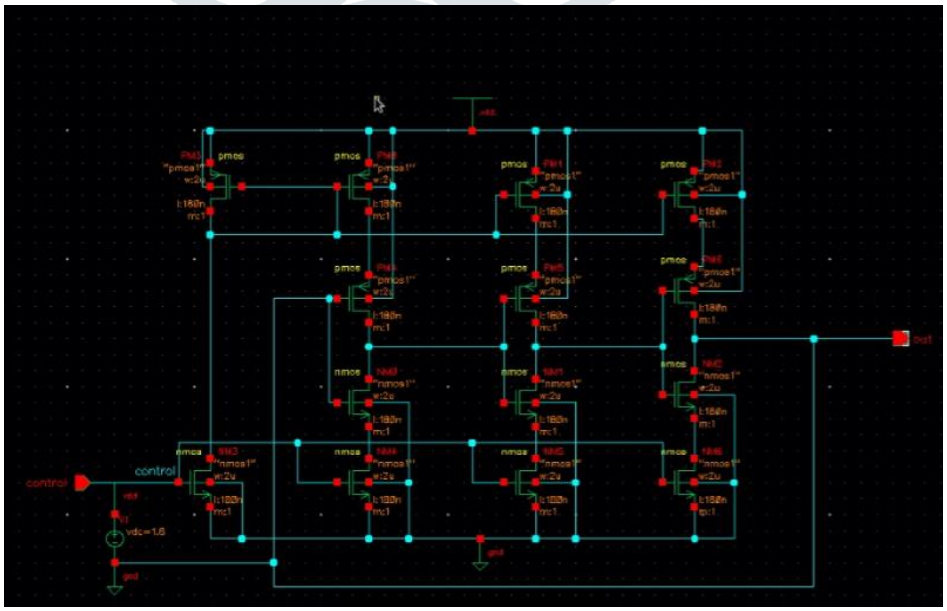

Figure 2 Three Stage VCO design on 22nm using Cadence tool

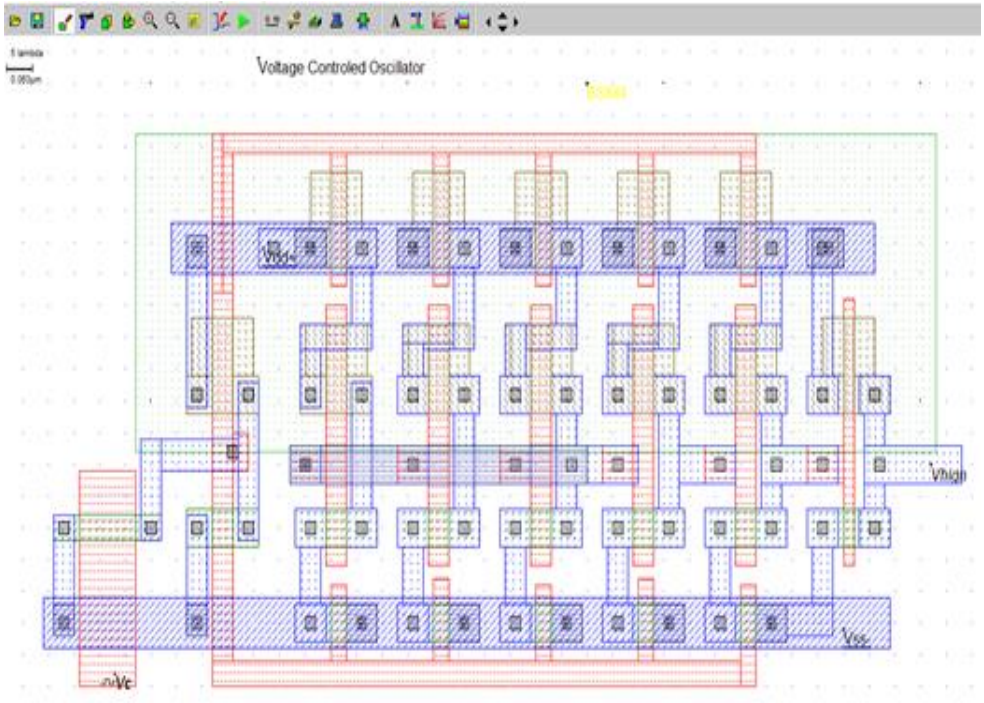

Figure 3 Five stage VCO design using 22nm technology

Where, N is the total no. of stages in a ring oscillator & T_d is the delay of each stage shown in eq. (2). Where Ceq is equivalent capacitor and Req is equivalent resistor of the system.

$$T_d = Ceq * Req \quad (2)$$

In general, VCO has output frequency as a function of applied control voltage which can be given in eq. (3)

$$Fout = F_0 + K_{VCO} V_{ctrl} \quad (3)$$

The total capacitance on drains of MOSFETs M_4 and M_8 is given by Eq. (1)

$$C_{total} = C_o + C_i \quad (4)$$

Where C_{total} the total capacitance on the drain of transconductance, Co is the output capacitance and C_i is the input capacitance. The frequency of oscillation of the current starved 3 stage VCO would be given in eq. (5)

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N.C_{total}V_{DD}} \quad (5)$$

Here N is the total number of stages and t_1 is output propagation for high to low delay time as well as t_2 is output propagation for low to high delay time [13-15]. The maximum VCO oscillation frequency F_{max} is determined by finding I_D when

$$V_{input} = V_{DD} \quad (6)$$

The average current of VCO depends upon VDD which is shown in eq. (7)

$$I_{avg} = \frac{Q_{Ctotal}}{t} = \frac{V_{DD}.C_{total}}{t} \quad (7)$$

Here in eq. (7) Q_{Ctotal} is the charge on C_{total}

Hence Power dissipation in current starved VCO is shown in eq. (8)

$$P_{avg} = V_{DD}.I_{avg} = V_{DD}.I_D \quad (8)$$

Here, P_{avg} is the average output power of the circuit.

III RESULTS & DISCUSSIONS

Output frequency is varying and controlled with the variation from 1.8V to 2.4V and in the 3 stage VCO design represents frequency variation in the range of 3.5GHz to 5.23GHz whereas power consumption varies in the range of 545.45μW to 667.4μW on the other hand five-stage VCO depicts frequency in the range of 1.807GHz to 2.654GHz with power consumption variation from 556.018μW to 990.3027μW. Table 1 shows the comparative analysis of power consumption, output frequency using 22nm technology on 3 stage and 5 stage VCO design.

Figure 4 and 5 represents transient analysis under the variable voltage and time period. It also shows the VCO start and stops time and used here for calculating the voltage, current and frequency parameters for the same design.

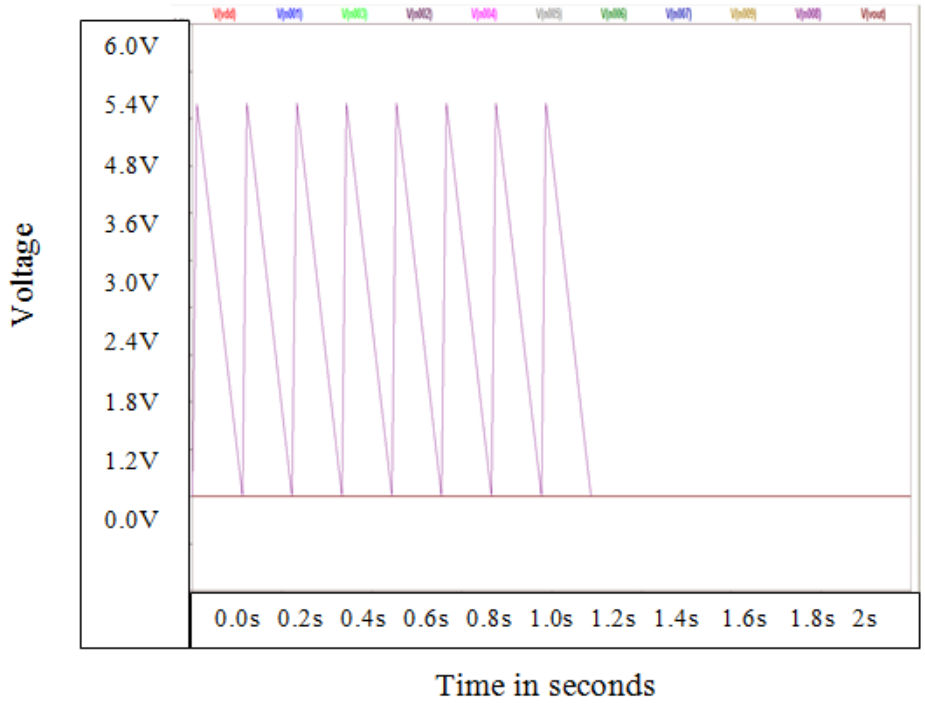

Figure 4 Transient analysis

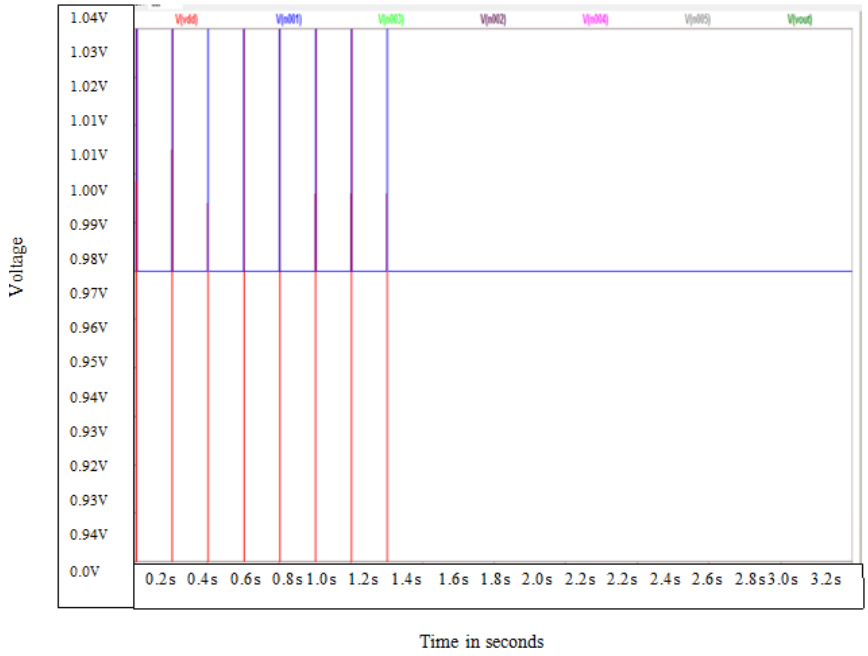

Figure 5 Transient analyses with variable time and voltage

Table 1 Comparative of five stage & three stage VCO design

S. No.	3- stage	5-stage
Technology	22nm	22nm
Control Voltage	1.8V to 2.4V	1.8V to 2.4V
Power Consumption	545.45μW to 667.4μW	556.018μW to 990.3027μW.
Frequency Range	3.5GHz to 5.23GHz	1.807GHz to 2.654GHz

IV CONCLUSION

Paper has been presented 3 stage and 5 stage VCO design and compared low power, voltage and current design in a wide range of frequencies for the latest research fields of advance communication, wireless network, and mobile communication systems. Implementation of design has been done on EDA tool; Cadence Virtuoso and it shows transient analysis of the design for variable time versus voltage.

ACKNOWLEDGEMENT

Simulation work has been carried out in VLSI laboratory of Electronics and Communication Engineering Department at Acropolis Institute of technology and research Indore MP. I am very grateful to AITR Indore teaching and nonteaching staff to support me during the research work.

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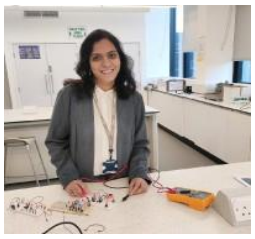
BIOGRAPHIES



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He has published 27 research papers in SCI listed journals and in reputed conferences. He is acting as referee for the International Journal of Electronics (U.K. based), he reviewed 10 papers. He supervised 11 no. of post graduate thesis and more than 20 no. of projects at undergraduate level. Research Scholar have completed Ph.D. under his supervision in area of Analog VLSI design. Under his guidance a Humanide serving Robot was developed by a team of faculty and students. This Robot was Installed at Indore Airport, it is a first such kind of robot installed at any Airport of India. Indore Airport authorities felicitated him on his achievement. Ongoing consultancy projects under his guidance are low cost Traffic Robot, Cleaning Robot, and Object Avoidance Robot.