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Comparative Analysis of Structured Design for Testability techniques

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Abstract – In the past, the designing and the testing of the IC had a huge gap, which was then bridged by the test engineering by developing and adopting a unified approach called "Design for Testability". The most important step for Testing any fault in an IC is to know where the problem exactly lies in the ICs, so the process of Fault localization is used for this purpose.However with the evolution of different IC testing methods there was an increase in testing and maintenance cost,Thus in such a situation where other methods have turned out to be less effective,BIST has provided improved efficiency with its shorter test application times and reduced cost

Keywords-fault model,test pattern generation.

I. INTRODUCTION

DFT offers an answer for the issue of testing sequential circuits. It's sort of difficult to test sequential circuits. Since there are clocks required alongside the flip-flops. In contrast to combinational circuits, we can't decide the result of sequential circuits by just looking into the inputs. Sequential circuits comprise limited states by virtue of flip-flops. The result likewise relies on the condition of the machine. It is difficult to control and observe the internal flip-flops externally. Subsequently, the state machines can't be tried unless a known value is initialized. Also to introduce them, we want a particular arrangement of highlights notwithstanding the ordinary hardware. DFT empowers us to add this functionality to a sequential circuit and accordingly permits us to test it.

II. METHODOLOGY/EXPERIMENTAL

Built In Self Test

The main components of BIST architecture requires the three hardware blocks and digital circuits. The hardware blocks are : a pattern generator, a response analyzer, and a test controller. It consist of System level, Board and a Chip. Every board consists of VLSI chips. System's level test manager's work is to continuously activate self-test on board. Test manager of board level's work is to activate self test on every chip of that board. A chip's test manager is liable for execution of self test and transmitting its result to the test manager of board.And the test manager from the board assembles test result from chip and give it to test manager of system level.Utilizing these results, the system test manager can confine defective chips and sheets.Fault coverage is a major issue in BIST designs.At the chip level, BIST includes the application of test patterns to the logic which can be tested and observation of the corresponding responses. The test engineer modifies on chip logic, using DFT technique such as scan, so that latches and flipflops can be controlled independently of the circuit's combinational logic[2].And for that CUT is used in most cases but not in all.CUT is circuit under test which consists of combinational logic,and the logic is arbitrate between pattern generator and response analyzer.

Transition Fault Model:It suppose thats the delay fault affects only one gte of circuit.A slow-to-rise fault and A slow-to-fall fault are the two types of fault connected with each gate of circuit.It is supposed that every non-faulty circuit have some delay. Delay faults result in increase or decrease of delay. In the transition fault model, the increased delay caused by the fault is conclude to be sufficient to prevent the transition from reaching any output at the time of observation.Especially, the delay fault can be noticed independent of whether the transition propagates through a long or a short path of output. Therefore, this model is also called the gross delay fault model[3].

Gate delay fault model:It suppose that the delay fault is put at one gate in the circuit. Unlike the transition model, the gate delay fault model does'nt suppose that increased delay will influence the execution independent of the propagation path through the fault site. It is supposed that increased paths through the fault site may affect the execution of circuit. The gate delay fault model is a quantitative model[3]. The gate delays are describe as either the worst-case values or intervals.

Path Delay Fault Model :In the path delay fault model a combinational circuit is observed faulty if the delay of any of its paths goes beyond the limit. A delay defect on a path can be consider by transmitting a transition through the path. Therefore, a path delay fault specification consists of a physical path and a transition that will be applied at the beginning of the path[3]. The delay of the path describe the addition of the delays of the gates and interconnections on that path.

Transition faults as well as gate delays faults describes single confined failures which cause the response of a gate to be slow compared to its specifications. As we discuss in transition fault model, that it is supposed that the increased delay generate by the fault is always sufficient to be observed on the output.And in Gate delay fault model, no inference is made on the size of faults.

The path delay fault model considers failures distributed along a path as well as single confined failures. From the above discussion, Transition and gate delay fault models are used for test generation, but they are mostly attractive for diagnostic purposes because they can have better accuracy than path delay faults. On the other hand, since path delay faults cover distributed failures as well as located delay defects, this model is more powerful for test pattern generation purposes.[4]

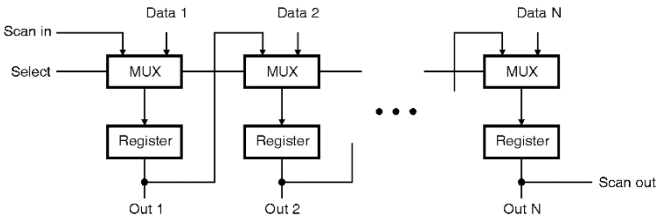
Scan Path

Scan path is generally created by the people designing the logic of the circuit. It can also be created by software during the process of IC synthesis, it is designed to test C in the most efficient way, without much effort.

Fault Modeling:The method is based on a two phase procedure. One being parallel exact critical path fault tracing to determine all "active" nodes with detectable stuck at faults. In the second phase reasoning is performed to know the physical defects. Parallel pattern single fault propagation (PPSFP) is widely used in combinational circuits for fault simulation. A lot of proposed fault simulators have PPSFP with the techniques as Test detect, critical path tracing and dominator concept. The Critical Path Tracing (CPT) is generally used as a fault free circuit by using binary values for backtracking from primary outputs to primary inputs to detect the faults. This continues until the chosen path gets non-sensitive or is at the very edge of the chosen network. CPT can find all the faults in a single run. Parallel critical path tracing in fanout free regions combined with parallel simulation of stem faults was investigated in [5].

Fault simulation is carried out in two phases: logic SAF simulation to determine the detected SAF faults, and mapping SAF faults to the physical defects. 1)First Phase: By using the basic logic level fault simulation, we use logic to determine the active node for the test pattern. This task of fault simulation can be referred to as calculation of Boolean derivatives. In order to extend the technique we use the concept of Partial Boolean differentials. After analysing the boolean values we get two tables i) Fault Table(FT) ii) Test pattern (TP). This data in the table can be used to map SAF faults. 2) Second phase: By using the already functional fault model we detect which physical defects are detected by the given test pattern. All the entries which we see in the FT are the ones with physical defects in the SAF. If any node variable, say *k* is active, then a defect d can be detected if the

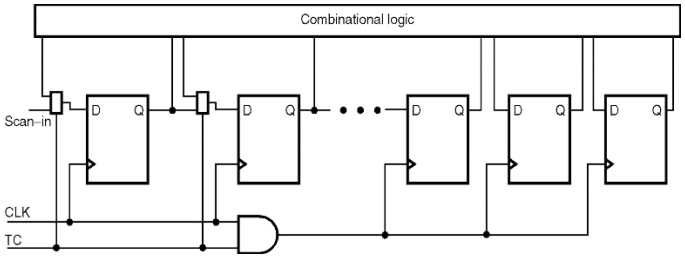
condition W(d,k) = 1 is fulfilled by the test pattern we considered. To find the conditions W(d,k) for a given defect d, we have to create the corresponding logic expression for the faulty function. Checking the conditions W(d,y)=1 is based on using data in PT.



Partial scan

In partial scan ,circuit is tested with help of flip flops which has registers and state machines. Partial scan technique is set on the idea of the structure of the resulting kernel of the modified circuit. these techniques were developed mainly to beat the world overhead which was found fully scan. Here scan testing signal determines whether we are visiting perform testing operation or normal operation.The complexity of test generation complexity for partial scan consisting of acyclic sequential circuits is proved to be one order greater than combinational circuits of full scan circuit kernel.however it had been observed that for various datapaths ,test genearation time of partial scan is over full scan whereas the fault coverage and fault efficiency remains same for both.

Morever to further reduce the hardware area overhead, the quantity of flip-flops to be converted into scan flip-flops are minimized. Thus to gain this goal several techniques may be used.In the[1],minimum feedback loops are broke which reduces the quantity of scan flip-flops. the following technique is H-scan which uses the present paths between registers, made from a series of multiplexers, thus further reducing the world overhead within the scan technique. In h-scan technique, some extra gates are added to the logic of the prevailing path in order that signals transfer between the registers is enabled by a replacement input independent on the signals from the controller.Orthogonal scan and partially strong testability method are few other scan techniques for testing provided they're applicable in datapath only.



III. CONCLUSION

In this paper, we compared and analyzed dft techniques like bist,scan path and partial scan on basis of parametes like test generation time,fault coverage and cost efficiency.Further we discussed different fault models.

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