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Survey on Design of CIC Decimator and Interpolator in Wireless Receivers

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Abstract: The advancement in Wireless communications has always led to the need of multi rate signal processing. Multi-rate signal processing plays a pivotal role in the field of wireless communication due to many reasons like its ability to improve its efficiency, flexibility, and performance in various aspects of signal handling. The computational complexity can be minimized; signal quality can be enhanced and easy adaptability to varied communication scenarios is possible by usage of different sampling rates. So should be the design of wireless receivers to adapt to different sampling rates where it is observed that Cascaded Integrator-Comb (CIC) filters play a pivotal role. CIC filters have multiplier-less architecture and are considered more efficient in decimation and interpolation which make them perfect for high-speed digital communications. This review not only highlights the relevance, design enhancements, and application of CIC filters in meeting the growing demands of next-generation wireless technologies but also focuses on the estimation of other hardware resource parameters to evaluate their performance.

Index Terms **- Multi rate signal Processing, CIC filter, decimation, interpolation, wireless communication.**

I. INTRODUCTION

In modern wireless communication systems, multi-rate signal processing is a fundamental requirement for converting between different sampling rates—especially in digital receivers and transmitters. **Cascaded Integrator-Comb (CIC) filters**, introduced by Eugene Hogenauer in 1981, is a class of hardware-efficient linear phase finite impulse response (FIR) digital filters in terms of multipliers and adders. As it offers to perform **decimation** (rate reduction) and **interpolation** (rate increase) without multipliers.

Its frequency response is tunable, by selecting the appropriate number of cascaded integrator and comb filter pairs. The CIC filter first performs the averaging operation, then follows it with the decimation. The transfer function of the CIC decimation filter in z-domain is given in equation (1).

$$H[z] = H[z]_I^N . H[z]_C^N = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} = \left(\frac{1-z^{-RM}}{1-z^{-1}}\right)^N \qquad (1)$$

In equation (1), N is the number of stages, R is the sampling frequency conversion factor and M is the differential delay usually 1. The numerator $(1-z^{-RM})^N$ represents the transfer function of the comb and the denominator $1/(1-z^{-1})^N$ indicates the transfer function of an integrator. A simple block diagram of a first order CIC decimation filter and CIC Interpolation filter is shown in Fig.1(a) and Fig.1(b) respectively.

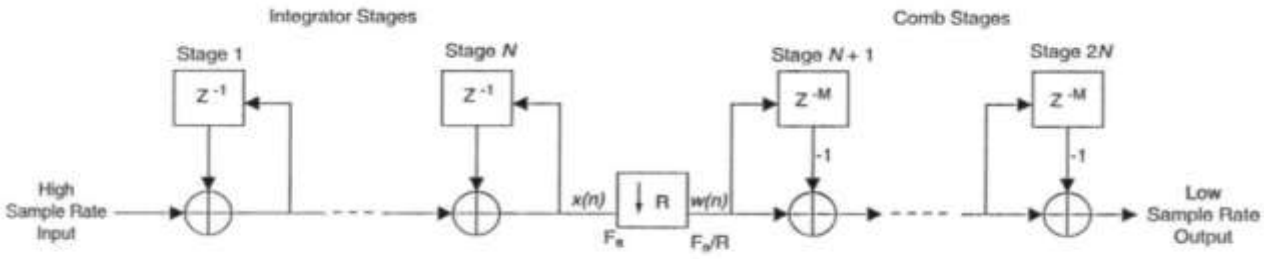

Fig. 1(a). Block diagram of CIC Decimation filter

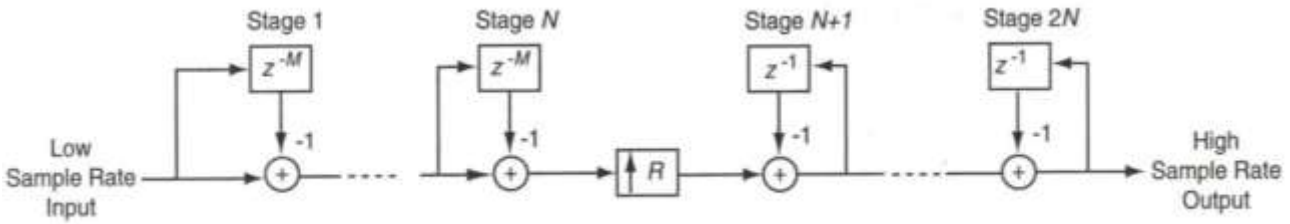

Fig. 1(b). Block diagram of CIC Interpolation filter

The CIC decimation filters play a major role in the wireless receivers for many reasons. Initially by reducing the sampling rate at the receiver end, these reduce the computational burden on the successive processing steps like channel filtering and demodulation. As the processing load reduces, the power consumption is also minimized which is making it more suitable for battery powered devices frequently used in wireless devices. CIC filters are simple, making them cost-effective on terms of design complexity and hardware resources. CIC filters are also adaptable to different wireless standards with different channel bandwidths as they can be designed for a wide range of decimation factors.

Though the CIC filters have significant advantages they do come with limitations like Passband Droop, Poor stop band attenuation, Limited frequency selectivity, Delay and Phase distortion, Word Growth and Overflow and Inflexibility for non-integer decimation.

However, traditional CIC filters suffer from significant passband droop and poor stopband attenuation, especially at higher decimation ratios. To overcome these issues, hybrid CIC decimation filters have emerged, combining CIC cores with auxiliary filter structures or arithmetic optimizations to balance performance with efficiency.

The review paper is organized in five sections. Section I introduces the basics of CIC filter and its role in multi rate signal processing i.e., sample rate conversion with respect to wireless communication receivers. Section II provides details of various CIC based decimators and interpolators. Section III encloses the analysis of different CIC filters-based sampling rate converters where their methodologies and performance metrics are compared. Section IV discusses Performance metrics and their related comparisons. The Section V gives the conclusion.

II. Literature Survey

In [1] Zhang et al proposed the design of CIC filter with compensation filter having inverse magnitude response to that of CIC filter to improve its passband and transition band features. A normal CIC filter is equivalent to a number of rectangular windows in cascaded recursive filter form, and thus has some prominent limitations like low attenuation and passband droop which is dependent on the decimation factor and the number of the section in cascade. To improve the performance in terms of magnitude drop compensation filters having magnitude response as sine compensator and cosine filters are proposed.

In [2] Dolecek et al presented a new two-stage CIC decimation filter for the signals which occupy ¾ of the digital band. Assuming an even decimation factor M, the decimation filter's first stage decimation factor is considered as M/2 and the second stage as 2. Sine based compensator filter was introduced to decrease the passband drop of the CIC filter and a cosine filter to improve the overall stopband characteristics. This resulted in an improved signal to noise ratio (SNR). Polyphase decomposing method of comb filter is used and the polyphase components of the comb filter are moved to the lower rate which is M/2 less than the input rate. The proposed filter uses only additions/subtraction to perform decimation which makes it more suitable for software radio applications.

In [3] Li et al presented a paper on Compensation method for CIC filter in Digital Down Converter which proposed a method with the structure of polyphase decimation FIR filter to attain wide broadband compensation of the CIC filter and sample rate conversion. The main attention is on the use of FIR filters for compensation.

In [4] Stephen et al presented a paper on "High Speed Sharpening of Decimation CIC filter" where an existing technique was modified. The existing method compensated passband droop in the frequency response of CIC filter for power of two decimation factor. The new techniques delivered passband droop correction comparable to the previous method, also allowing better operation than the existing system by moving the integrator away from the filter input. A sharpened technique by Kaiser and Hamming was used which allowed programmable FIR filter to be replaced by a constant co-efficient FIR filter. Though this resulted in an increased hardware consumption by the CIC portion, but has led to an overall efficient hardware solution. The hardware implementation of both CIC and sharpened filters resulted in a series of integrators running at the high sample rate. As these sections are recursive, they cannot be pipelined, thus limiting the critical path to one adder operation. Non-recursive structures can be pipelined (at bit-level for increased speed) thereby reducing the critical path to a fraction of an arithmetic operation and allowing the circuit to be clocked at a faster rate. In the proposed method a partial non-recursive structure is obtained by factorizing the CIC filter transfer function.

In [5] Qingxiang Zhang et al have introduced a Digital Down Conversion model which is based on orthogonal mixing. Here the digital mixer produces an output which is the sum and difference of frequencies. Further these outputs are given to CIC, CIC Compensation and PFIR filters. The main function of these devices is suppressing both the image spectra and noise present in the aliasing bands, and also to maximize the received SNR.

III. Analysis of Various Designs of CIC Decimation/Interpolation Filters

In this field the researchers have identified solutions to overcome the limitations. The following section gives a complete overview of the different solutions provided.

Table 1 Comparison of various designs of CIC Decimation/Interpolation filters

Author	Methodology	Remarks
Vishal Awasthi and Krishna Raj [6]	Developed a hardware-efficient narrow-band filter for decimation/interpolation, using a CIC + compensation FIR structure.	Passband response improvement: ~26.6% boost in the band of interest Hardware savings (compared to direct FIR-only decimator): • Multiplications per input sample reduced by ~12.3% • Additions per input sample reduced by ~23.4% Gate-level resources: • FIR-only: ~1,265 multipliers, 1,264 adders • CIC + compensator: only ~103 multipliers, 105 adders.
Srivastava et al. [7]	Proposed a signed-digit-based FIR compensation filter. This filter leverages the redundant number system to reduce computational load and improve hardware performance.	• 17.27% reduction in passband droop • 12.29% improvement in folding band attenuation • 10.44% decrease in LUT (Look-Up Table) usage compared to traditional designs.
Gautam et al.[8]	Introduced a decimation filter optimized for flat passband characteristics using linear programming optimization (LPO)	• Minimized passband droop: Achieved a droop of less than 0.007 dB. • Elimination of compensator filters: Thanks to the high-quality magnitude response directly from the LPO design. • Significant reduction in computational complexity: Demonstrated a 50.5% decrease compared to conventional filter designs.
Supriya Aggarwal and P. Meher [9]	Introduced novel CIC-based decimation filter architectures designed to improve magnitude response while maintaining low hardware cost Hybrid Sharpening Structures: Two filter structures are proposed, both using a cascade of sharpening stages: • Structure I combines Kaiser-Hamming (KH) and Saramäki–Ritoniemi (SR) sharpening. • Structure II uses a two-pass SR sharpening scheme for enhanced alias rejection.	• Structure I achieves low passband droop and adequate alias rejection, making it suitable for general applications. • Structure II enhances alias suppression further, though at a slight cost to passband droop.
Zhikun He et al.[10]	Addresses performance bottlenecks in CIC filter implementations for sigma-delta analog-to-digital converters (ADCs), focusing on enhancing power efficiency and speed	Hybrid CIC Filter Design: • Operates at 625 MHz, designed using 28nm CMOS technology. • Features: 3-bit input, 4-stage cascade, and decimation by 8. • Achieves 41.69% power reduction (to 0.2607 mW) compared to traditional recursive CIC filters. • Area overhead is modest at 10.8%. Non-Recursive CIC Filter Design: • Optimized for high-speed operation at 2 GHz. • Also designed with 3-bit input, 4-stage cascade, and decimation by 8. • Introduces an extraction multiple allocation strategy for better performance. • Offers 3.2× speed improvement and operates at 0.9493 mW, with only 5.33% area increase.
Babic, Vesma, and Renfors [11]	A novel architecture for sample rate conversion, specifically addressing irrational or fractional decimation ratios—a key requirement in multi-standard communication receivers	• The system uses two parallel CIC filters to compute values that are immediately before and after a desired output sample. • A linear interpolation filter then generates the final sample, effectively enabling decimation by irrational factors.

		• The interpolation is performed at the high input sampling rate, preserving precision and reducing complexity.
Debarshi Datta and H. Dutta [12]	Reconfigurable Architecture: The authors introduced a pruned CIC decimator which minimizes unnecessary hardware operations, leading to reduced slice usage and power consumption. Partitioned Decimation Factor: By applying a partitioning technique to the decimation factor, they achieve notable reductions in computation time.	The three-stage CIC design shows: • 39.84% reduction in slice registers • 16.17% power savings compared to conventional designs.
Abinaya et al.[13]	The paper investigates the integration of various parallel prefix adders (PPAs) into the CIC structure—such as the Brent-Kung adder, which outperforms others in terms of FPGA resource usage and speed.	Brent-Kung based CIC achieved: • 41.67% LUT reduction • 34.78% power savings compared to traditional CIC. Signal Quality Enhancement: The authors introduced a new polynomial method that further improves filter response: • 33.33% reduction in passband droop • 41.14% reduction in stopband ripple compared to sharpened CIC variants.
S. Kim et al.[14]	CIC filters, though computationally efficient and commonly used for decimation and anti-aliasing, inherently suffer from passband roll-off, which negatively impacts the flatness of the receiving filter and degrades overall receiver performance.	• The authors present a CIC roll-off compensation filter specifically tailored for W-CDMA systems. This filter is designed to correct the amplitude distortion introduced by the CIC filter without compromising computational efficiency. • The compensation filter is designed as a FIR filter optimized to counteract the CIC's frequency response. • The method ensures the flatness of the overall response in the signal band, improving receiver sensitivity and performance.
Latha et al. [15]	MSDF (Multi-Standard Decimation Filter): Uses traditional CIC filters in early stages, designed for GSM and WiMAX signal reception. Polynomial-CIC-based MSDF: Incorporates polynomial CIC filters for improved flexibility and standard compatibility. Polyphase-CIC-based MSDF: Focuses on area and power efficiency, optimized for FPGA implementation.	Polyphase MSDF architecture: • 32.11% area reduction over traditional MSDF. • 28.57% dynamic power saving vs. polynomial MSDF. • 15.5% speed increase vs. polynomial MSDF.
V. Jayaprakasan, S. Vijayakumar, and P. Vyomal Naishadh kumar [16]	Proposes an efficient two-section CIC-based decimation filter for WiMAX systems, focusing on improved magnitude response, reduced power consumption, and hardware efficiency on FPGA. Dual-stage CIC design: Decimation factor M split into M1 and M2enabling: Improved passband droop and stopband suppression when M1<M2. Lower power consumption when M1>M2 Additional improvements through sharpening, zeros distribution, and a compensation filter in stage two.	When using M1<M2 configuration: • Passband droop improves by ~38% (for M=8). • Stopband attenuation increases by about 33%. • Power consumption minimized when M1>M2
Pu Wang, Yuming Zhang, and Jun Yang [17]	Hogenauer "cut-off" truncation: Applies bit-width truncation at each stage using Hogenauer's theory, optimizing resource usage without significant performance loss Combines multiple optimized CIC stages to form a multi-level architecture, balancing filter performance and hardware	• Significant reductions in logic usage (LUTs/registers) compared to traditional CIC filters with fixed register widths. • Despite truncation, the filter maintains desired frequency response characteristics (passband and stopband) with negligible degradation but for low frequency signals.

	complexity Unlike fixed-width registers in classic CIC implementations, this design tailors each stage's bit width to actual signal requirements, reducing resource waste.	• Architecture supports easy extension and adjustment of filter levels and register widths to meet varying system requirements.
Rajesh Mehra and Rashmi Arora [18]	Introduce a multiplier-free, high-speed CIC decimator tailored for wireless systems such as SDR (Software Defined Radio) and GSM, optimized for FPGA implementation. Implements a fully pipelined CIC decimation filter using only additions/subtractions, eliminating multipliers. Leverages embedded LUTs within the FPGA to boost operational speed while reducing logic resource usage.	• Multiplier-less CIC design enables fast, low-power decimation with minimal FPGA resource consumption. • Fully pipelined architecture and LUT-centric strategy deliver high throughput (~277 MHz), making this design ideal for real-time wireless and SDR signal processing.

IV. Performance Metrics

The previous section gives a complete overview of the enhancements made in the design of CIC decimation and interpolation filters. In this section the comparison of the above designs is done in two levels i.e., based on the performance parameters of the filters and the hardware resource utilization.

Table 2 Comparison based on Passband ripple and Stopband Attenuation.

Paper	Decimation Factor	Passband Ripple	Stopband Attenuation	FPGA / Hardware Resource Usage
Awasthi & Raj (2021)	64	Improvement: 26.57% vs uncompensated CIC	Not explicitly quantified	Complexity reduced: 12.25% MPIS, 23.4% APIS
Srivastava, Raj & Kumar (2022)	4–16	Avg. ripple reduction: 17.27%	Avg. attenuation improvement: 12.29%	LUT usage reduced by 10.44%
Gautam, Khare & Shrivastava (2021)	32 (M1=4, M2=8)	$\leq$ 0.007 dB	$\geq$ 44.91 dB	Complexity: 93 APOS (50.5% lower)
Abinaya, Maheswari & Jebaraj (2025)	16	0.12 dB	81.17 dB	Kintex-7: 1260 LUTs, 840 FFs, 0 DSP
V. Jaya Rakasan, Kumar & Kumar (2019)	32	0.05 dB	74.35 dB	Spartan-6: 754 slices, 28 DSP, 876 FFs

Table 3 Comparison based on Area & Power

Paper	Technique	Platform	Area metric	Power
He et al., 2022	Non-recursive CIC (high-speed, low-power)	ASIC (design-level report)	Area +5.33% vs. recursive baseline	0.9493 mW @ 2 GHz
Datta & Dutta, 2022	Reconfigurable DDC (polyphase CORDIC + multirate/HB + Farrow)	Xilinx Kintex-7 FPGA (xc7k160t-2fbg676)	Slices: 169 (proposed) vs 1238 (ref.); LUTs: 276.6 MHz fmax (proposed)	0.970 W (proposed) vs 1.446 W (ref.)

V. Conclusion

To summarize, the evolution of wireless communication systems continually drives the demand for efficient multi-rate signal processing techniques, with Cascaded Integrator-Comb (CIC) filters standing out as a key enabler. The multiplier-less architecture of CIC filter offers significant advantages in terms of speed, hardware simplicity, and power efficiency, making them ideal for decimation and interpolation in wireless receivers. By adapting to varying sampling rates, CIC filters support flexible receiver architectures capable of addressing diverse communication scenarios while maintaining low computational complexity and high signal quality. Recent advancements in CIC filter design including architectural optimizations and hardware implementations — not only enhance their performance but also ensure their viability in meeting the stringent area, power, and throughput requirements of next-generation wireless systems. This positions CIC filters as a cornerstone technology in the pursuit of scalable, high-performance, and resource-efficient signal processing solutions.

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