45nm Technology Based 8-bit ALU Design using Multiplexers and Decoder

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Abstract
This paper proposes 8-bit ALU with low power designed using 45nm technology. The proposed ALU consists of decoder, data selectors, full adder and some other logic gates such as AND, OR, NAND and XOR, which are used to perform the logical operations. It consists of two sub modules, they are arithmetic unit and logical unit. The arithmetic unit consists of one 4×1 mux and a full adder. The full adder takes the input from 4×1 mux and produces two outputs carry and sum. The logical block consists of one 2×1 decoder whose output is connected the four logical gates out of which one operation will be selected by the 4×1 mux which is the logical output. these ALU has been broadly used in central processing units, micro processors and micro controllers etc. The proposed ALU consumes very less power that is in the order of Pico watts.

I. INTRODUCTION

Most of the processor procedures are performed using one or more ALUs. An ALU loads data from the registers, an external control unit then tells the ALU what is the operation to be performed on the data and then the output is stored in the output register. The 8-bit ALU is designed in the Cadence Virtuoso software and is implemented in 45nm technology. The main objective of the project is to design 8-bit ALU and verify different operations of arithmetic and logical unit. The design consists of two blocks one is arithmetic block and the other one is logic block. The arithmetic or logic operations can be selected with the help of a selection line. The arithmetic unit consists of a 4 is to 1 mux and a full adder. The logical block consists of a 2 is to 4 decoder, logic gates like NAND, AND, OR and XOR gates and a 4 is to 1 multiplexer. The inputs for the 2 is to 4 decoders are the selection lines s0 and s1, the four outputs of the decoder are given to the four logic gates, the four outputs of the logic gates are given to the 4 is to 1 whose output is nothing but the output of the logical block. We first designed the decoder, multiplexer, all the gates in transistor level and then extracted the symbol. With the use of all the symbols we designed one-bit ALU from which we extracted the symbol and finally implemented an 8-bit ALU. The performance analysis is done with respect to power, delay and power delay product.

II literature survey: Current ALU [11] is planned using 180nm expertise but the proposed ALU uses 45nm technology which reduces the power feasting, delay and increases the performance. Design and optimization of 8 bit ALU using revocable logic provides delay of 5.52ns.Implementation of Low Outflow and High Performance 8Bit ALU for Low Power Digital Circuits consumes power of 0.7786 µW and provides a delay of 21.8ps and the power delay product is 16.97x10-18J.Design, analysis and performance comparison of GNRFET based adiabatic 8-bit ALU consumes power of 38.75mW .VHDL implementation of 8-bit ALU consumes 38mW with a delay of 13.58ns and power delay product of 516.04 x10-12 J .Multi-level approaches to low power 8 bit ALU design with power of 54mW delay of 5 ns and power delay product of 270 x10-12 J. Design of High Speed, Area Optimized and Low Power Arithmetic and Logic Unit with power 27 µW delay 76 ns and power delay product of 2.052x10-12 J .Proposed System with power consumption of 136pW and a delay of 60.0ps along with power delay product 8.16x10-24J

3.1 CIRCUIT DESIGN OF ALU:

The truth table for ALU is shown in the table below. For the different combination of inputs it performs different operations as shown below.

S0	S1	S2	output
0	0	0	Decrement
0	0	1	Increment
0	1	0	Addition
0	1	1	Subtraction
1	0	0	NAND
1	0	1	AND
1	1	0	OR
1	1	1	XOR

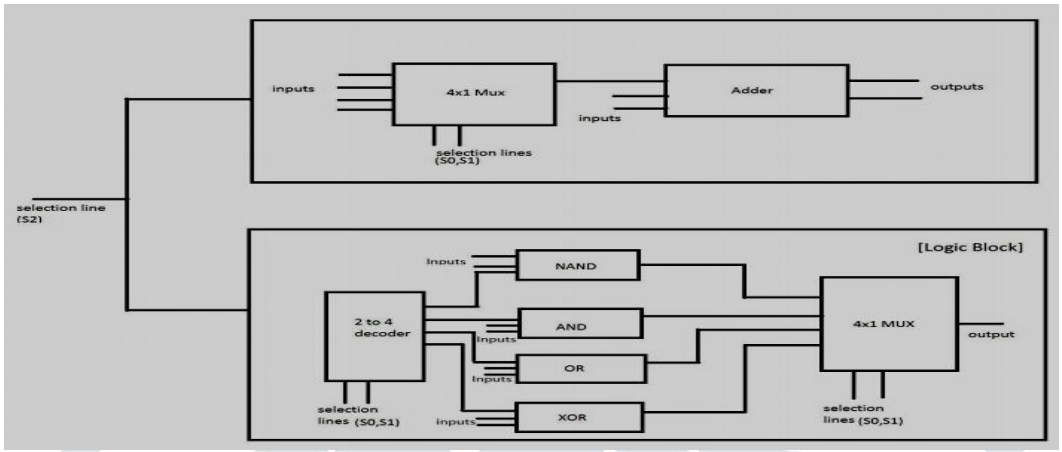


fig. proposed block diagram

3. SIMULATION AND WAVEFORMS:

FULL ADDER

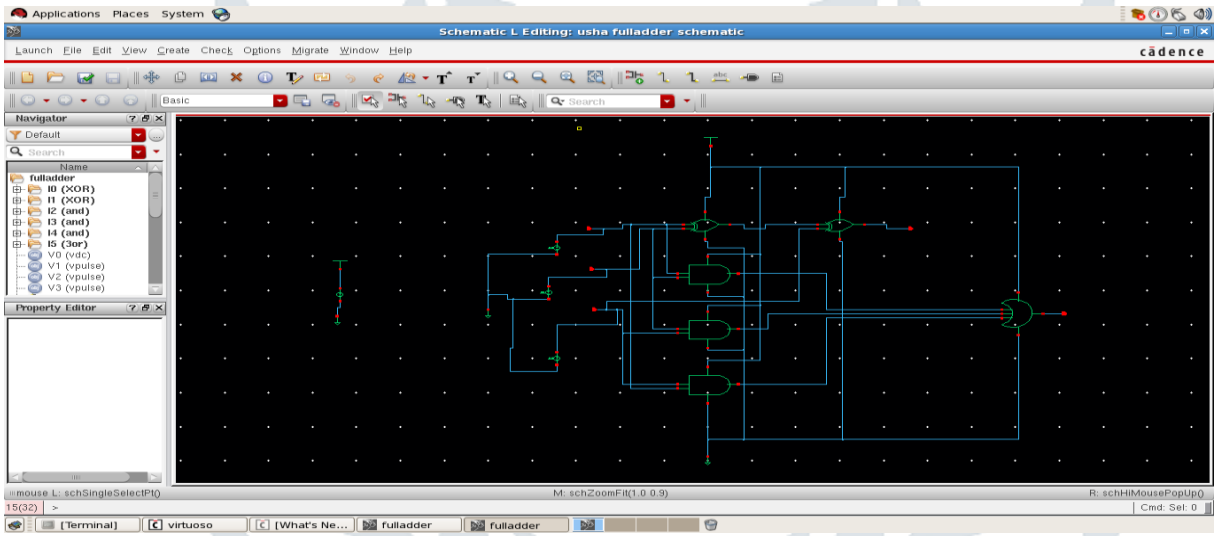


fig. full adder

Full Adder Truth Table:

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

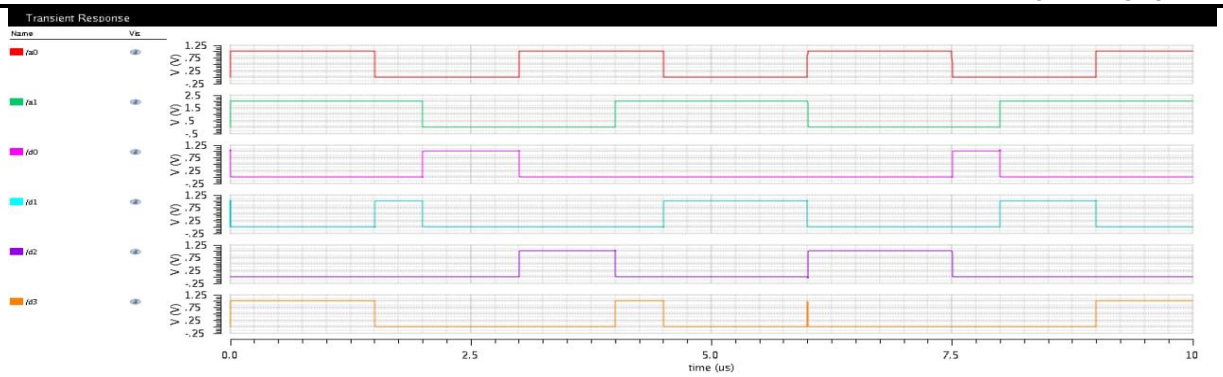
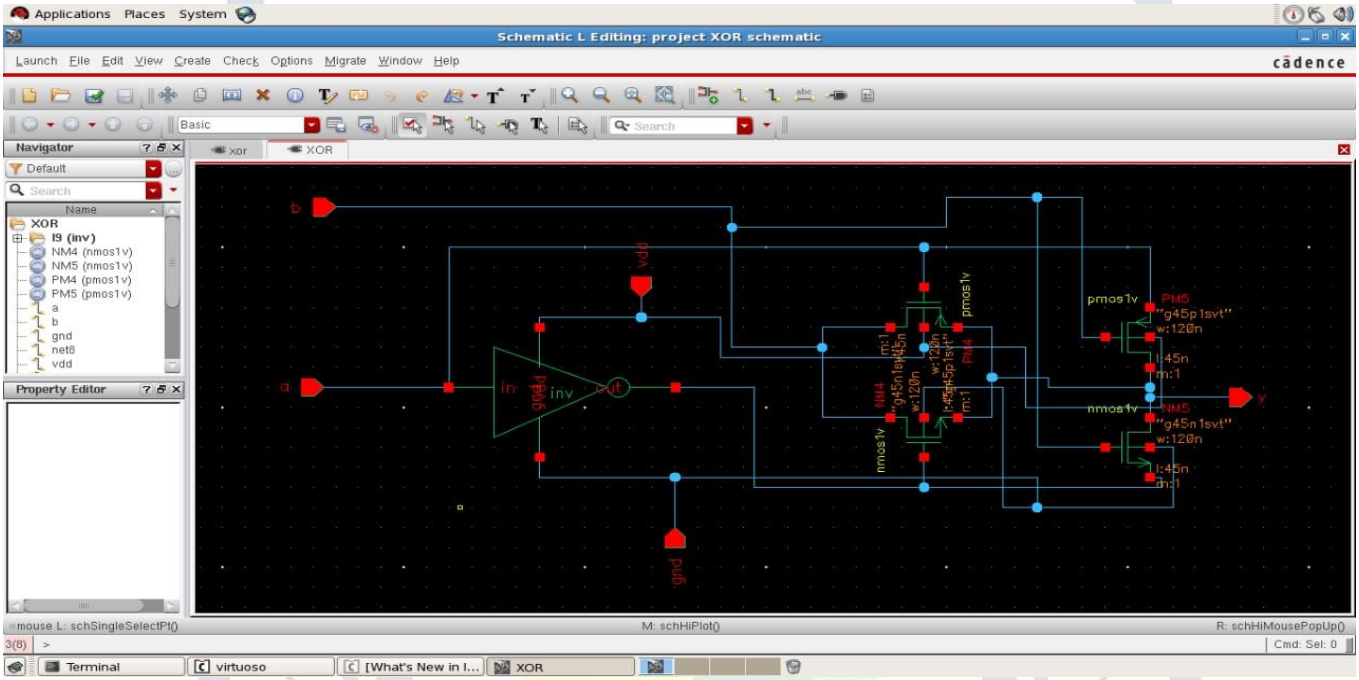


fig. output waveform

XOR:

An XOR gate can be constructed using MOSFETs. The ALU is implemented by using full adder. The basic component of full adder is XOR gate.



The R_{ss} current prevents shunting current directly from "A" and "B" to the output. Without it, if the circuit that provides inputs A and B does not have the proper driving capability, the output might not swing rail to rail or be severely slew-rate limited. the R_{ss} current also limits the current from $V_{dd\ to}$ ground which protects the transistors and saves energy when the transistors are transitioning between states.

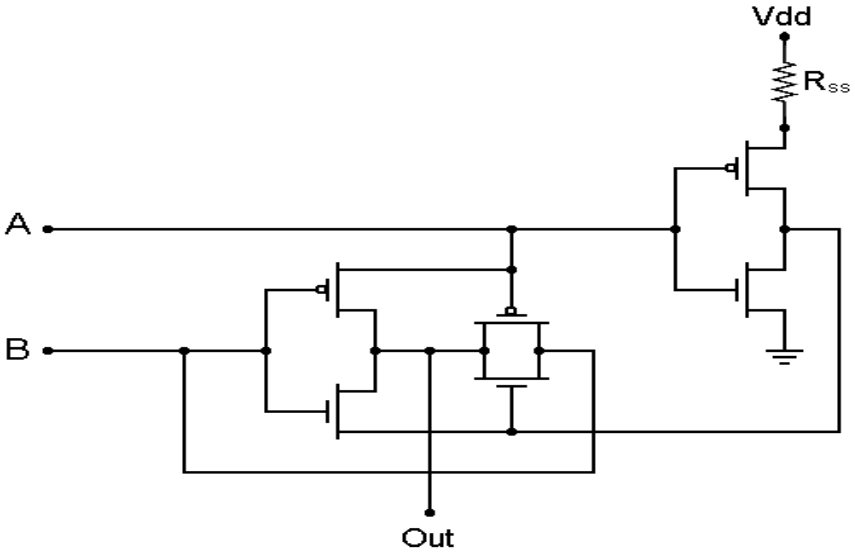


fig. XOR using transistors

2 TO 4 DECODER

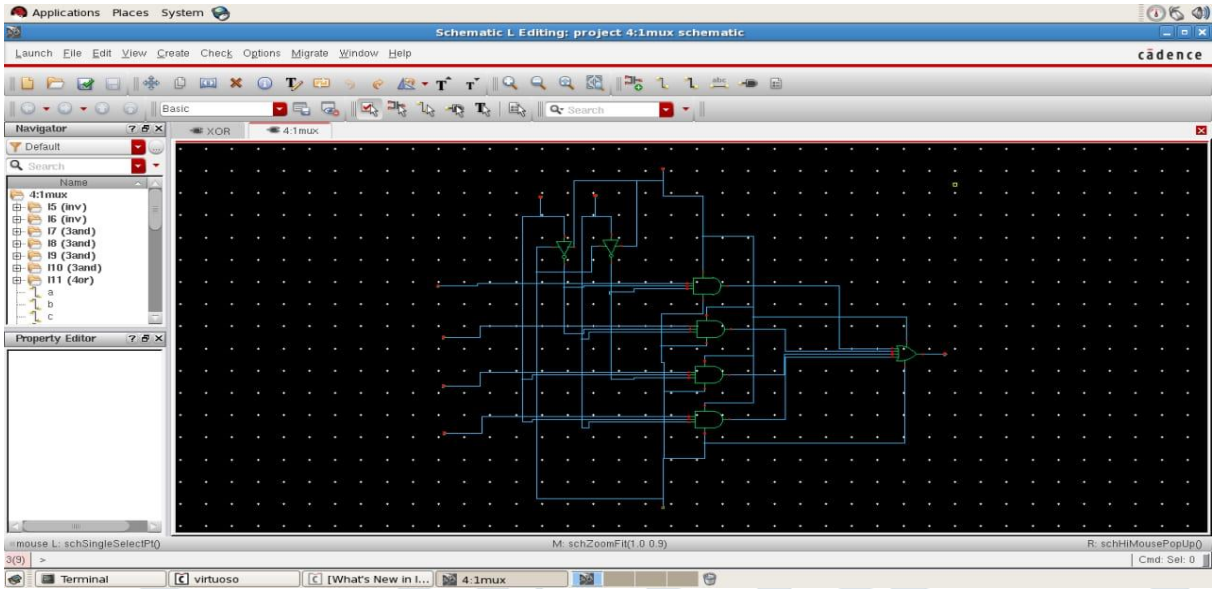


fig. circuit of decoder

A decoder may be a multiple input, multiple output logic circuit that changes codes input into coded outputs, wherever each the inputs and outputs square measure dissimilar for example n-to-2n, and binary coded decimal decoders. Decoding is important in applications like knowledge multiplexing, memory address secret writing, and seven phase show. The best example of decoder circuit would be AN AND-gate as a result of once all its inputs square measure "High.", the output of this gate is "High" that is termed "active High output". As an alternate to AND gate, the gate is connected the output are going to be "Low" (0) only if all its inputs square measure "High". Such o/p is called "active low output".

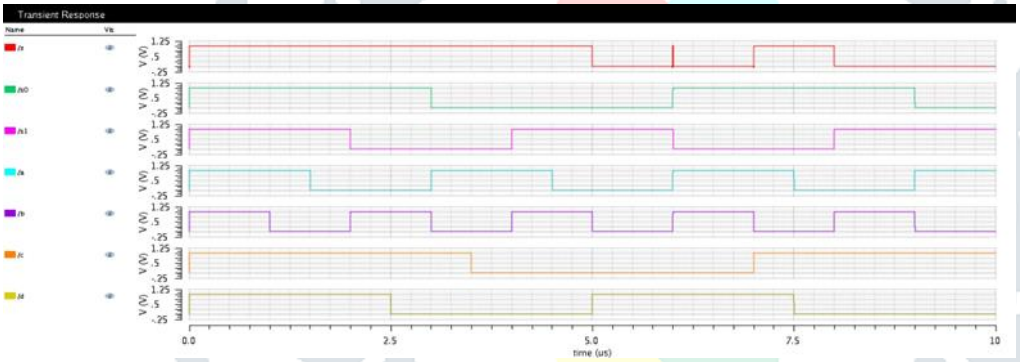


fig. output waveforms of decoder

ONE BIT ALU

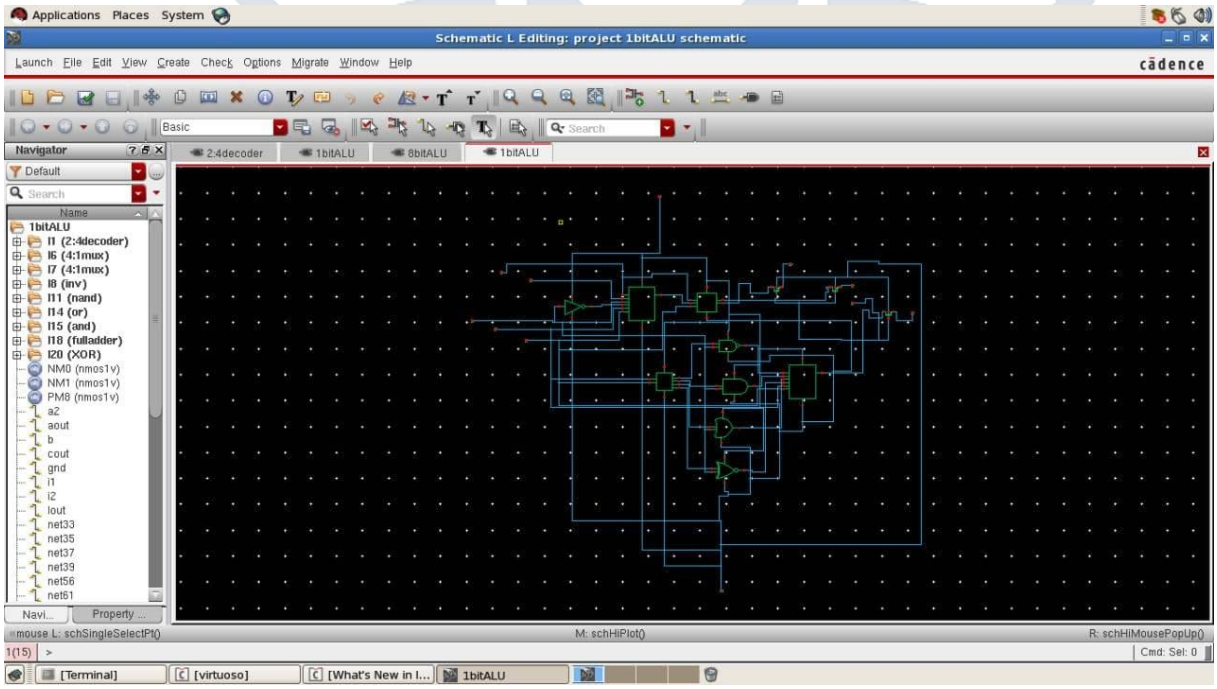


fig. 1-bit ALU schematic

The arithmetic unit of ALU consists of 4 is to 1 data selector, the inputs for the data selector are A,B,C and D out of which it selects only one input depending upon the combination of selection lines S0 and S1.the output of ALU is connected to as one of the inputs to the full adder, the full adder takes the inputs and then process to get two outputs one is sum and the other output is carry. Whereas the logical section contains 2 is to 4 decoder which is also called as data distributor, four logic gates namely NAND, AND, OR and XOR and a data selector. The functioning of logic unit is in such a way that the 2 to 4 decoder takes two selection lines as inputs and the output of these gates is connected to the data selector, which selects one among the four logical inputs as output.

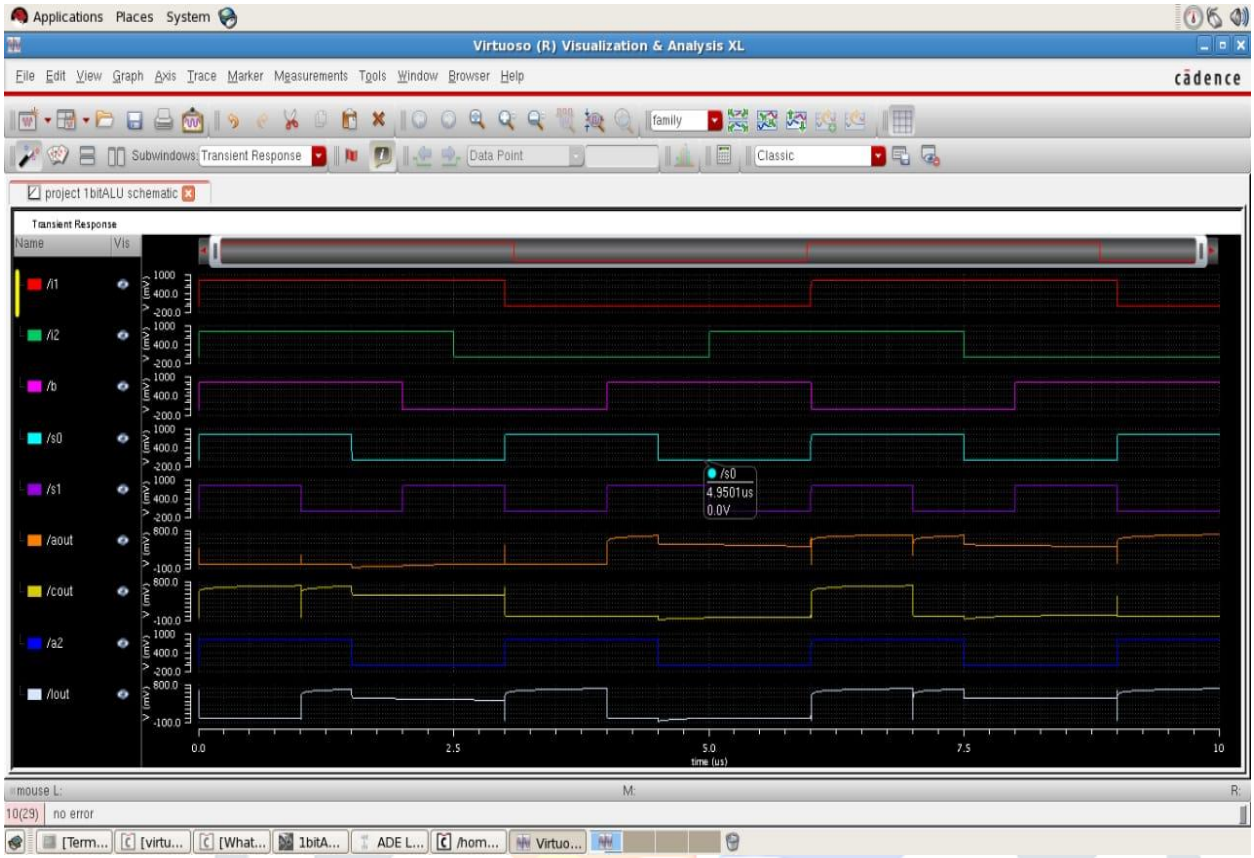


fig. transient analysis of 1-bit ALU

8 BIT ALU:

The symbol of 1- bit ALU is designed using Cadence Virtuoso software and it's symbol is extracted and then placed in order to design a 8 bit ALU.

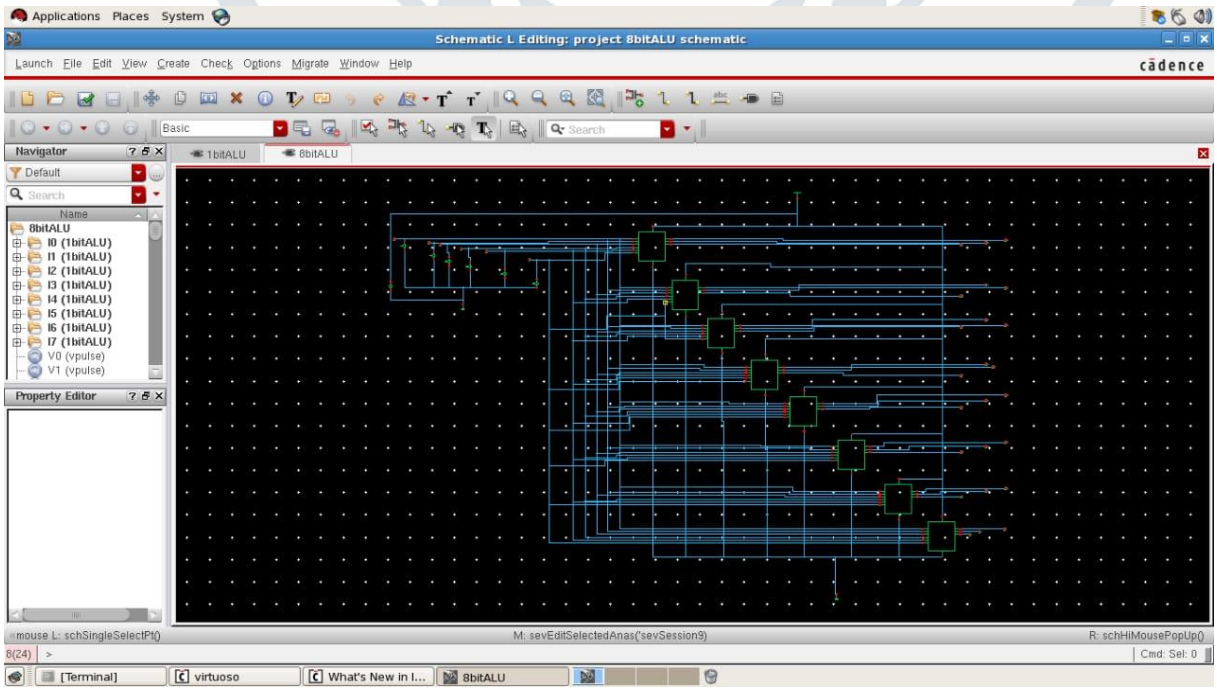


fig.8-bit ALU

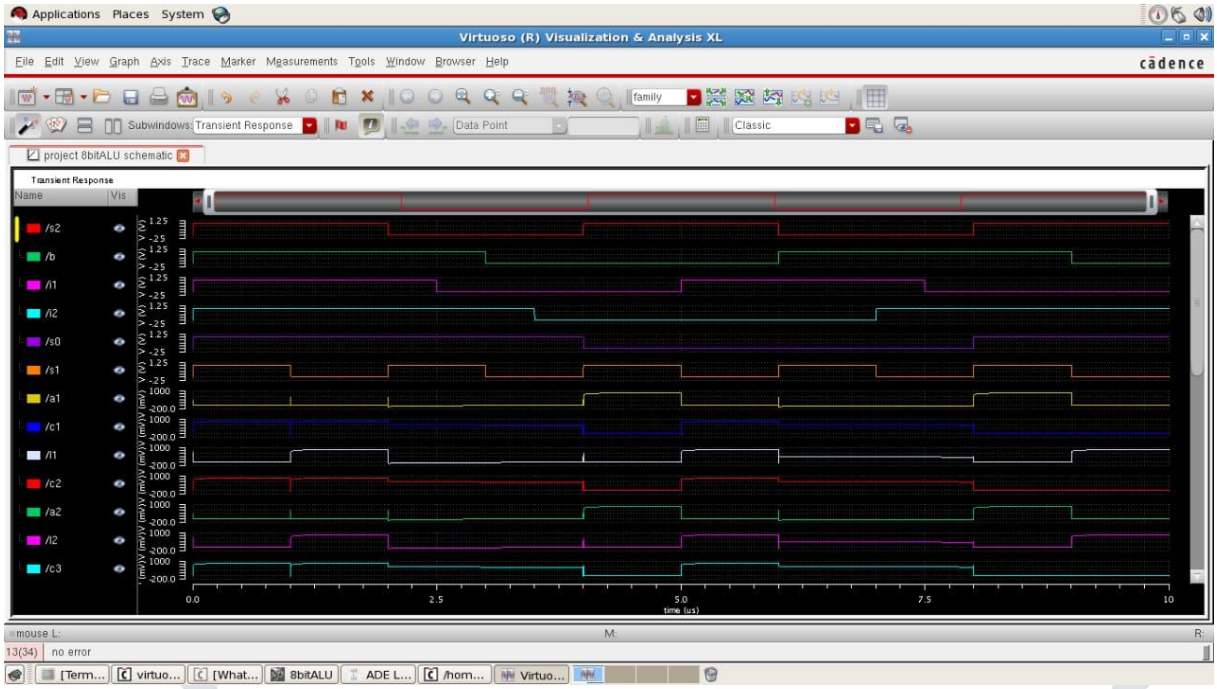


fig. transient analysis of 8-bit ALU

RESULT ANALYSIS

(i). Power comparison

The dynamic power dissipation of any circuit can be intended using the formula given below, by the equation

P dynamic power = α×f×C1× V dd

All other designs offer middle power between the two extravagances.

The projected ALU style offers thirty eighth saving with reference to the Static CMOS and Mirror adders.

This strategic design offers a least transistor option to meet the wanted necessities where other low-transistor projects fail to offer power efficiency.

(ii). Delay comparison

Propagation delay normally depends on the supply voltage. As experiential in the table the planned strategy shows less delay than other topologies. Due to large quantity of the threshold voltage loss in the pass transistor circuits, the delay gets affected.

(iii). PDP comparison

At very low supply voltages, ALU shows less delay. The planned ALU offers stable PDP value throughout the supply voltage range, present significant upgrading compared to existing designs at lesser voltages. In particular, it offers in place of much as 65.58 % improvement in PDP at VDD 1.8 V with respect to the conventional systems

(iv). Temperature Analysis

The variations in temperature will affect the performance of the circuits. This proposed design was done under ambient conditions and mostly performance was estimated in range of room temperature. The supply voltage is fixed at 1.8 V. The simulation results of 1-bit full adder as shown in fig 5.

The input patterns square measure applied to stimuli to visualize the performance of 1-bit adder circuit.

CONCLUSION:

The proposed ALU is designed to give low power delay product which is designed in LINUX computer and is implemented in Cadence Virtuoso tool using 45nm technology. All the designed circuit schematic is simulated and verified for the functionality. The proposed ALU consumes a power of 136pW, which is very less when compared to all other designs.

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