DESIGN OF BRAUN MULTIPLIER USING PASS TRANSISTOR LOGIC

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ABSTRACT *:* In this paper the perception that is used is power resourceful multipliers which are very significant part of all VLSI system design which provides high Speed with Low Power Consumption which are the key necessities for any VLSI circuit design. This paper propose an well-organized execution of a high Speed with low power multiplier using Double Pass Transistor Logic technique and also presents the realization of Braun multiplier using Double Pass Transistor Logic in Cadence RTL Complier with simulation which includes creating the Test circuit for each block that is combined together which forms Multiplier. The paper explains the design of Braun Multiplier and simulated by creating the schematic circuit for each of the structure blocks such as the AND gate, OR gate, NOT gate, EXOR gate, Half Adder, Full adder circuits. Symbol for these building blocks are generated and are called to construct the structure of Braun Multiplier. All the test circuits are simulated and synthesized using the Cadence tool. Then the Braun multiplier is compared with respect to the existing and proposed method to know the number of transistors and also compared the power dissipation for both existing and proposed method.

Index Terms-Braun, Cadence, RTL Complier, Low Power Multiplier, Double Pass Transistor Logic, full adder, half adder, xor gate.

I.INTRODUCTION

Multipliers are the most important structure of many digital circuits that has many applications in VLSI world. By reducing the power consumed by the multipliers will provide a capable digital circuit in conditions of power consumption. Multipliers are designed using adders at different stages. Mainly full adders are implemented to create the multipliers, simulated and analyzed to give better results and also to reduce the number of transistors used in the overall implementation of the multipliers that is used in many digital circuits.

II. BRAUN MULTIPLIER

From all the entire parallel multiplier, the Braun multiplier is the simplest which is used to multiply unsigned binary numbers. The partial products are formed parallel, and then are collected through a stage of Adders. This kind of multipliers have replaced the basic traditional multipliers with double passtransister logic. These multipliers possesse main features such as accuracy, dynamic range and speed when compared to the traditional multipliers.

The number of bits that are used in the multipliers affects and is the deciding factor of the accuracy and the dynamic range of the given multiplier. In this paper we are considering multiplication of two unsigned numbers A and B. The method f multiplication of binary numbers is shown below.

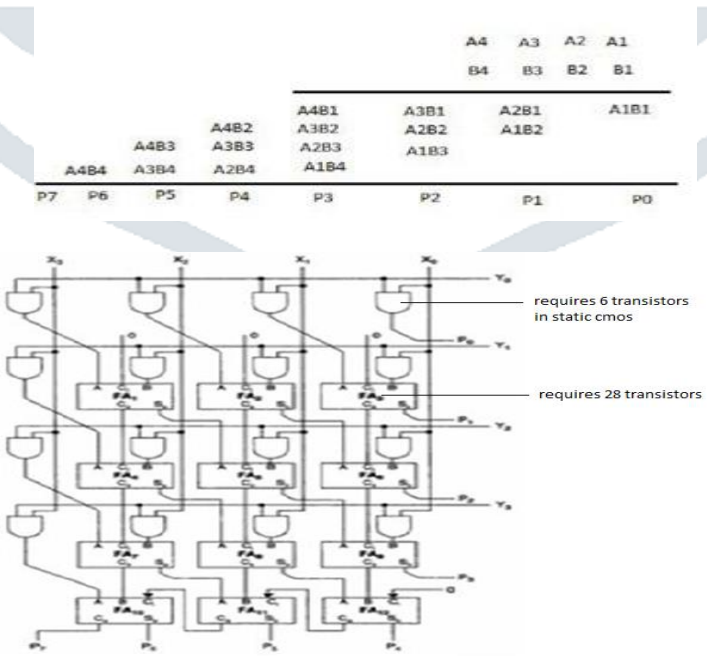

Fig.1: Conventional Braun multiplier

III. PROPOSED METHOD:

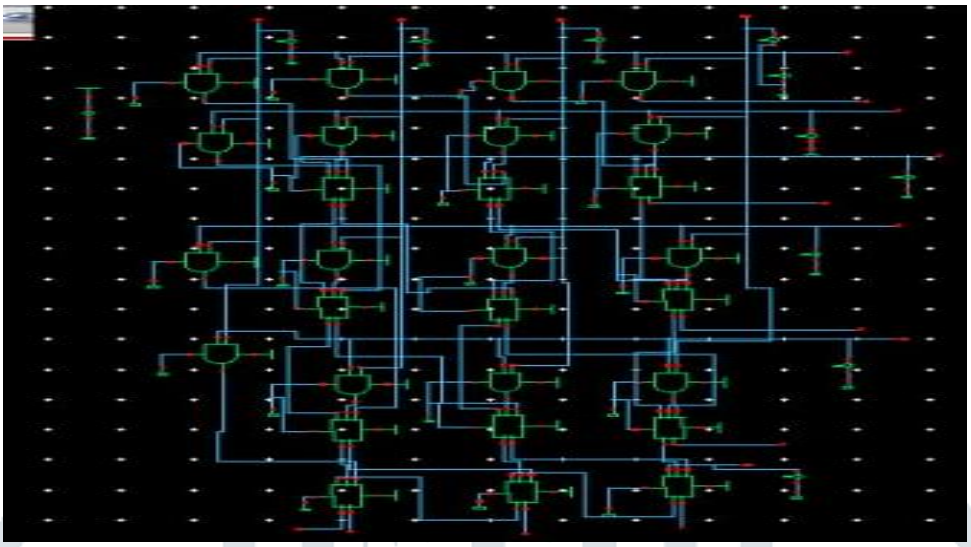

Fig.2: Proposed Braun multiplier with double pass transistor logic.

Fig.3: AND gate with double pass transistor logic.

AND OPERATION:

The input A is given to select line.The input A is given to the select line. The output depends on the value given to A. The output depends on the value given to A. When A=0 output is 0 since the MUX is off.Hence the comditions for AND Gate is satisfied.Refer[3].

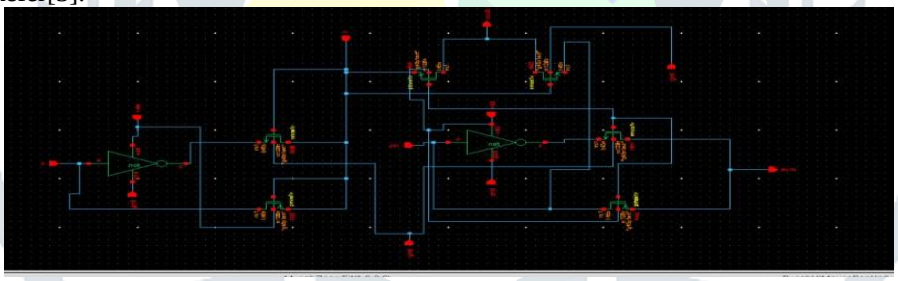

Fig.4:10T full adder

10T FULL ADDER OPERATION:

CASE[1]:The input A=1,B=1,C=1 is given to the inputs the transistor Q4 ON and Q1 OFF and Q3 ON and Q6 OFF the COUT=1 Q2=1 then SUM=1.Refer[2].

In the proposed method the Braun multiplier design with the help of double pass transistor logic technique. Due to this the number of transistors which are required to design it drastically reduces when compared to the static CMOS technology which was used in existing method. When the number of transistors reduces the design are reduces automatically the power dissipation reduces when compared to existing method. In the proposed method the full adder design with the help of 10 transistors combination of both pmos and nmos transistors with the help of double pass transistor logic. The AND gate also designed by only one pmos and one nmos transistor. The operations of full adder and AND gates are verified with the test circuits which are simulated with the help of Cadence tool. The Individual blocks that is required for forming of Braun multiplier are AND gate, Full Adder and Braun multiplier as shown in Fig2 to Fig 4.

The procedure is described in steps

1. The gates are created by using the transistors.
2. The schematic circuit is checked for any errors and rectified.
3. The test circuit is created for the schematic circuit by giving appropriate inputs from the device library and generic library from the software.
4. The circuit is Simulated and different analysis are verified and the block is checked.
5. All the blocks are connected and placed together to work as Braun Multiplier Fig.2 and simulation results are shown in Fig 5.

IV.SIMULATION RESULTS:

In proposed method the power consumption for braun multiplier is 1.521Uw.

The simulation results obtained by Cadence Virtuoso tool by applying proper input signals to the input terminals of Braun multiplier. The simulation results are as shown in the below fig.5.

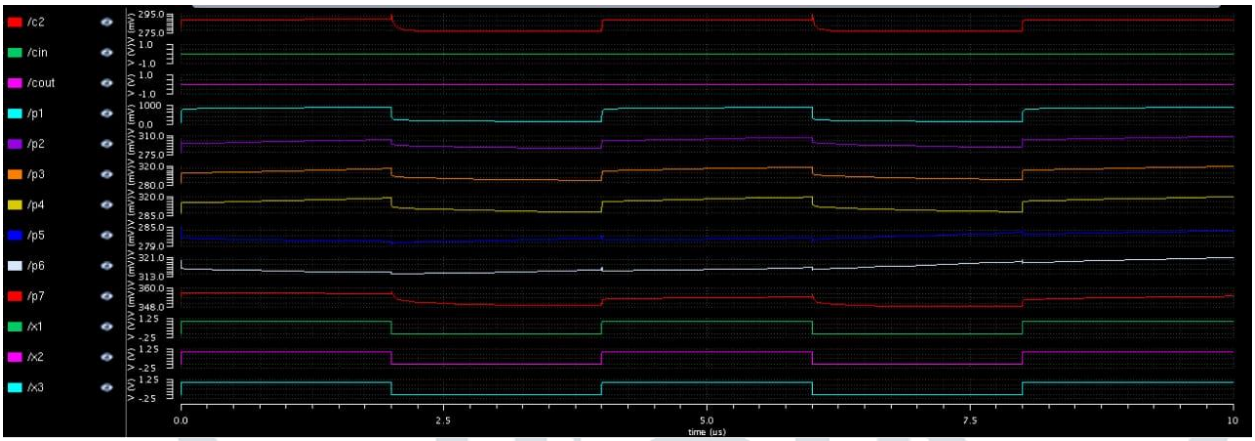

Fig.5: Proposed method Simulation Results of Braun multiplier

V.COMPARISON:

Braun multiplier has been simulated using a common test setup in Cadence. A variety of test vectors are applied at the input ports and the resultant outputs are analyzed using Spectre waveform window.

The functionality of multipliers is tested by first applying all "0" signals at the input ports. And then by setting one of the inputs high while keep the other still "0". And finally, by setting all of the inputs high and measuring the delay and Power Consumption. The worst case Power is obtained when all the inputs are pulled high.

Multiplier	Braun Multiplier	Proposed Braun Multiplier
No.of AND gates	16	16
No.of full adders	12	12
No.of transistors	580	152

VI. CONCLUSION:

The Braun multiplier was implemented by double pass transistor logic using cadence Virtuoso tool, layout them in Encounter by cadence and the analysis of average dynamic power dissipation was done. The proposed Braun Multiplier is 120x faster than Conventional Braun multiplier which was designed by static CMOS technique. Power can be further reduce by implementing the design using latest technological node such as 22nm, 18nm etc.

REFERENCES:

[1] P.Sangeetha, Aijaz Ali Khan, "Comparision of Braun Multiplier and Wallace Multiplier Techniques in VLSI",Fourth International Conference on Devices ,Circuits and Systems(ICDCS'18)"PP-48-53

[2]S.Selvi*,S.Pradeep "6Transistor Full Adder Circuit using Pass transistor Logic" Journal of Chemical and pharmaceutical sciences PP-144-148.

[3]Sruthi.V,Akhila.Raj.K.M , Madhulika.A.R,Ajin.A.S, "SSRG International Journal of Electronics and Communication Engineering(SSRG-IJECE)-Volume 3 Issue 6- June 2016 PP-5-8.

[4] M. H. Rais, M. H. Al Mijalli, "Virtex-5 FPGA Based Braun's Multipliers", Int. J. Comput. Sci. Network Security, vol. 11, no. (8), pp. 81-84, 2011.

[5] Yan J and Z, Chen, Low-Cost Low-Power Bypassing-Based Multiplier Design. IEEE International Symposium on Circuits and Systems, 2010.

[6]Neil H. E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design- A Circuit and Systems Perspective", Pearson, 2006,pp.345357.

[7] N. Bandeira, K. Vaccaro, And J. A. Howard, "A Two's Complement Array Multiplier Using True Values of the Operands",IEEE Transactions On Computers, VOL. c-32, NO. 8, August 1983.

[8]R. Bajaj, S. Chhabra, S. Veeramachaneni and M B Srinivas, "A Novel, Low-Power Array Multiplier Architecture",International Institute of Information Technology-Hyderabad.

[9] P.V. Rao, C Prasanna Raj, S. Ravi, "VLSI Design and Analysis of Multipliers for Low Power", Fifth International Conference on Intelligent Information Hiding and Multimedia Signal Processing",2009.PP-1354-1357.