

AN EFFICIENT PRIORITY ENCODER & DECODER USING 45nm FinFET TECHNOLOGY

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Abstract : Now a days the technology is improved in day to day life. The area, power and timing these three characteristics are very important in the design of low power VLSI systems. The CMOS technology is one of the fastest growing technologies where the analog and digital ICs are fabricated. Reduction of power consumption & reduction of area are the most important issues in CMOS circuit design. To optimize these parameters the proposed research work incorporated the 45nm FinFET technology for designing of 16:4 encoder and 4:16 decoder by using universal gates. The 16:4 encoders occupied an area of 170.04 μ m², 4:16 decoder area is 189.88 μ m², power consumption of encoder and decoder are 1.173 μ W and 2.05 μ W. All simulation results and analysis are performed on 45nm using cadence virtuso tool. In this paper analyzes and optimizes area, power and size of the encoder and decoder using 45nm technologies.

Index terms: FinFET, Digital and analog circuits, Encoder, Decoder

I. INTRODUCTION

The electronic devices are used in many different applications and the size of these devices is linearly reduced, this is due to integrated circuit technology. These integrated circuits are directly or indirectly used in our real time applications. The growth of integrated circuits towards the large integration density with high performance like high speed, less delay and less area. The IC's have two major advantages over discrete circuits which is cost and performance. In IC fabrication. In recent years we are using CMOS technology for fabrication of IC's. The CMOS consists of both PMOS (pull-up network) and NMOS (pull-down network). This technology is used in fabrication of microprocessors, microcontrollers, static RAM and other digital circuits.

In the applications such as image and signal processing, computer graphics, communication networks and digital applications the analog to digital and vice versa conversion is needed. To obtain these we are using encoding and decoding techniques. The encoding means the analog information is converted into binary form. The decoding means the coded value will be converted into original information. Based on types of applications different types of encoders and decoders are available. To achieve low power and less area of encoder & decoder design we are using innovative MOS structures called Fin-FET technology. FinFET technology is also called as Double-gate CMOS (DGC MOS) is very close to that of conventional CMOS process, with only minor disruptions, offering the potential for a rapid devolvement to manufacturing. The benefit of finFET's double gate structure exhibits in the maximizing of the gate-to-channel capacitance and minimization of the drain-to-channel capacitances. The main objective of this paper is to design and analyze the performance of 16:4 encoder and 4:16 decoder using finFET 45nm technology node and compare the performance with CMOS 45nm technology node using metrics (power, delay and time).

II. LITERATURE SURVEY & RELATED WORKS

In the world integrated circuits, CMOS has lost it's preference during the scaling beyond the 45nm. From the literature so many works have been carried out for the implementation of FINFET based circuits. The main drawback of using CMOS technology is high power consumption and high leakage current. The CMOS 45nm scaling cause severe short channel effects which is difficult to reduce. SCE causes an exponential increase in power dissipation & leakage current. The solution for this problem can be achieved by using multi gate MOSFET technologies, this provides a stronger control over a thin silicon body with multiple electrically coupled gates.

The FinFET technology is the most promising and suitable technology to overcoming the problems in the single gate field effect transistors(SGFET). FinFET technology reduces the short channel effect and the similarity of the fabrication steps to the existing standard technology (Sushil Bhushan et al.2010).

FinFET device has a higher controllability. The reason behind the improved performance is that the FinFET has two gates in which the second gate was used to dynamically control the threshold voltage of the first gate in order and reduce leakage power (dhruva et al.2003).

The Encoder and Decoder circuits can be designed by using this FinFET 45nm technology in order to achieve high performance.

Related works

Many of the researches contributed in the low power design perspective of digital circuits as follows:

Akash Shyam et al. designed CMOS based 2:4 decoder using self-controllable switch technique to achieve low power and high speed performance

Amuthavalli et al. elaborated the design of different digital circuits in CMOS technology and achieved the reduced subthreshold leakage using leakage reduction technique.

T. B. Singha et al. achieved low power solution to CMOS based 4:2 priority and 2:4 decoder in context of adiabatic logic.

Amitraut et al. discussed the performance of 2:4 decoders using reversible logic for low power consumption.

III. PRIORITY ENCODER

A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. Encoder converts information from one format or code to another, for the purpose of security. It is mainly used for the encoding of the data. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. The purpose of this paper is to design the 16:4 encoder using universal gates. The FinFET 45nm technology is used in the design process of 16:4 encoders. By using FinFET Technology the Encoder Area, Power consumption will be reduced. Encoders are the sensors that generate digital signals in response to movement. It can also be used to measure the linear movements, speed and position. A digital encoder more commonly called a binary encoder take 2^n data inputs one at a time and then converts them into a single encoded output unlike a multiplexer that selects one individual data input line and then sends that data to a single output line.

A 16:4 priority encoder is digital circuit which provides binary equivalent any of the asserted input signal. If two or more inputs are given at the same time, the input having the highest priority will take in the precedence. The digital 16:4 priority encoder and its inputs lines are D15,D14,D13,D12,D11,D10,D9,D8,D7,D6,D5,D4,D3,D2,D1,D0 and output lines are O4,O3,O2,O1. The output is '0' if there are no inputs i.e. all inputs pulses are low. the outputs can be derived from the truth table of priority encoder. The O1,O2,O3,O4 equations are given by

$$\begin{aligned} O1 &= ((D8D9)' (D10D11)' (D12D13)' (D14D15)')' \\ O2 &= ((D4D5)' (D6D7)' (D12D13)' (D14D15)')' \\ O3 &= ((D2D3)' (D6D7)' (D10D11)' (D14D15)')' \\ O4 &= ((D1D3)' (D3D7)' (D9D11)' (D13D15)')' \end{aligned}$$

By using the above equations we can realize the schematic diagram of the priority encoder. This can be designed by using universal gates. The schematic diagram of a 16:4 priority encoder in VMWARE software is shown below.

After designing the schematic diagram check for errors and generate the waveforms by using procedure and calculate the power using the formula and compare this power with cmos 45nm technology.

For area calculation design the layout diagram which is shown below and check for errors that are DRC & LVS errors. If no errors occurs then calculate the area using formula compare with CMOS technology.

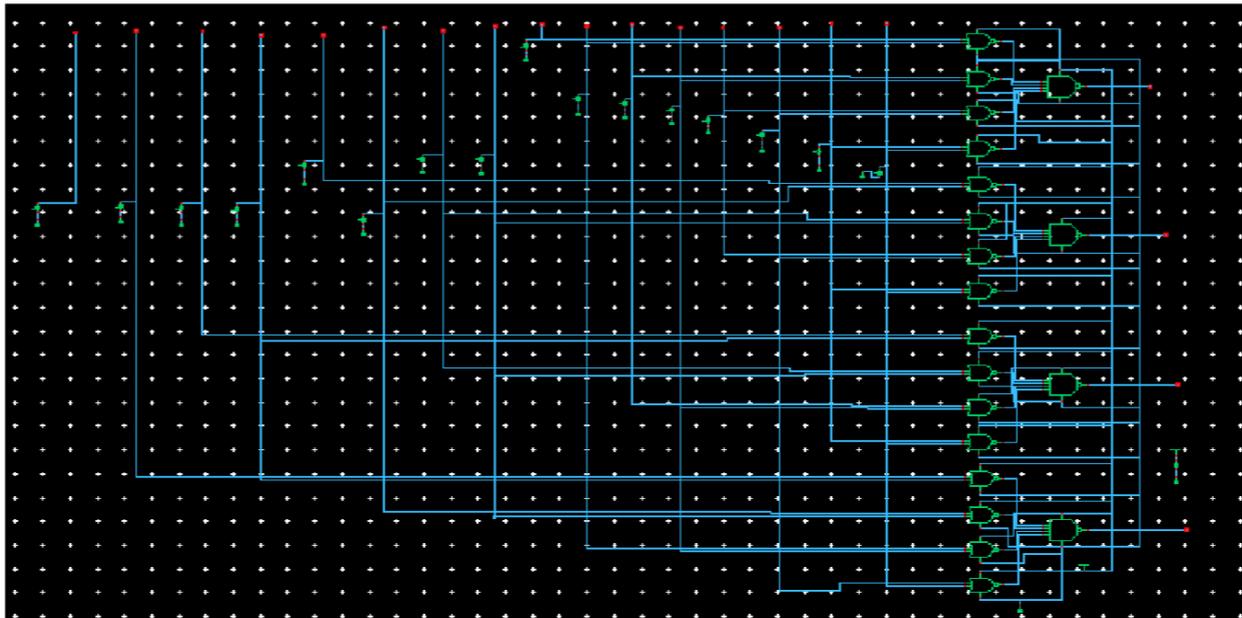


fig. 1 (a) schematic diagram of 16:4 encoder

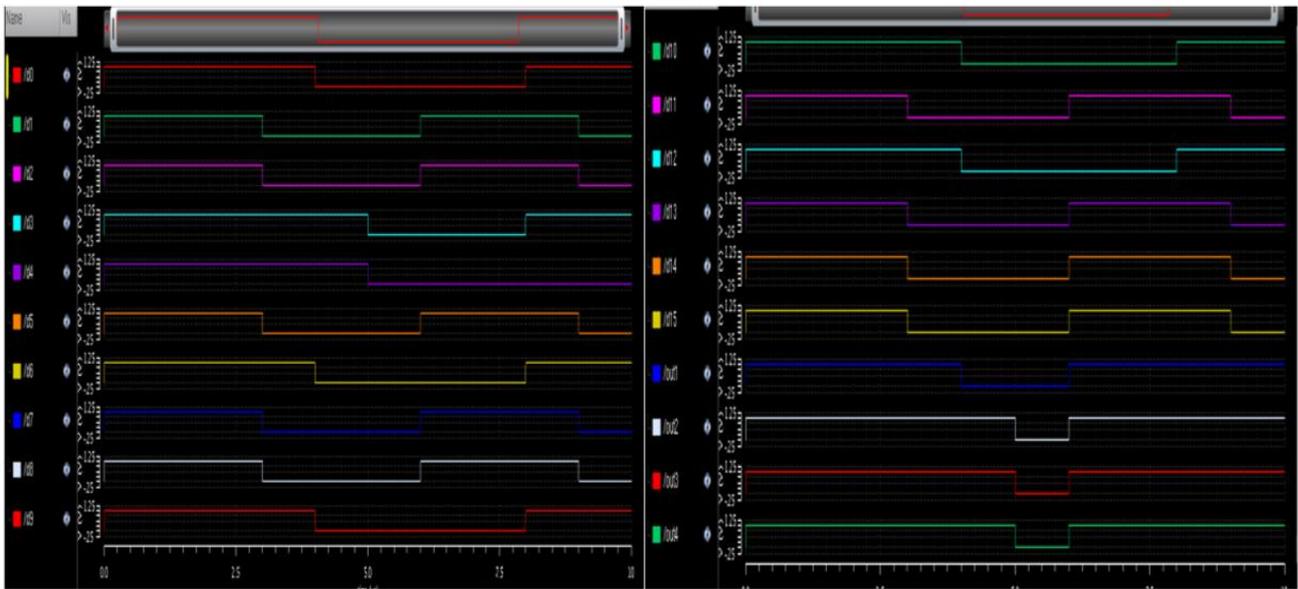


fig. 1(b). simulated results of 16:4 encoder for the pulse with ton=2us, toff =2us and total time period=4ns.

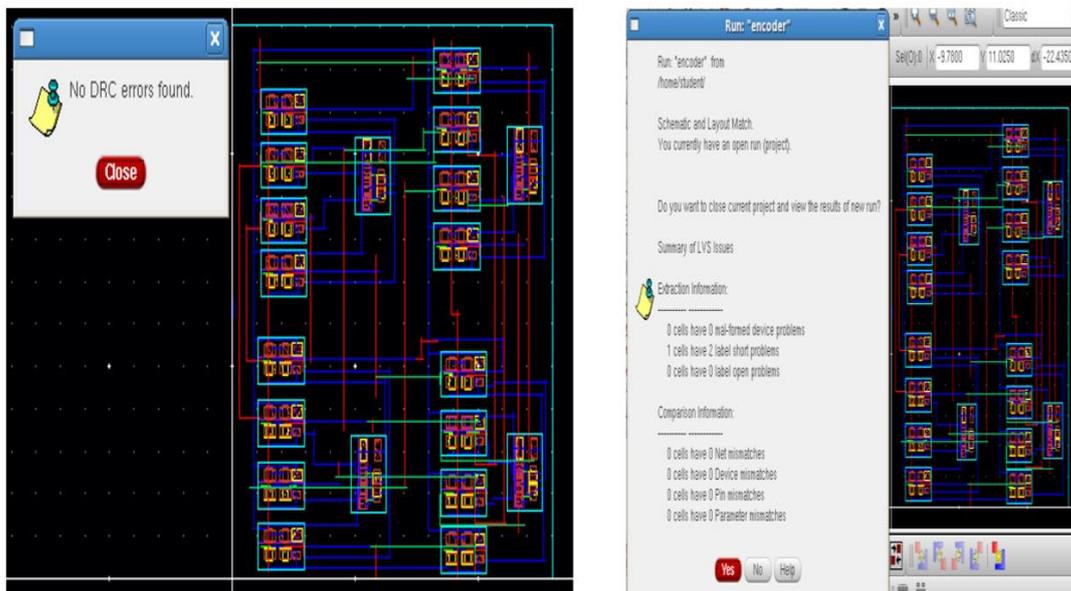


fig. 1(c) .layout design and drc ,lvs error checking of 16:4 encoder

IV. DECODER

A Decoder is a device which does the reverse operation of an encoder. It is a combinational logic circuit that converts binary information from the N coded inputs to a maximum of 2^N unique outputs. A Decoder is generally used to decodes the data means the binary data converted into non binary data. They are used in many applications like de multiplexing , seven segment display and memory address decoding. However, there is a limit to the number of inputs that can be used for one particular decoder. Because of N value is increase, the number of NAND (or) AND gates also increase. But same binary decoders are constructed using NAND gates. Instead of using AND gates because of the NAND gates cheaper to produce than AND's. They require fewer Transistors to implement, they use of NAND gates as the decoding elements, results in as Active “low ” output while the rest will be “High”. As a NAND gate produces the AND operation with an inverted output.A 4:16 decoder is having 4 inputs &16 outputs the decoder equations are given below. By using that equations design the schematic diagram using nand gates and calculate the power compare with 45nm CMOS technology. For area calculation go for layout design and calculate the area using formula.

Decoder design equations:

Inputs (A ,B, C,D)

Output :(D0 ,D1 ,D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15)

$$D0 = A' B' C' D' \quad D1 = A' B' C' D \quad D2 = A' B' C D' \quad D3 = A' B' C D$$

$$\begin{array}{cccc}
 D4 = A'BC'D' & D5 = A'BC'D & D6 = A'BCD' & D7 = A'BCD \\
 D8 = AB'C'D' & D9 = AB'C'D & D10 = AB'CD' & D11 = AB'CD \\
 D12 = ABC'D' & D13 = ABC'D & D14 = ABCD' & D15 = ABCD
 \end{array}$$

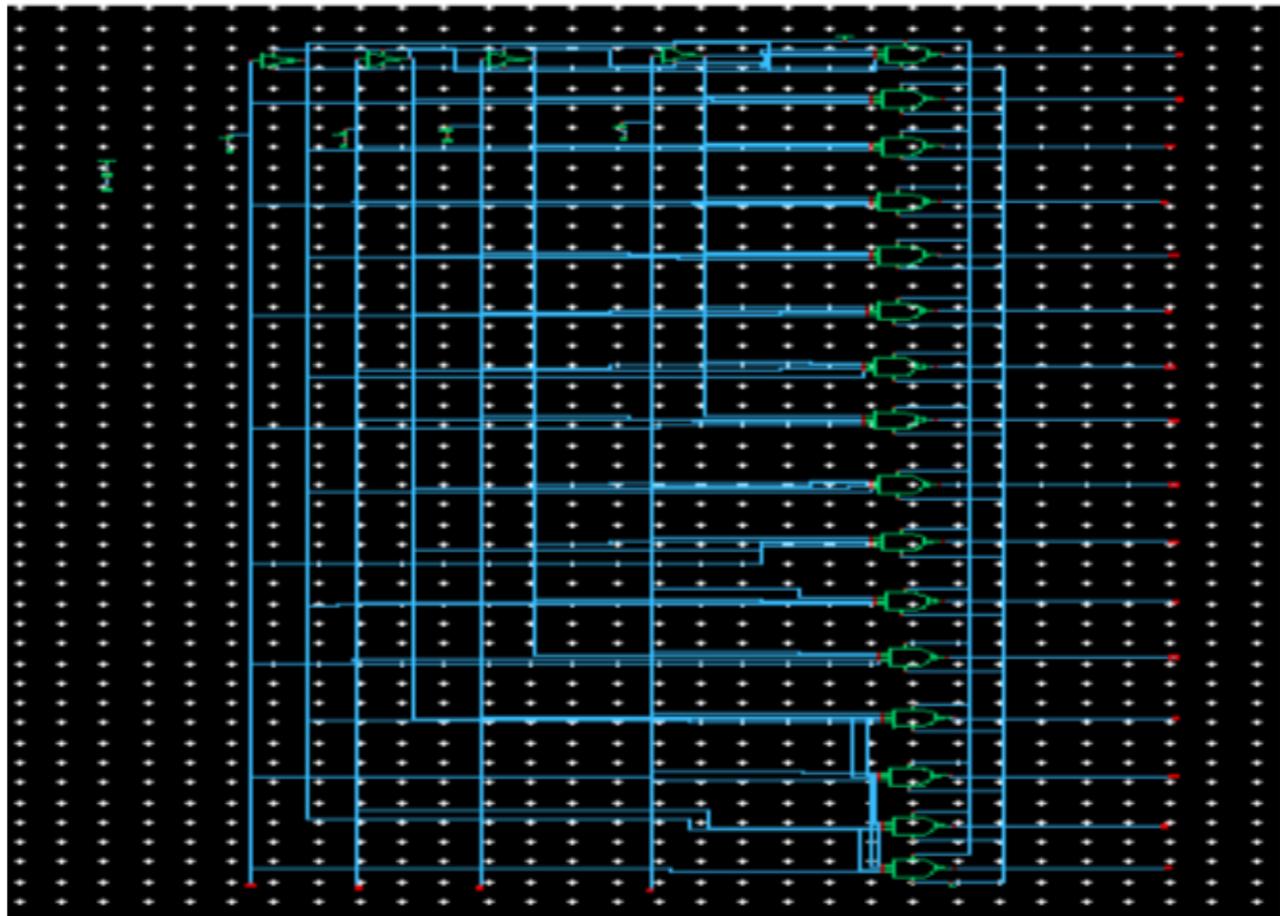


fig. 2 (a).schematic diagram of 4:16 decoder

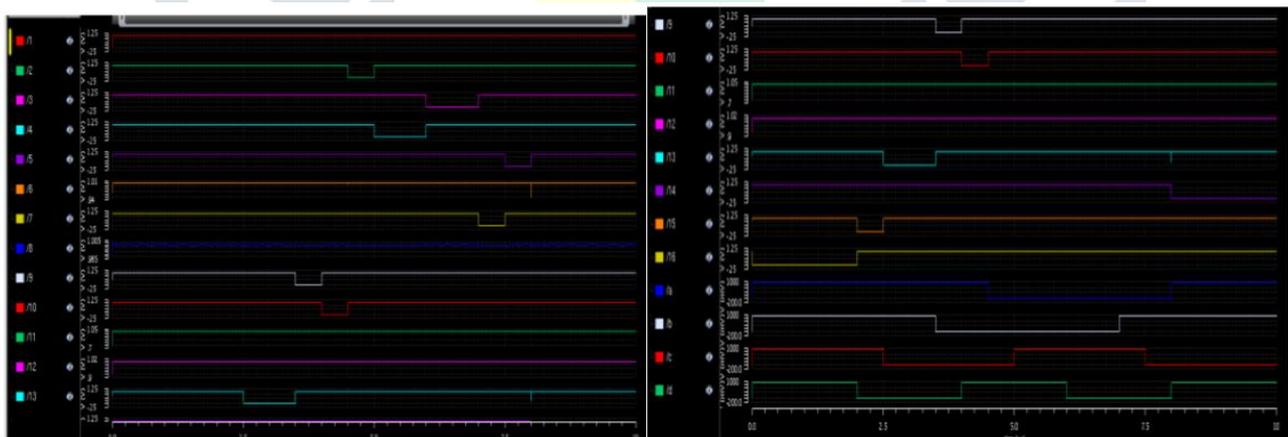


fig.2(b). simulated results of 4:16 decoder for pulse with $t_{on}=2\mu s$, $t_{off}=2\mu s$ and total time period= $4\mu s$

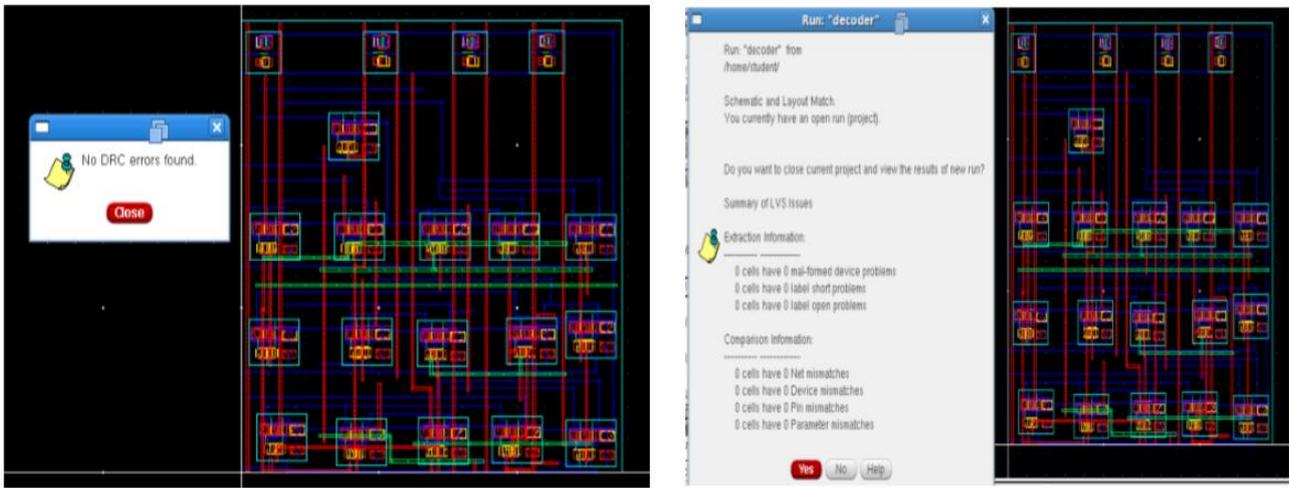


fig. 2(c). layout design of 4:16 decoder using 45 nm finfet based and its drc and lvs verification.

In the design process of 16:4 encoder and 4:16 decoder we are using universal gates that are NAND & NOR gates. In this design we are using 4 input NAND gate & 2 input NOR gate. The schematic diagrams and layout diagrams of NAND & NOR gates are shown above & below figures. We can extract the symbols for NAND & NOR gates that can be used in the design of encoder & decoder.

For this gates also calculate the power and compare with this 45nm CMOS technology and we can observe the reduction in the power.

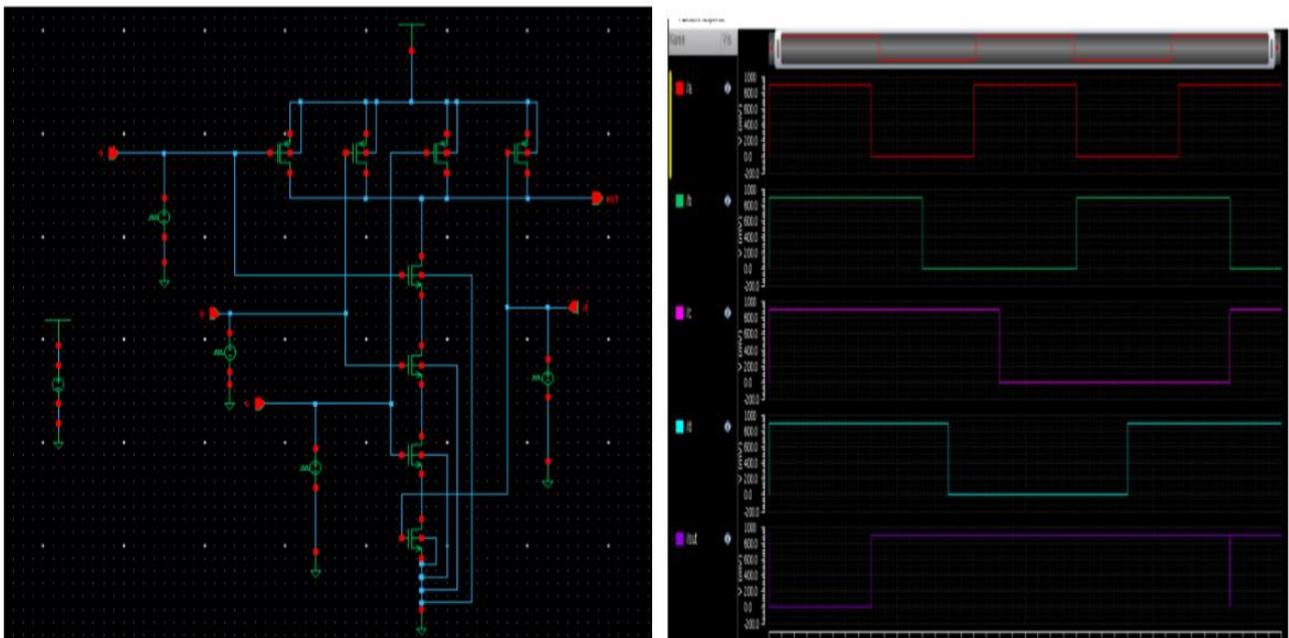


fig.3 (a). 4-bit input nand gate which is used for the design of encoder and decoder and its simulated results for pulse width of 10nm, ton=4um and toff=4um.

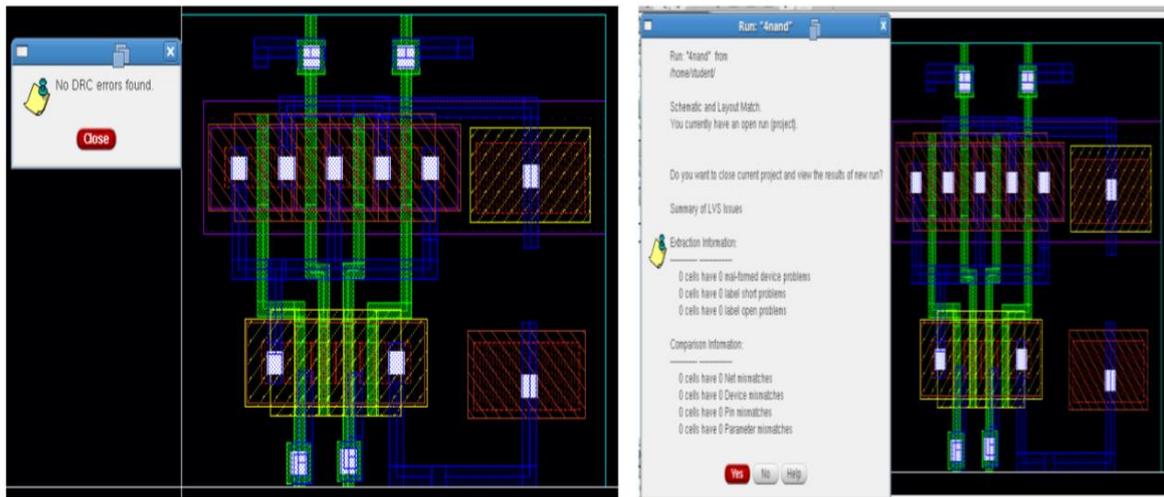


fig. 3 (b). layout design of nand gate and its drc and vls verification

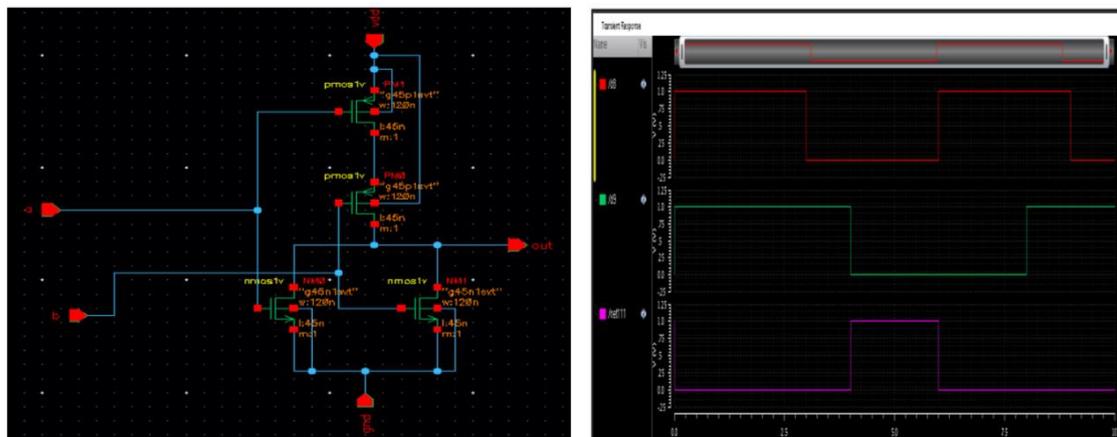


fig. 4(a). schematic diagram of 2 input nor gate and its simulated results

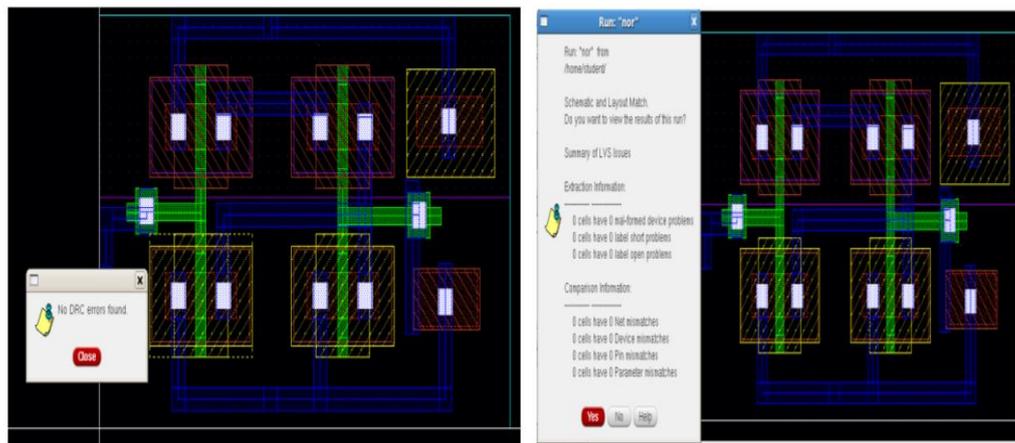


fig. 4(b). layout design of nor gate and its drc and lvs verification

V. PERFORMANCE COMPARISION

The Encoder and decoder are designed has been effectively actualized with the SOC Encounter. The 16:4 encoders occupied an area of 189.88um², 4:16 decoder area is 170.04um², power consumption of encoder and decoder are 2.68uW and 1.98uW .their delays are 24.4 and 19.56msec. The below Table shows the Synthesis of Physical Layout Results Implemented in SOC Encounter

table 1.power ,area comparision of cmos 45nm & finfet 45nm technologies

Component	CMOS 45nm		FinFET 45nm	
	Power(uw)	Area(um ²)	Power(w)	Area(um ²)
NAND (4input)	56.7	732.1	111.3pw	2.56
NOR (2input)	83.5	864.4	51.68pw	2.01
16:4 Encoder	362858.23	3409	1.17nw	170.04
4:16 decoder	329592.263	3237	2.05nw	189.88

VI. CONCLUSION

The all-advanced 16:4-piece encoder dependent on various heartbeat signals at 20 Gbit/s is proposed and tentatively exhibited utilizing the 4-bit inputs NAND impact in SOAs fell with detuning NOR entryways. As the last outcomes, right and clear transient waveforms and open eye designs were acquired, and elimination proportions surpassing 15 dB were accomplished. An increasingly confused computerized need encoder circuit with a higher activity bit rate could be acknowledged by falling the 16:4-piece need encoder 4:16 decoder. In addition, the proposed plan can possibly be substantial scale incorporated.

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