HIGH SPEED AND LOW PDP CARRY SKIP ADDER USING PASS TRANSISTOR LOGIC

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Abstract : Adders are the basic architectures that are used in ALU's ,DSP Processors and in Micro Controllers .In this paper, we present a Carry skip adder that has a high speed yet low energy consumption compared with the conventional one. We are concentrated on reducing the power delay product which is figure of merit of VLSI circuits. The Conventional structure is designed by the Static CMOS Technology, the number of transistors and area coverage ,power consumption and delay of the circuits is increased due to more wiring lengths .In Proposed structure the CSKA is designed by using the Pass Transistor Logic technique which reduces the number of transistors count, area and power consumption of the circuit .The design and simulation results are obtained by using Cadence Tool ,Virtuoso using 45nm technology .The results are compared with conventional structure interms of power, delay and area consumption.

Keywords : VLSI, CSKA, PTL, RCA, FA, HA.

I. INTRODUCTION:

Adders are the architectures used in many digital applications .For performing arithmetic and logical operations adders are used in ALU's and in Processors .Full adder and Half adder are binary adders. Full adder is the basic module (block) to design any adder circuits. As every complex circuits requires the Full adder circuit .The low power consumption and delay can be achieved in any computational complex circuits using the Pass Transistor Logic Technology. PDP is the figure of merit in VLSI circuits. The scaling factor improves the transistor density and functionality of a Chip. The scaling factor helps to increase the frequency , speed and Performance of the Chip. Designing of circuits using Static CMOS Technology leads to increase area, power , delay , static power dissipation which occurs leakage current when device is in standby mode. Designing of circuits using Dynamic CMOS Technology reduces the transistor compared to static CMOS Technology but leads to dynamic power dissipation due to charging and discharging of capacitors , short circuits, glitches in the circuits.

II. Conventional CSKA:

The Conventional CSKA block consists of M bit Carry skip adder consists of Q stages. The CSKA structure is builded by cascading full adders in the parallel form to implement Ripple Carry Adder [RCA].In RCA the stage of carryout is given as carryin to next preceding stage for full adder for further addition, but the critical path delay of the circuit is increases. So, The CSKA is implemented which is adder that improves delay on the RCA but the area ,power consumption is similar as RCA[1].The power delay product(PDP) of the CSKA is littler than those of the CSLA and CSKA is significantly littler than the one in the RCA[4] . The CSKA also consists of 2:1 multiplexer and basic gates like 2 input AND, XOR, The 2:1 multiplexer is used for the carry skip logic operation.

The working operation of CSKA is that it operates in two stages that is by generating sum bits from Ripple Carry Adder block and carry propagation block. The carry propagation block uses the 2:1 multiplexer and propagate block. The carry is skipped to the ith position without waiting for rippling by using carry skip logic done by 2:1 multiplexer. The EXOR gates are used to generate the propagation bits. The propagation bits are applied to the AND gates. The output of propagation block will give propagate signal which acts as selection line for multiplexer and selects the carry. If selection line=0 the carryout of RCA is selected ,if selection line=1 the carryin of RCA is selected. The conventional structure of CSKA is shown in below figure 1.

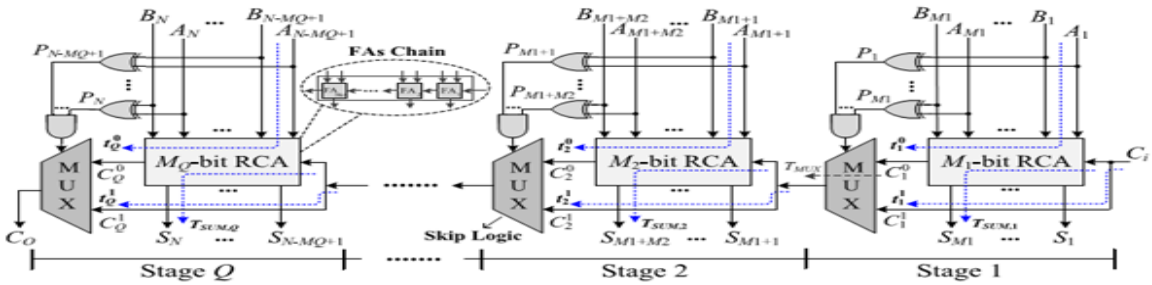

Fig 1: Conventional structure of CSKA

The 16 bit Carry Skip Adder is designed by using Static CMOS Logic Technology, it requires a total number of 736 transistors to design. The full adder consists of 448 transistors, AND gate consists of 72, EXOR gate consists of 160 and 56 transistors for 2:1 multiplexer .Due to increase in the number of the transistor the area coverage ,power consumption and delay of the circuit is increases.

Equation: The Power delay product (PDP)= Power*delay=12.62E-6*15.386E-9=1.941713E-13watts

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III. Pass Transistor Logic:

Pass transistor logic is one of the logic families used for designing the integrated circuits. Pass transistor achieves the characteristics of the switch and passes the signal from input to the output. The Pass transistors are used in many applications because it consumes the less area and power to design by reducing the number of transistor count compared to the Static CMOS Technology[2].

The Pass transistor logic is divided into two types they are PMOS and NMOS .PMOS pass transistor passes strong 1's and weak 0's.NMOS pass transistor passes strong 0's and weak 1's.The NMOS pass transistor logic is used in design in this paper, because NMOS has the better switching characteristics.

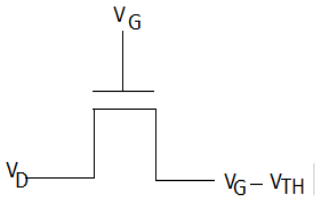


Fig 2: NMOS Pass transistor logic

IV .Proposed CSKA:

The proposed structure of carry skipadder is designed by using the NMOS pass transistors. The working operation of the proposed structure is similar to the conventional structure of CSKA ,the difference only is the internal structure shown in below figure3,4,5 and 6. The full adders ,2:1 multiplexer,EXOR,AND gates are designed by using PTL. The proposed structure of CSKA requires 160 total transistors to design.

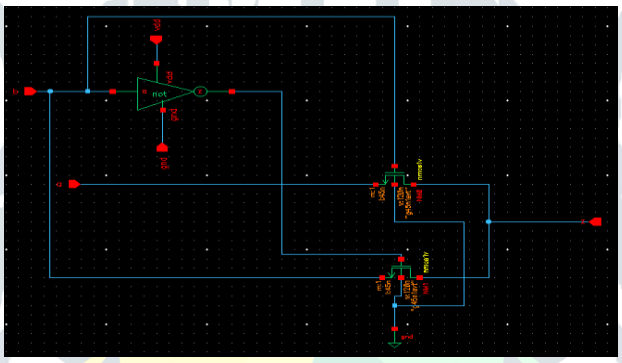


Fig:2 Input AND gate

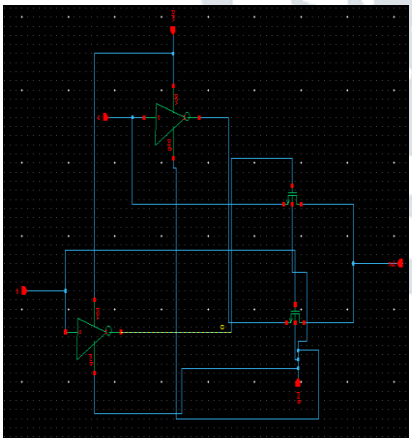


Fig: 3 EXOR gate

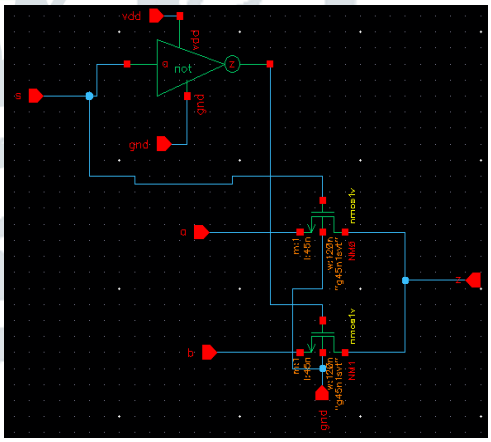


Fig 4: 2:1 multiplexer

Operation of Full Adder:

The Full Adder using Pass Transistor logic consists of 6 transistors to design. The full adder consists of three inputs a,b,c and consists of two outputs sum, carry outputs . Consider applying inputs a=1, b=1 ,c=0 . the complement input c(1) is applied to source and complement input b is applied to gate terminal of 1st transistor the output(1) will be same as input and for 2nd pass transistor c input is applied to source and complement of b(0) is implemented to gate and output will be zero and output (1)(x=intermediate output) is applied to not gate and it acts as input source and a is applied to gate terminal of 3rd transistor and intermediate output(x) is applied to 4th transistor the drain of 3rd and 4th transistor is combined together and give output sum=0.the intermediate output is applied to gate terminal of 5th transistor and a(1) is applied to source and input b(1) is applied to source

terminal of 6th transistor and complement of intermediate output(0) is applied to gate terminal, the both drain terminals are connected together and gives carry out as 1.

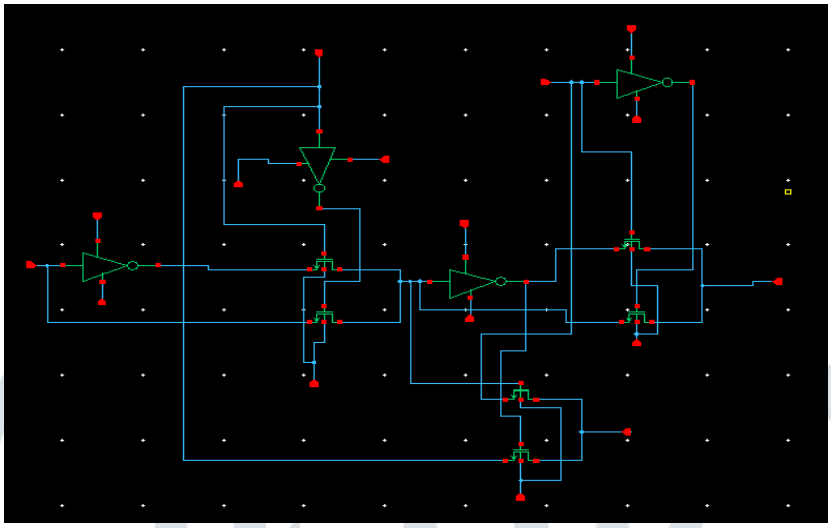


Fig 5: full adder

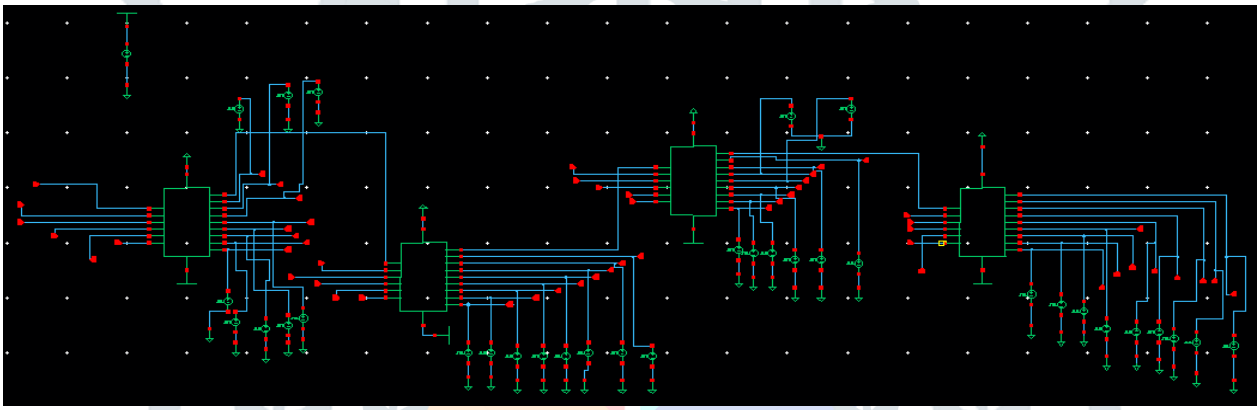
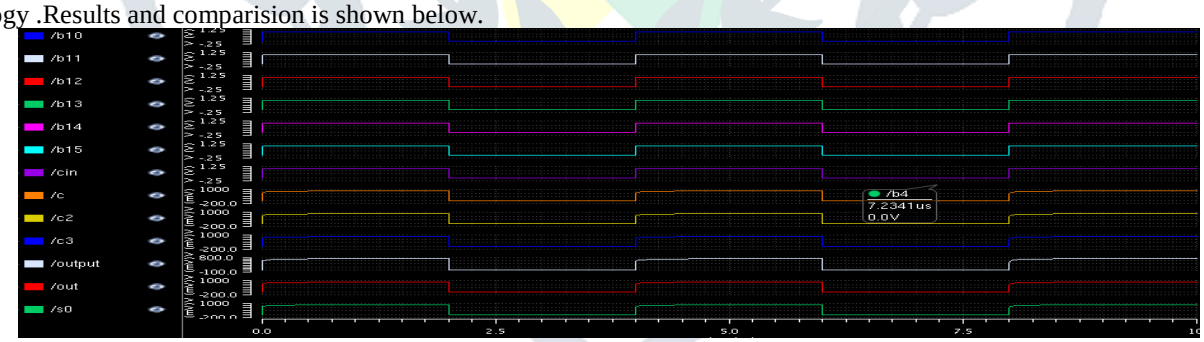


Fig 6: Proposed structure of 16 bit CSKA

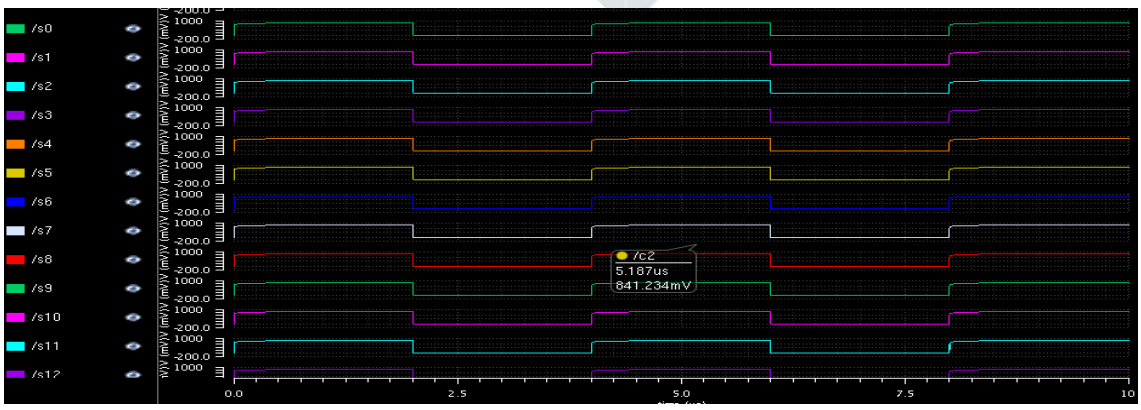
Equation: Power delay product(PDP)=Power*delay=7.314E-12*15.386E-9=1.125332E-19watts

V. Simulation and Comparision :

Simulation of proposed structure of carry skip adder is carried out in Cadence Virtuoso software in 45nm technology .Results and comparision is shown below.



Showing multiplexer output cout, output



Showing outputs s0 to s12

Table 1: Comparision of Conventional CSKA and Proposed CSKA

Factors	Conventional CSKA	Proposed CSKA
Number of transistors	688(with static CMOS)	288(with Pass transistor logic)
Power	15.62uwatts	7.589uwatts
Delay	132.28ps	38.61ns
Power delay product(PDP)	1.941713E-13watts	1.125332E-19watts

VI .Conclusion:

The proposed carry skip adder using Pass Transistor logic has more speed and enhancement compared to conventional CSKA . We can observe the number of transistors, power and delay of the reduced to half compared to conventional structure of CSKA. The proposed CSKA can be used for low power applications. In future, the voltage drop of Pass transistor logic output cannot be same voltage level of input voltage. We can still reduce the power delay product and power dissipation with 32nm and 22nm and 18nm etc.

References:

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