DESIGN OF LOW POWER AREAEFFIECIENCY CSLAUSINGBEC-1 CONVERTER

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Abstract:As we know the analysis of conventional carry select adder from its structure it is clear that there is a scope to reduce the area so it leads the low power consumption and high speed of operation, so it increases the DSP system performance and reduces the complexity of the processor. In this project we implemented the low power area efficient carry select adder by using binary to excess -1 converter. the main function of the binary to excess -1 converter is the logic comes from the lesser number of logic gates as compared to the n-bit ripple carry adder (RCA).CSLA designing with ripple carry adder is not efficient because it uses the multiple number of ripple carry select adders to generate the partial sum and carry by using the carry input. Then the final sum and carry is selected by the multiplexers . so this idea we are uses the binary to excess-1 converter it has less logic gates less power less cost, convenient to handle most used in VLSI systems.

Index Terms - CSLA, RCA, BEC,

INTRODUCTION:

Adder is major part of the processor , as a single processor uses the several adders so in order to design efficient adder it improves the system performance . Initially carry select adder is one of the fastest adder in the digital data processing units.The ripple carry adder is a complex adder. Mainly the ripple carry adder consists of the many cascaded single bit full adders by this we can achieve a simple and efficient but it is very slow process i.e, speed is very low .in carry select adder there will be two ripple carry adders according to the logic we can get the output in carry select adder the delay will reduced as compared to the ripple carry adder.

In this CSLA uses a ripple carry adders which has large area consumption so the proposed technique reduces all the redundant logics by using binary to excess -1 converter .it gives good performance and better output than conventional carry select adder.in my proposal system the final sum is carried before the calculation where as in conventional CSLA it is not done there is also reduces the power delay.here we are using two different carry words(cin=0,cin=1)these fixed bits are going give the logic optimization of carry select and carry generation.

many electronic applications adders play important role , the applications like calculation dsp algorithms like DFT,FFT it requires more number of calculations and complexity increasesCSLA is the one of the most simplest adder it alleviatesthe problem of propagation of carry but it has high area requirement and high power,it can be reduced by binary to excess -1 converter

LITTURATURE SURVEY

The main reason for using the carry select adder with BEC is to reduce the no. of gates when compared to normal Wallace multiplier. The 1'b1 case in normal CSA is replaced by BEC. The result from 1'b0 case is given as inputs to the BEC adder.Design of high speed data path logic systems are one of the most substantial research area in VLSI systemdesign. High speed addition and multiplication has always been a fundamental requirement of high performance processors and systems. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The basic idea of the proposed work is using n-bit Binary to Excess-1 Converters (BEC) to improve the speed of addition. This logic can be implemented with Carry Select Adder to Achieve Low Power and Area Efficiency. The proposed 32-bit Carry Select Adder compared with the Carry Skip Adder (CSKA) and Regular 32- bit Carry Select Adder. The main advantage of this Binary to Excess Converter (BEC) is logic comes from the lesser number of logic gates than the n- bit Ripple Carry Adder (RCA). A structure of 4-bit Binary to Excess Converter (BEC) and the truth table is shown in Fig.1.1 and Table 1 respectively.

Low power, area-efficient, and high-performance VLSI systems are increasingly used in portable and mobile devices, multi standard wireless receivers, and biomedical instrumentation, [An adder is the main component of an arithmetic unit. A complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system. A ripple carry adder (RCA) uses a simple design, but carry propagation delay (CPD) is the main concern in this adder.

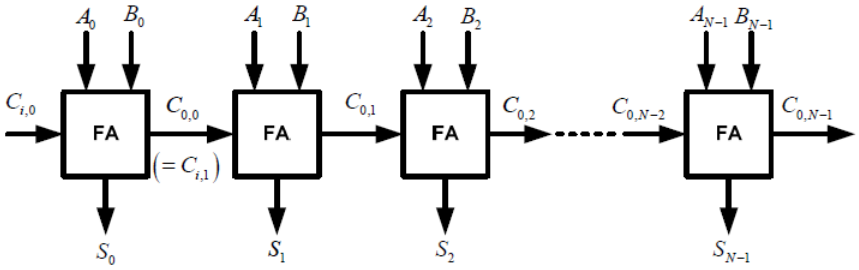

Fig1.carry select adder using full adder

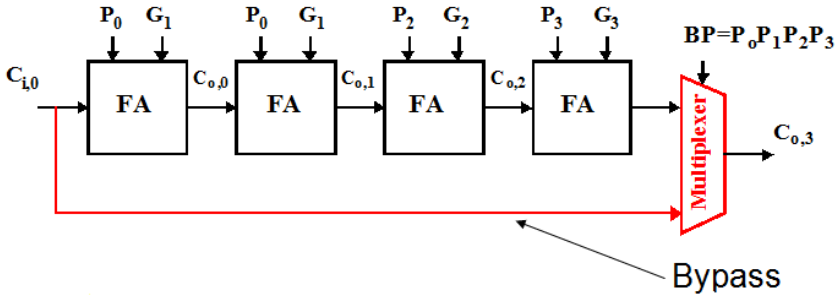

Fig2. Carry select adder using multiplexer

Carry look-ahead and carry select (CS) methods have been suggested to reduce the CPD of adders. A conventional carry select adder (CSLA) is an RCA–RCA configuration that generates a pair of sumwords and outputcarrybits corresponding the anticipated input-carry (*c*in =0 and 1) and selects one out of each pair for final-sumand final-output-*carry* A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses a dual RCA.

Few attempts have been made to avoid dual use of RCA in CSLA design. used one RCA and one add-one circuit instead of two RCAs, where the add-one circuit is implemented using a multiplexer (MUX). He *et al.* Proposed a square-root (SQRT)-CSLA to implement large bit-width adders with less delay. In a SQRT CSLA, CSLAs with increasing size are connected in a cascading structure. The main objective of SQRT-CSLA design is to provide a parallel path for carry propagation that helps to reduce the overall adder delay.a binary to BEC-based CSLA. The BEC-based CSLA involves less logic reso4urces than the conventional CSLA, but it has marginally higher delay.

BINARY TO EXCESS- 1CONVERTER

The main idea to implement conventional CSLA with BEC instead of RCAs in order to reduce the area so automatically it reduces the power consumption and improves the system performance.as we know the operation of binary to excess code suppose if gives the binary number 0000, the BEC is 0001 so it increased by 1 means there is no wait of carry propagation due to this speed increases.in this project the BEC has several modules such as carry and sum units.

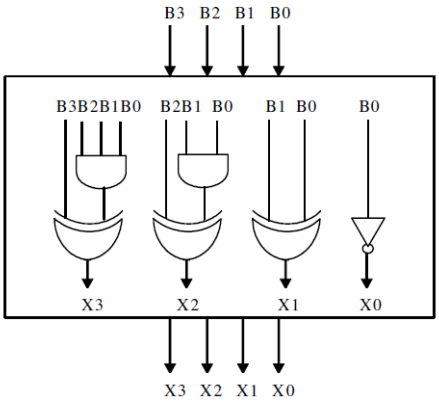

Fig 3. Binary to excess -1 converter

The basic work is to use binary to excess -1 converter (BEC) in the regular CSLA to achieve lower area and increases speed of operation this logic is replaced in RCA with cin=1 . this logic can be implemented for different bits which are used in the modified . design the main advantage of this BEC logic comes from the fact that it uses less number of logic gates than the n-bit full adder structure. As stated above the main idea of this work is to use because instead of RCA with cin=1 in order to reduce the area and the speed of operation in the regular CSLA to replace the n-bit RCA, n+1 bit logic is required.

RESULTS AND DISCUSSION;

The reduced logic CSLA has one Half Sum Generation (HSG) unit, one Full Sum Generation (FSG), one Carry Generation (CG) unit, and one Carry Select (CS) unit The carry generation unit is constructed by two CGs (CGand CG). Initially then bit operands (A & B) are given as the input to the HSG unit. The HSG unit generates half sum and half carry. Both CG and CG receive the sum and carry generated by HSG. The CG0 and CG1 units have theoptimized designs for fixed input carry bits. The Carry Selection unit selects the carry among the two carriesbased on the control signal. According to the selected carry the FSG unit generates the full sum word.

ADDERS	POWER(mw)	AREA(micro metre^2)	GATES
CSLA	1.109	6201	600
RCA	0.206	2214	200
BEC-1	0.05	1154	105

Table .1 CSLA Power and Area.

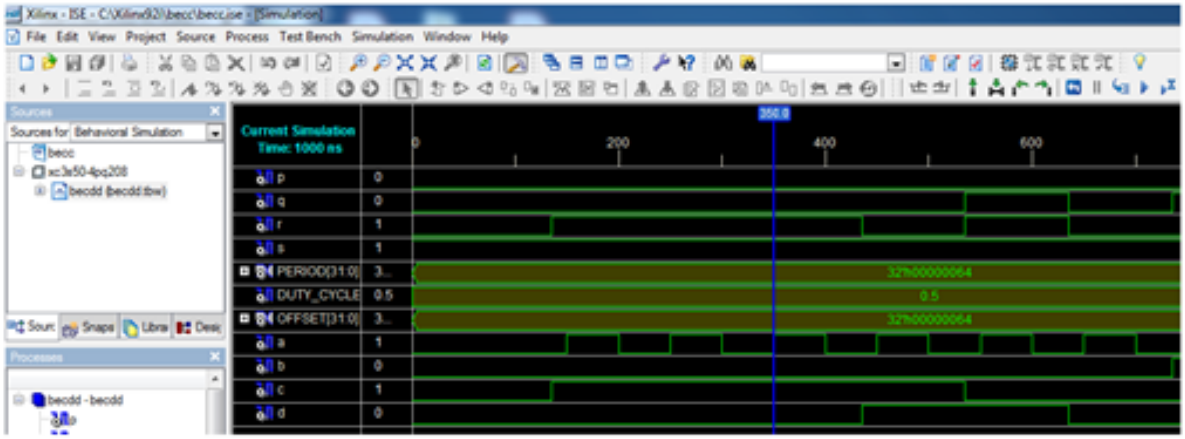

Fig .simulation results for CSLA using binary to excess-1 converter

CONCLUSION;

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic logic unit, the adder structures become a very critical hardware unit. In any book on computer arithmetic, someone looks that there exists a large number of different circuit architectures with different performance characteristics and widely used in the practice. Although many researches dealing with the adder structures have been done, the studies based on their comparative performance analysis are only a few. Digital Adders are the core block of DSP processors. The final carry propagation adder (CPA) structure of many adders constitutes high carry propagation delay and this delay reduces the overall performance of the DSP processor. In this project, qualitative evaluations of the CSLA adder with and without BEC architectures are given. Among the huge me0mber of the adders we wrote VERILOG (Hardware Description Language) code for Carry skip and carry select adders to emphasize the common performanceproperties belong to their classes. With respect to delay time and power consumption we can conclude that the implementation of CSLA with BEC is efficient. The main advantage of t hi s BEC l o gi c come s from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

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