A COMPREHENSIVE SURVEY ON DISTINCTIVE IMPLEMENTATIONS OF CARRY SELECT ADDER

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Abstract **–**VLSItechnology is everywhere in digital world. The real applications of VLSItechnology are personal computers, cell phones, digital camera or camcorders. The important parameters for these applications are speed, area and power consumption. The main component of modern digital devices is adders. In signal processing adder plays a vital role. We have many kinds of adders. Each adder has its own functionality. To reduce the fundamental problems i.e., speed, area and power, many new adders are invented. Carry select adder(CSLA) is the important adder among the adders. The propagation delay of carry select adder(CSLA) is better than other adders but the key issue is with its power consumption and area. In this brief, we have discussed about different implementation logics of carry select adder(CSLA) and the comparative analysis has been done for different types carry select adders(CSLA).

Key words – RippleCarry Adder(RCA),Carry Select Adder(CSLA),Binary to Excess-1 Converter(BEC), Combination Boolean Logic(CBL), D-latch.

I. INTRODUCTION

Very large scale integration(VLSI) is one of the most widely used technologies for microchip processors, integrated circuits(IC) and component designing. Such applications require high speed, low power and less area. One of the most trending areas for research in VLSI system design is the designing of area, power efficient, high speed data path logic systems. In order to get the VLSI circuits with small computational delay, we have to change the adder circuit. Adder is the basic component of central processing unit(CPU), arithmetic logic unit(ALU). ALU performs both logical and arithmetic operations such as AND, INV, OR, comparison, multiplication, division, addition, subtraction. Adder circuit is the part of all the operations.

An adder takes the inputs in the form of binary format, performs addition operation. Apart from ALU, it is also used in other applications like digital filter applications, digital transformation applications (FFT, IFFT etc.), digital modulators, image processing. Adder circuit has a very impact on the most of the applications. The performance of adder plays a key role for such applications. So, the VLSI system designers need to concentrate on, hoe to increase the speed. Also, there is a necessity to minimize the chip area as well as power consumption. Now-a-days portable devices have a high demand. Example for such devices is mobile phones. So, there is a balance required in between speed, area and power consumption.

Half adder was the basic adder. It takes two inputs and generates the outputs as sum and carry. After half adder, full adder (FA) was invented. Full adder takes three inputs and gives two outputs. When full adders are connected in series, the carry out of one full adder was given as carry in for the next full adder. This makes the great advantage for full adder but with increasing computational delay.

There are many types of adders are invented such as ripple carry adder (RCA), carry look ahead adder (CLA), carry select adder (CSLA), carry skip adder (CSKA) and carry save adder (CSA). Among all ripple carry adder was easy to fabricate but its computational delay is more i.e., speed is less. In order to overcome delay, carry select adder (CSLA) was proposed. CSLA was constructed by two ripple carry adders (RCA) and outputs are selected by multiplexers. To improve the efficiency add-on circuit was used in CSLA.

This paper organized as follows: section II describes about basic modules, section III explains about literature review of CSLA. Section IV describes about comparative analysis of different CSLA. In section V conclusion has been done.

II. BASIC MODULES

1. RIPPLE CARRY ADDER (RCA):

Since full adder performs the addition of two one bit inputs. To calculate addition of multiple bits ripple carry adder (RCA) was used. Ripple carry adder (RCA) was constructed by connecting the full adders in series. Each full adder carry out was given as carry in to other full adder. The outputs of full adders give the sum of input binary numbers. Using RCA we can perform N-bit addition. N-bit addition requires N-bit full adders. The circuit diagram of 4-bit ripple carry adder is given below.

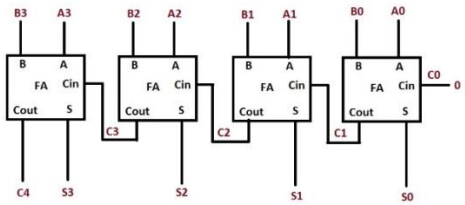

Figure -1: 4-bit ripple carry adder

The advantage of ripple carry adder (RCA) is the circuit fabrication is easy among the other adders. Since, it has less circuit complexity. The major drawback of ripple carry adder (RCA) is its speed. Since, every full adder was waiting for carry input which comes from previous full adder. This connection increases the computational delay. For N-bit addition the total delay of ripple carry adder is given as, Total delay=(N – 1)tc+ts.

As bit size increases, the number of full adders is increases. This makes the increase in circuit area which causes more power consumption.

2. CONVENTIONAL CARRY SELECT ADDER (CSLA):

The figure shows below is a 16-bit conventional CSLA.

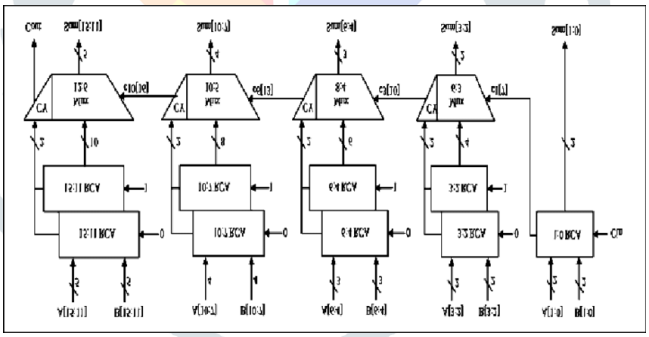

Figure-2: 16-bit conventional CSLA

The solution for computational delay of ripple carry adder is carry select adder (CSLA). CSLA has less computational delay than ripple carry adder (RCA) but its area is very large.

The conventional CSLA was constructed by 5 groups of ripple carry adders (RCA) with different size. Each ripple carry adder (RCA) generates the sums for carry-in =0 and carry-in =1. The outputs are selected using a multiplexer with carry-in as selection line. The sum and carry equations are given below.

S(i)=A(i) XOR B(i) XOR C(i-1)

C(i)=(A(i) AND B(i)) OR (C(i) XOR A(i) XOR B(i))

Conventional CSLA is very faster than ripple carry adder (RCA) with less computational delay but it is not an area efficient. To enhance the performance later CSLA was replaced by different add-on circuits.

III. LITTERATURE SURVEY

This paper [1] investigated on the add-on circuits of CSLA. The CSLA has two ripple carry adders (RCA). One with carry-in=0 and another with carry-in=1. In this paper the ripple carry adder (RCA) with carry-in=0 was not disturbed. The ripple carry adder (RCA) with carry-in=1 was replaced by binary to excess-1 converter (BEC). Since the difference between sums of two ripple carry adders in conventional CSLA is 'one'. The binary to excess-1 converter (BEC) is a special type of logic whose inputs are in binary format and gives the output which is same as by adding one to the input binary number. The binary to excess-1 converter (BEC) takes the inputs which are the outputs of ripple carry adder (RCA) with carry-in=0. For N-bit ripple carry adder (RCA) requires (N+1)-bit binary to excess-1 converter. The outputs of binary to excess-1 converter were given to multiplexer. Multiplexer has carry-in as selection line and gives final sum and carry. When compared to conventional CSLA the area was decreased with this implementation but delay was increased.

In this paper [2] the redundant cells used in conventional carry select adder (CSLA) was eliminated. They proposed a new logic for implementing the carry select adder (CSLA). By analyzing the truth table of full adder, they find out a new logic. For carry-in=0, the output sum of full adder follows the XOR logic and output carry following the AND gate logic. For carry-in=1, the output sum following XNOR logic which is inversion to the XOR i.e., output sum with carry-in=0. Output carry following the OR gate logic in case of carry-in=1. These XOR output and its inversion given as two inputs for a multiplexer whose selection line is carry-in. The output of multiplexer gives final output sum. The AND gate and OR gate outputs given to another multiplexer with same selection line i.e., carry-in. The output of multiplexer is given as carry-in for another block. By using this connection, the gate count almost reduced to half when compared to conventional CSLA. We can save 70% power compared with CSLA and 2% increase in power compared with ripple carry adder. The speed is little slower than CSLA because of a shortage of parallel path in the design.

This paper [3] proposed a new logic for designing carry select adder(CSLA). The proposed logic contain four blocks, half sum generation (HSG), full sum generation (FSG), carry generation (CG), carry selection (CS). Carry generation consists two carry blocks CG0 and CG1 corresponding to the carry-input 0 and 1. The HSG block takes the binary inputs and gives the outputs as half-sum and half-carry. The CG block generates the two full carry words for corresponding to the carry input 0 and 1. The CG block equations are same as full adder carry equations. In general, CS block consists of a multiplexer with carry-input as selection line. However, the carry words follows a specific bit pattern. So, the optimization of CS unit has been done. CS unit has AND-OR gates which decides the output carry words depends on the carry-input. After selecting the final carry words, the FSG unit generates the output sum by using carry words and half- sum. This design technique has less area and delay than BEC based CSLA. The area-delay-product (ADP) was 35% less than the BEC based CSLA.

This paper [4] replaced the BEC logic with D-latch for area efficient, low power and less delay. D-latch is a one bit storage device with enable signal. When enable signal is HIGH i.e., 1, the D-latch copies the input to the output. When enable signal is LOW i.e., 0, the D-latch is in off state and outputs are remain unchanged. The clock signal is given as one of the input to the full adder along with binary inputs. When clock signal is HIGH, it performs addition for carry-in=1 and if clock signal is LOW, it performs addition for carry-in=0. The output sum of full adder was given to D-latch and output carry was given to carry-in for other full adder. The outputs of D-latch was given to a multiplexer along with output sum of full adder. The multiplexer selection line is carry-in. When clock signal is HIGH, full adder performs addition and given it to D-latch. The same clock is applied to D-latch. So, the D-latch copies the input sum to the output which is fed to a multiplexer. Similarly, when clock pulse is LOW, the full adder does same work and here D-latch does not copies the input. The multiplexer selects the output depends on the carry-in value. The D-latch implementation has less area, power consumption and delay as compared with BEC based CSLA.

This paper [5] investigated on the area and power consumption of CSLA. The CSLA using D-latch has less area, power consumption with high speed. The aim of the designers is to reduce the chip area and power consumption. A 16-bit CSLA using D-latch uses 4 multiplexers. The gate count for multiplexer is 4. In order to enhance the performance of CSLA using D-latch, the multiplexers are modified. To achieve effective area and power consumption. The last stage and first stage of CSLA with D-latch was modified and constructed without using the multiplexer. The circuit was modified by using full adder sum and carry equations. The multiplexers are removed in these stages which means area efficient is achieved. Since the proposed design uses less gates than the exiting design. The major drawback is it have more propagation delay than the existed D-latch adder. The proposed design uses 6.28% less power and 7.62% less are than D-latch adder for a 16-bit operation.

IV. COMPARATIVE ANALYSIS

Sl.No	Authors	Implementation Logic	Advantage	Disadvantage
1.	Pallavi Saxena, Urvashi Purohit, Priyanka Joshi	CSLA with binary to excess-1 converter (BEC).	Less area and power than conventional SLA.	Delay was increased.
2.	I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng	CSLA by sharing the common boolean logic (CBL).	Gate count reduced to half and decrease in power consumption.	The proposed design is little bit slower than conventional CSLA.
3.	Basant Kumar Mohanty, Sujit Kumar Patel	CSLA using HSG, FSG, CG and CS unit.	Less propagation delay than CBL and BEC based CSLA.	Slightly more area than CBL based CSLA.

Table1: Detailed analysis of different CSLA adders

Sl.No.	Authors	Implementation Logi	Advantage	Disadvantage
	Sakshi Bhatnagar, Harsh Gupta and Swapnil Jain	CSLA with D-latch.	Requires less delay than BEC based CSLA.	More area than CBL and BEC based CSLA.
5.	Avinaba Tapadar, Sujan Sarkar, Ayan Dutta, Jishan Mehedi	CSLA with D-latch	Less area and power consumption than CSLA with D-latch.	More delay than CSLA with D-latch.

Table1: (Table1: Contin…)Detailed analysis of different CSLA adders

V. CONCLUSION

In this paper we have discussed about different implementations of carry select adder (CSLA). Since some of the designs are good enough with area and other designs have less propagation delay. There is a balance required between the chip area and propagation delay. CSLA with BEC have more area and delay than all other designs. CSLA with D-latch has the less propagation delay among other CSLA designs. After that, the CSLA with HSG, FSG has a better performance regarding propagation delay. CSLA with modified D-latch has more propagation delay than the CSLA with D-latch. The CSLA with CBL has very less area than other designs. It is more area efficient design. CSLA with HSG, FSG has a slight increase in area than CSLA with CBL but its propagation delay is more. Taking chip area into consideration, CSLA with CBL is the most efficient design and considering propagation delay CSLA with D-latch has a better performance. By analyzing above papers we are working on design for CSLA which has less area, power consumption and having more speed.

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