# LOW POWER ARCHITECTURE OF RADIX-8 SDC FFT FOR OFDM WIRELESS COMMUNICATION SYSTEMS

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***Abstract*- Fast Fourier Transform (FFT) is a primary element of many multiple digital signal processing (DSP) systems. FFT processor is one of the high computational complexity modules in the physical layer of Orthogonal Frequency Division Multiplexing (OFDM). Wireless data transmission techniques face a lot of challenges in the current world. In this paper, low power architecture of Radix-8 Single path Delay Commutator (SDC) Fast Fourier Transformation (FFT) for OFDM system has been designed for performing frequency transformation techniques.Radix-8 FFT, which is used to enhance the speed of functioning by reducing the computational path. In the proposed new architecture named as "Radix-8 SDC FFT". The performance evaluation of Radix-8 SDC FFT architecture has been determined through Very Large Scale Integration (VLSI) system design environment. In the VLSI system design, less area utilization, low power consumption and high speed are the main parameters.**

***Keywords*- FastFourier Transform(FFT), Orthogonal Frequency Division Multiplexing (OFDM),SinglePath DelayCommutator (SDC), Digital Signal Processing (DSP).**

## I. INTRODUCTION

Fast Fourier Transform (FFT) is a technique widely used in many communication systems. The purpose of the FFT is changing one form of signal into another form of signal. In general FFT is a frequency transformation technique, it is used to convert time domain signal into frequency domain signal. The transformation of signal helps to improve the signal rate. The time domain signal can be recovered by applying Inverse FFT process for getting the time domain signal from the frequency signal. FFT can be applied into many application one of the main application is orthogonal frequency division multiplexing (OFDM), software defined radio (SDR) MIMO based applications and so on.

Pipelined based FFT architecture; it is designed and implemented by using clock based processing elements. Frequency transformation structures such as SDF, SDC, MDF, and MDC are preferred to increases the efficiency of frequency transformation Single path Delay Commutator (SDC) architectures are used to perform the process known as frequency transformation. Bit Parallel Multiplier (BPM) based FFT architectures are designed to improve the performances and computation speed.

Various FFT processors have been proposed to meet the real-time processing requirements and to reduce hardware complexity, which are especially important for high throughput applications. Orthogonal Frequency Division Multiplexing (OFDM) and Software Defined Radio (SDR) technology brings cost efficiency, flexibility and power to drive and establish long distance communications. In this paper, implementation of Radix-8 SDC FFT for OFDM wireless communication system. The main goal of proposed architecture is to reduce hardware complexity, power consumption and increasing both speed and throughput of the system.

## II. RELATED WORKS

The efficient implementation of Radix-8 Fast Fourier Transform (FFT) algorithm has been explained in [1]. High radix FFT algorithm contains many advantages, obviously radix-8 have less multiplications and taking less memory for accessing the process. So the power consumption is also reduced in the process. But one drawback in the high radix butterfly is complex multiplication. It required more complex multiplier for FFT operation [2]. The more number of complex multiplier occupy more area, so the complexity is increased in the processing element. To avoid the area complexity using a cascaded parallel multiplier, so the usage of complex multipliers is reduced.

An OFDM system transmit the data over a channel with number of carriers [3], each and every carrier is orthogonal to each other. Fast Fourier transform (FFT) and inverse fast Fourier transform (IFFT) pairs are used in the OFDM system [4], because of its high efficiency. In normal FFT/IFFT architecture achieving higher rate of processing, but it occupy more silicon area and it also consume more power to process the elements. To avoid the problem in the OFDM system, using pipelined FFT/IFFT architecture and memory based architecture was developed [5].

The new radix-2/8 FFT is described in for performing the discrete Fourier transform in [6]. It reduces the complexity of the operations such as data transfer, generation of address, evaluation of twiddle factors and lookup table accessing. The arithmetic operation such as multiplication and addition of the proposed method is same as the existing split radix

FFT. The proposed method uses the mixture of radix-2 and radix-8 FFT. The proposed algorithm reduces the computational complexity and arithmetic complexity.

Different types of radix algorithms are used[7] in the FFT processor. Power consumption, hardware cost and memory requirement of each radix is varied in the FFT processor. Radix-2 FFT algorithm is an efficient method to compute the Discrete Fourier transform. Radix-2 takes more time to perform the operation, and also it takes more complex multiplier for twiddle factor multiplication. Radix-4 is the improved version of radix-2; it reduces the stages of butterfly operation. It improving the speed and reducing the computational cost of the processor.

## III. Proposed Radix-8 SDC FFT Structure

In this paper, architecture of Radix-8 Single path Delay Commutator (Radix-8 SDC) FFT has been designed to reduce the hardware utilization, power consumption and to improve the speed of the processors. Radix-8 FFT algorithm which was observed to develop the speed of functioning by reducing the calculation, it can be obtained by changing the base to 8. FFT algorithms using higher radix can be designed by decomposition of the frequency domain samples into more groups at the cost of more difficult control. Single path delay Commutator improves the utilization of the butterfly elements by modifying the butterfly elements. However, increases the memory requirement. The number of words which are required to be stored is 3N/2, 3N/8… 6. Commutator is used to convert the one form of signal to another form of signal. Compared to radix-2 and radix-4 FFT, Radix-8 FFT has reduced the number of stages and also gives the better performance of the architecture. SDC architectures are presented for improving the architectural performances in terms of VLSI main concerns, in this proposed architecture. The numbers of stages are reduced in this method. SDC has also reached the minimum requirement for both multiplier and adder.

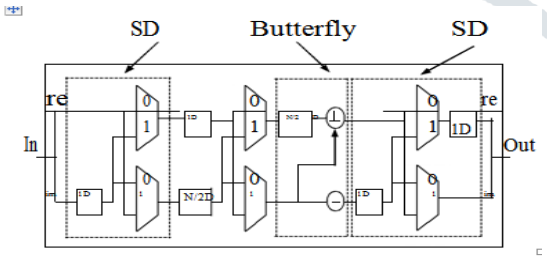


*Fig. 1 Radix-8 SDC FFT for OFDM system*

## IV. Results and Discussion

Radix-8 SDC FFT architecture has been designed for OFDM wireless communication system and simulated by using Modelsim 6.3C tool. The simulation result of 8-point Radix-8 SDC FFT is shown in Fig.2.The performance of proposed method has been improved in terms of less silicon area utilization, high speed and lower power consumption than the existing method.

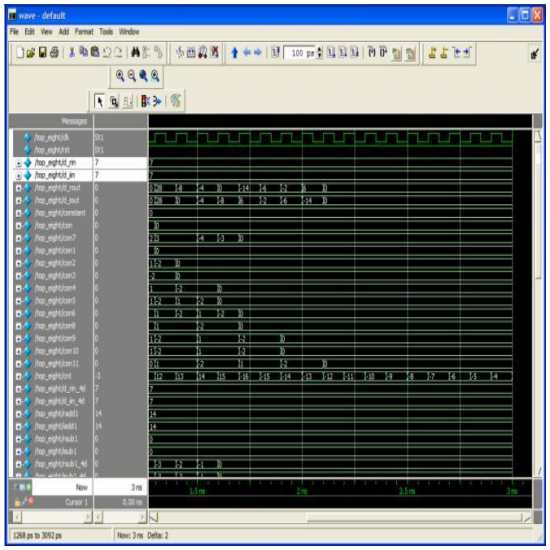

*Fig. 2 Simulation result of Radix-8 SDC FFT*

*Table 1 Comparison of Existing Radix-8 SDF FFT and proposed Radix-8 SDC FFT*

| Types/ VLSI concerns | Number of Occupied Slices | Total Number of LUTs | Power (W) |
|---|---|---|---|
| **Existing Radix-8 SDF FFT** | 343 | 674 | 0.727 |
| **Proposed Radix-8 SDC FFT Method** | 324 | 535 | 0.691 |
| **Percentage Reduction%** | 5.50% | 20.60% | 4.90% |

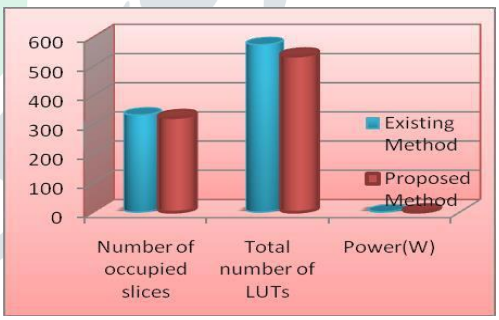


*Fig. 3 Performance Evaluation of Proposed Radix-8 SDC FFT*

## V. Conclusion

In this paper, designed an efficient approach to perform the high-radix butterfly elements. Low power architecture of Radix-8 SDC FFT has been proposed for OFDM wireless communication system. In this method, pipelining techniques are used to cascade the butterfly elements and thus the silicon area for high radix butterfly is significantly reduced. The advantages of this method are high throughput and small area. Therefore, the proposed method offers 5.5% reduction in slices, 20.6% reduction in LUTs and 4.9% reduction in power consumption. This type of FFT architectures can be used in major of the communication systems like OFDM. When compared with existing method, proposed architecture gives better performances.

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