DESIGN OF TREE BASED MULTIPLIER (TBM) FOR HIGH SPEED APPLICATIONS

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Abstract **– In this paper, we present the low power based high speed Tree based multiplier (TBM) architecture and the performance analysis of tree based multiplier (TBM) with the conventional multiplier design. The speed and efficient level of the proposed architecture is achieved by improving the conventional tree based multiplier (TBM) stage with the proposed AND-OR invert (AOI). There are two basic methods are used to propose the efficient architecture such as AND-OR invert (AOI) and OR-AND-invert (OAI). Proposed architecture is designed with the advanced adder technology with the low area and power. Modelsim XE tool is used to evaluate the simulations and Xilinx ISE is used to estimate of the synthesis of the proposed architecture.**

Key words**: Carry skip adder, AND-OR invert, OR-AND invert. Nanometer.**

I. INTRODUCTION

Expansion of standard mobile and wireless network communication applications have large demands on signal processing. Traditional signal processing approaches are filtering, convolution, correlation and transformation of signals. Among these approaches, filters are widely used in wireless mobile and network applications to filter the services of incoming and outgoing users.

Primary function of a filter is to selectively allow the desired signals to pass through and suppress undesired signals based on frequencies. Filters are broadly classified into two types namely, analog filter and digital filter. Large endeavours have been suggested the suitability of digital filter for wireless communication application.

Aim of such approaches is to improve the performance of Multiplication and Accumulation (MAC) unit in terms of less area utilization and lower power consumption. Hence, high performance of adder and multiplier structures is necessary to improve the efficiency of MAC unit.

II. RELATED WORKS

Ramesh Babu M et al [1] proposed an efficient low power ripple carry adder (RCA) for ultra applications. The main objective of this work is to reduce power dissipation by eliminating PMOS tree and also by retrieving the energy stored at the output by reversing the current source direction discharging process instead of dissipation in NMOS network with domino logic, pass transistor logic. The performance of the circuit increases due to elimination of power consumption. Further a comparison of the performances of dual rail domino logic and CPL adder circuits with traditional adder circuits has been presented. Also, a four bit ripple carry adder was designed using adiabatic logic and is considered as a benchmark circuit for future design.

Carry Select Adder (CSLA) is introduced to improve the performance of digital addition operation as described by Laxman Shanigarapu [2], In this work, D-Latch is used instead of RCA in CSLA circuit. Cascade of RCA structures exhibit more delay and area for performing addition operation. But, D-Latch circuit reduces the area and delay for exhibiting addition operation. A unique approach is proposed in this article to reduce area, delay and power of SQRT CSLA. The proposed SQRT CSLA structure is compared with regular SQRT CSLA which results in developed architecture, consuming less area and delay than regular one.

Muhammad Ismail et al [3] proposed the 8-bit RCA by using CMOS circuits, pass transistors and transmission gates. To design 8-bit ripple carry adder, 1-bit ripple carry adders are considered as basement. Schematic design of developed 8-bit adder is converted into layouts for verification. Further, simulation of the schematic designs is carried out to check the logic operations. In the end, performance analysis with respect to power dissipation of layout designs is analyzed with previous work. Finally, this work concludes that the CMOS technologies are most power effective for improving the performances of digital circuits. Hence, it is further recommended to use the CMOS logic for the design of portable embedded system industry.

Rajendar Kumar [4] developed the 4-bit, 8-bit and 16-bit Carry Look-ahead Adder (CLA) using Very High speed integrated circuit Hardware Description Language (VHDL). Propagation delay of RCA circuit has been reduced in this work. It occupies less area in terms of LUT, slices and total number of gate count. As well as delay path also reduced significantly in carry look-ahead adder when compared to Ripple Carry Adder. The main disadvantage of this work is that it is not possible to realize constant delay for wider bit adders, because there will be a substantial loading capacitance and hence it consumes more than considerable complexity.

Ravish Aradhya H. V et al [5] proposed the Hybrid Carry Look-ahead Adder (HRCLA). HRCLA has been designed by rippling the last carry bit of a 4-bit CLA. A four bit HRCLA has been implemented by using Cadence using 45nm technology. The implementation results show that the 12.2% of Area,

4.6% of power improvement and 14.01% of critical path delay overhead over CLA. This high level of performance is achieved by minimum delay full adder. This work would be useful for MAC design of FIR filter, FFT and other digital signal processing applications.

Murthy P.H.S.T [6] proposed the CLA adder design by using Multi-input Floating Gate (MIFG). Low voltage and low power circuits are essential for mobile gadgets which generally have mixed mode circuit structures embedded with analog sub-sections. Generally by using the reconfigurable logic of multi-input floating gate MOSFETs, 4-bit full adder has been designed for 1.8V operation. Multi-Input Floating Gate (MIFG) transistors have been anticipating in realizing the increased functionality on a chip. A multi-input floating gate MOS transistor accepts multiple inputs signals, calculates the weighted sum of all input signals and then controls the ON and OFF states of the transistor. Implementing a design using multi-input floating gate MOSFETs brings down transistor count and number of interconnections. Design of Carry look-ahead

adder is tested using 45nm technology and extended to ALU in this work. The proposed circuit has been implemented in 45n-well CMOS technology.

Modern electronic devices require a less expensive, compact and power saving technology design for signal processing functions like filter, correlation, convolutions and frequency transformation. Computational units like multipliers and adders are some vital components of those systems working with this target. Among the adders available and used, Carry select adders are the fastest adders as in Venkata Sateesh B [7]. Here, Dual ripple carry adders - one for CIN = 0 and other for CIN = 1 are used. To reduce Propagation delay of generated carry, Carry look-ahead adders are used instead of ripple carry adders. To enhance the performance, Binary to Excess 1 Conversion circuit is used instead of RCA for CIN = 1. Hence, low area and high speed is achieved in dual RCA based CSLA over Carry look-ahead adder.

III. PROPOSED PARTIAL PRODUCT GENERATOR (PPG) ARCHITECTURE

Wallace tree multiplier [Wallace, C.S.1964] performs multiplication of two unsigned integers basically. It reduces the number of partial products stages as two at the end of the reduction process. Wallace tree multiplier has three steps:

a). Partial Product Generation (PPG) Stage

b). Partial Product Reduction (PPR) Stage

c). Partial Product Addition (PPA) Stage

Partial Product Generation (PPG) stage

Partial product generation is initial step in binary multiplier. Partial products generation (PPG) stage is the beginning stage in which the multiplicand and the multiplier are multiplied bit by bit to execute the partial products. These values are intermediate values which are generated based on the value of multiplicand and multiplier. If the value of multiplier bit is “0”, then partial product row is simply zero, and if it is “1”, the multiplicand will be printed. From the 2nd bit of multiplication, each partial product row value is shifted left one unit. Partial product generator reaches the highest reduction in the number of partial products for a radix-4 multiplier (78%), by joining advantages of redundant binary encoding with redundant binary addition. Partial products are implemented with Radix-4 modified booth recoding. Partial product generators [Priyatharshne, T.N. et al. 2014] are done only by using of a series of logic AND gates. Figure 1shows partial product generation of Wallace multiplier.

The most important operation in the process of multiplication is addition of the partial products which was produced. Performance of the multiplier mainly depends on the performance of the adder. In the partial product generator circuit, high-radix RBBE needs high fan-in gates. Since the circuit for each and every digit of the RB partial product will be duplicated in a large number, the general of high fan-in gates is more prominent in long operand length multipliers. Booth encoded digit is utilized for one RB partial product, half of the binary bits representing an RB partial product generated from a simple power-of-two multiple in the RBBE are filled with “0”s, which is rather inefficient. Booth encoder and partial product generator change the efficiency of the partial product generation. The number of partial products that can be stored by this stage impacts the cost, performance and power consumption.

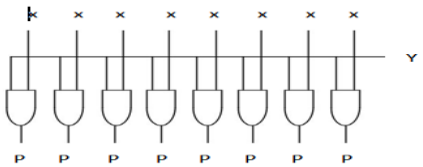

Fig. 1 Partial Product Generation Stage of Wallace Multiplier

Partial Product Reduction (PPR) Stage

Partial product reduction (PPR) is the second stage which is the most important as it is the most sophisticated and that calculate the speed of the overall multiplier and the end of the addition stage or carry- propagate addition(CPA) using different compressors. It consists of transforming all the developed products into only two. This stage takes a large amount of time in relation to the total delay of the operation. The design [Waters, R.S. et al, 2010] analysis starts with multiplication process by Wallace Tree multiplier. Figure 2 shows the algorithm for 8 x 8 multiplication using Wallace Tree multiplier.

In Partial Product Reduction stage has five stages to complete the multiplication process. Each stage uses half adders as well as full adders. If there any 1-bit individual in arrow, it will pass to the next stage without any processing. First of all, we have to reduce the partial products using half adders and full adders until two rows of partial products left. By using a fast carry-propagate adder, final stage add the remaining two rows to improve the speed of the multiplication process within the computational unit, there is a bottleneck that is needed to be assumed partial products reduction network which is used in the multiplication segment. For implementation of this stage require addition of large operands that

involve long paths for carry propagation. The partial product reduction is based on the stored logic paradigm. It is used in a complementary way to the combinational design. The technique consists of storing the results of any combination of operands for the function desired in an attached memory.

SIMULATION RESULTS AND ANALYSIS

In figure 2, it shows multiplicand and multiplier in the form of a and b. Then multiplier result is represented as final. First of all it takes one clock cycle for initialization of the result. Here initialization input reset is as "0" at the time final value is "0000000000000000". For next clock cycle "a" is given as "00110111" and "b" as "00011001", the final value is "0000010101011111".

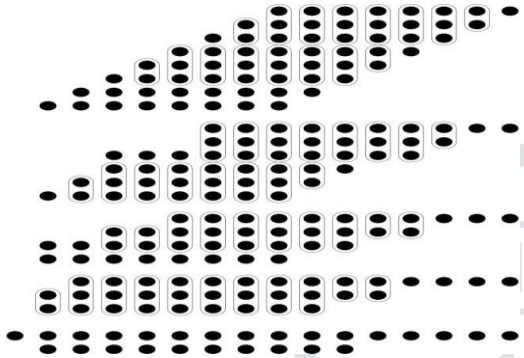

Fig.2 8x8 Wallace Tree multiplier

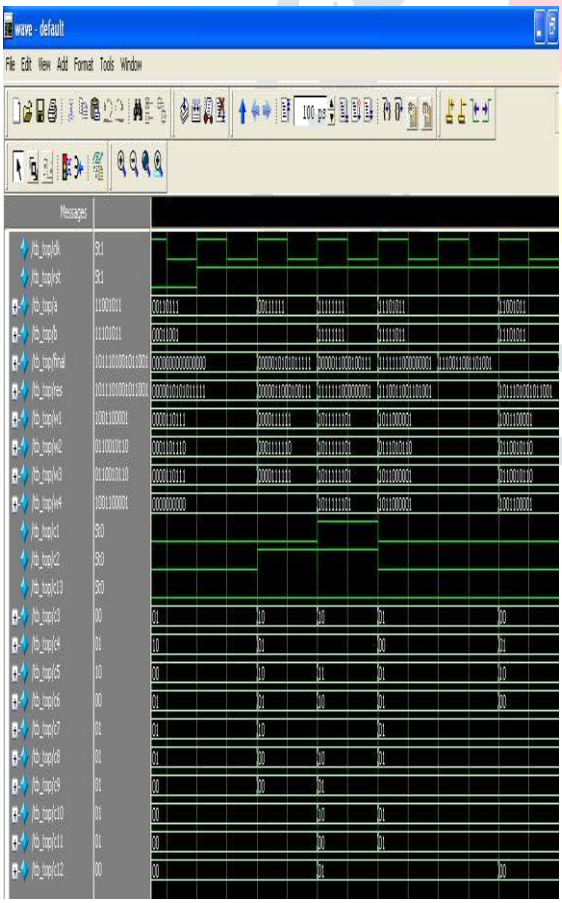

Fig.3 Simulation Result of Mux-based Multiplier

Table 1- Result Analysis of ConventionalMultiplier

STRUCTURE	CONVENTIONAL MULTIPLIER ARCHITECTURE			
BIT SIZE	8 BIT	16 BIT	32 BIT	64BIT
NUMBER OF4 INPUT LUTS	170	717	2964	9046
SLICES	95	397	1658	4798
SLICES FLIP FLOPS	32	64	128	256
DELAY DURING BEFORE CLOCK (NS)	22.325	42.774	89.145	130.65
POWER	13.487	40.697	80.121	161.097

Table 2 Result Analysis of Proposed Multiplier

STRUCTURE	PROPOSEDMULTIPLIERARCHITECTURE			
BIT SIZE	8 BIT	16 BIT	32 BIT	64BIT
NUMBER OF4 INPUT LUTS	170	713	1427	3689
SLICES	93	400	1104	2451
SLICES FLIP FLOPS	32	64	79	189
DELAY DURING BEFORE CLOCK (NS)	22.327	34.147	68.26	110.36
POWER	21.698	31.487	68.214	148.25

IV. CONCLUSION

This paper presents a Tree based Multiplier (TBM) with help of wallace stage. This reduces N rows of partial products into N/2 rows of partial products with slight increase in bit-lengths. Due to lesser number of partial products, the number of adders used to make partial product addition is also less. Due to its less area and low power performance, Tree based Multiplier (TBM) will be implemented in some applications such as Finite Impulse Response (FIR) filter, Digital Signal Processor (DSP) and Arithmetic Logic Unit (ALU) in future.

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