Design and Analysis of Low power,High Speed PLL Frequency Synthesizer using Dynamic CMOS VLSI Technology

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***Abstract*— Power and speed are the important parameters in various communication systems. Phase locked loop (PLL) is an efficient method used in frequency synthesis. A dynamic logic based CMOS is proposed to design phase detector, VCO and loop filter. The CMOS dynamic logic is the fastest logic in all the CMOS logic families. The DSCH3 tool is used in the design of logical circuits and microwind2 tool using 90nm CMOS technology is used to measure the parametric analysis. The speed of transition time between the synthesized frequencies gives the bandwidth of loop filter. In the dynamic CMOS logic PLL, the power is reduced to 0.196mW and speed is improved to be 5.31GHz.**

Keywords—CMOS Dynamic logic, PLL, VCO, DSCH3, Microwind 2.

I. INTRODUCTION

Low power design is necessary to extend the operating time of integrated circuits (ICs) as well as to reduce the packaging and cooling costs. As the scale of integration keeps growing, more and more complex signal processing systems are being implemented on a VLSI chip. These signal processing applications consume considerable amount of energy. The trade-off of performance and area remain to be the two major design factors, high power consumption is critical in today's VLSI system design. The need for low power VLSI system arises from two main forces. First, Static power dissipation is due to the leakage current. Second, Dynamic power dissipation is due to the transition activity that dominates the total energy dissipation due to charging and discharging of capacitors. Phase Locked Loop (PLL) circuits are used for frequency control. PLL can be used as frequency multipliers, demodulators, tracking generators or clock recovery circuits. In PLL the output signal is continuously compared with the input signal. If the output signal phase is same that of input signal, the PLL circuit will lock the signal. In this paper we proposed CMOS VLSI dynamic logic to get high speed, less area and reduced power of the PLL system.

A PLL-based frequency synthesizer is one of the control systems that generates radio-frequency (RF) signals from a clean low-frequency clock. During input phase lock condition, it enables the VCO to repeat and track the frequency. The PLL can trace the input frequency in addition to synchronize the signals. PLL generates the output frequency which is equal to the multiple of input frequency.

The basic functional block diagram of PLL is shown in Fig.l. The output frequency is continuously monitoring with the input frequency and number of repeating iteration will reduce the phase difference. It consists of three blocks namely,

- Phase detector
- Low pass filter
- Voltage controlled oscillator

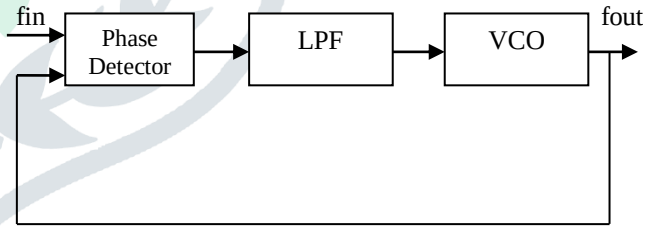

Fig.1. Block Diagram of PLL

II. RELATED WORKS

[1] Introduced a design aspect for low power phase locked loop using VLSI technology where it is designed using 45nm process technology parameters, which in turn offers high speed performance at low power.[2] Problem between channel spacing and loop bandwidth is reduced.[3] It has presented the comparison of design and simulation of a chip layout of fractional –N phase locked loop for wireless application using 45nm and 32nm VLSI technology.[4] Discussed the comparison of Low power and low jitter phase

frequency detector and found high speed phase frequency detector is the best.[5] In the dynamic CMOS logic PLL the power is reduced to 0.l3mW and Speed is improved to 0.50GHz.

III. DESIGN

A. CMOS Dynamic Logic Phase Detector

The phase detector compares two signals with respect to their phase. There are two basic types of the phase detectors these are analog and digital. In development of the analog filter, the multiplier circuit is applicable. It will take a product of two signals and shows resulting signals. For development of digital phase detector, we are using a XOR logic gate. The XOR gate is designed by using various logic gates i. e. AND and OR gate. In this phase detector design, we used XOR implementation using CMOS dynamic logic shown in Fig.2. The numbers of transistors are reduced in XOR logic. In order to achieve high speed of operation with less power, CMOS dynamic logic has been chosen. When the phase of input and output signals are same then the XOR gate's output will be logic zero. When the phase of input and output signals are not same, the output will be logic one.

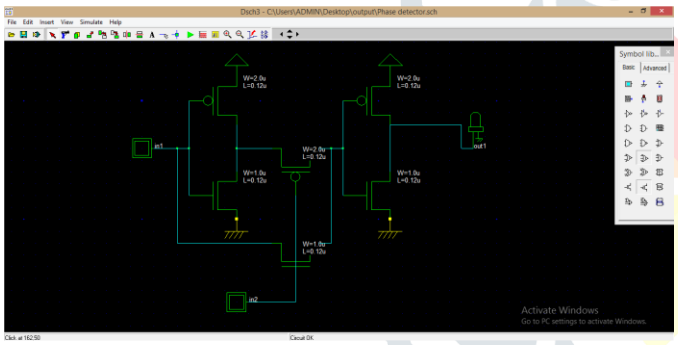

Fig. 2. DSCH3 Layout Of Phase Detector

B. CMOS Dynamic Logic Loop Filter

The loop filter is designed in the CMOS dynamic logic which is shown in Fig. 3. It allows only the low frequencies and attenuate high frequencies by the loop low pass filter and thus noise is removed. The phases between the PLL output signal voltage and the input reference signal voltage are continuously compared. The phase difference between them is proportional to the loop filter output signal. It offers an enable signal to the oscillator. To select a particular band of frequency, frequency selective circuits are used whereas the overall noise in phase will be suppressed by VCO control line input.

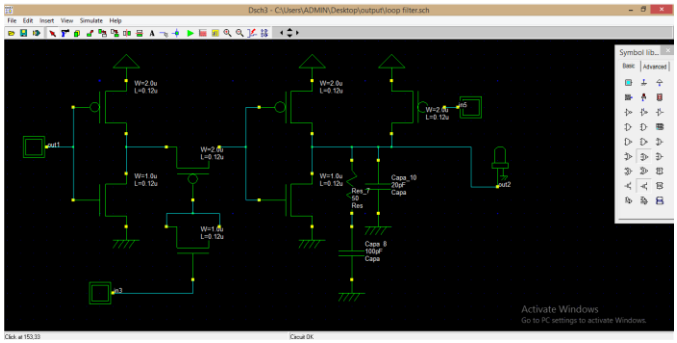

Fig. 3. DSCH3 layout of loop filter

C. CMOS Dynamic Logic Voltage Controlled Oscillator

Voltage-Controlled Oscillator (VCO) is designed in the CMOS dynamic logic as shown in Fig. 4. A Voltage Controlled Oscillator (VCO) is an electronic circuit whose oscillation frequency is controlled by an input signal voltage. The applied input voltage determines the instantaneous oscillation frequency. It is very challenging to design VCO which has high frequency deviation, adequate VCO sensitivity, good phase stability and capablility of accommodating wide band modulating signal.

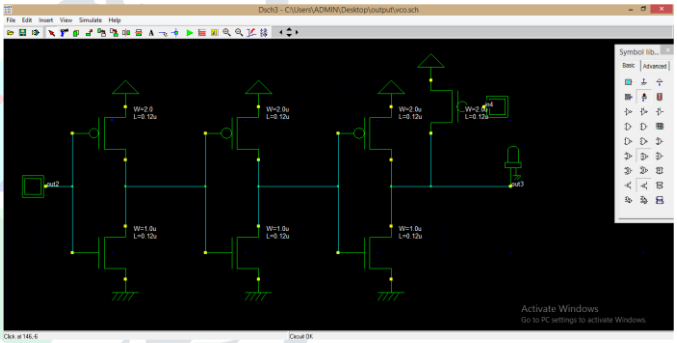

Fig. 4. DSCH3 layout of Voltage Controlled Oscillator

IV. PROPOSED MODEL

In order to achieve Low power, High Speed and Less Area, the number of transistors have to be reduced. The three blocks described above are combined to form a PLL frequency synthesizer in DSCH3 Tool. The output of Phase detector is fed to Low pass filter to allow only the low frequencies and in turn fed to Voltage controlled oscillator to obtain a range of Frequencies which acts a Frequency Synthesizer. Then the output of VCO is fed back to the Phase detector. Thus the range of frequencies is generated from single clock frequencies.

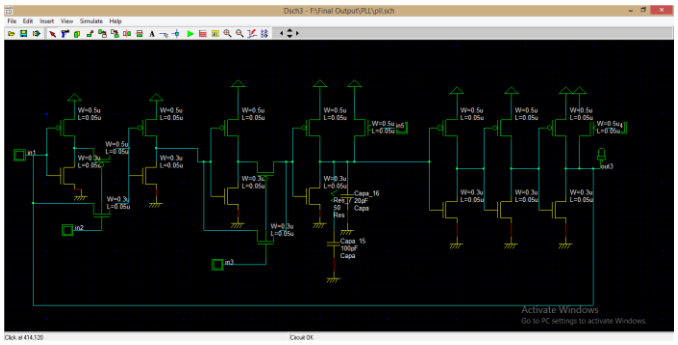

Fig 5. DSCH3 Layout of Phase Locked Loop

V. SIMULATION RESULTS

The design layout is obtained and simulated in Microwind 2 Tool using 90nm Technology. The Area, Speed, Time delay and Power consumption is analysed in this tool.

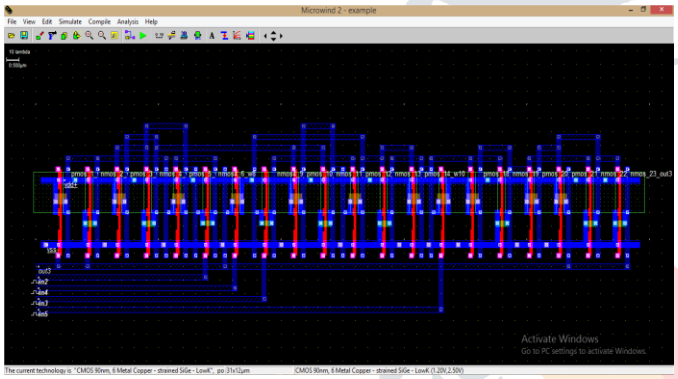

Fig. 6. Layout design of PLL in Microwind 2 Tool

The area of the layout is measured as 31x12 μm in 90nm CMOS technology as seen in Figure 6. The other parameters mentioned above are analysed and the generation of different frequencies are observed through the simulated graph below.

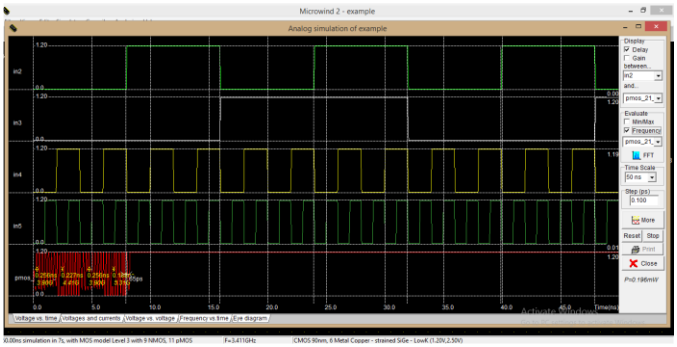

Fig.7. Simulation Results of Speed, Power, Time delay in Microwind 2 Tool

TABLE I. OBTAINED RESULTS OF PARAMETRIC ANALYSIS

S.No.	Parameters	Obtained results in 90nm technology
1	Speed	5.31GHz
2	Area	31x12um
3	Time delay	65ps
4	Power consumption	0.196mW

VI. CONCLUSION

The dynamic CMOS PLL operates at very high speed which is improved up to 90% with less power consumption of 0.196mW. In the design the number of transistors is reduced thus area is also reduced to 31x12 um. The time delay obtained is 65ps. This PLL generates a range of frequencies from 3.90 GHz to 5.31 GHz. It can be implemented in communication application such as frequency synthesis for missile tracking and also in FM transmitter.

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