Different Low Power Full Adder Using CNTFET

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Abstract: Due to large use of portable devices in the market battery operated low power devices are come in picture. Arithmetic unit is the main component of any embedded and digital signal processor devices. Therefore, implementation of full adder with low power consumption is required as it is a heart of arithmetic structures. This high performance adder reduces entire power of the system. Due to number of restriction occurs in CMOS technology, Carbon nanotube field-effect transistor(CNFET)is found an suitable solution to construct low-power devices by using different techniques. It reduces number of blocks required in generation of full adder. The different design of full adder are less complex and number transistors requires are less ,so automatically power consumption and delay is less. In this paper, different types of full adder circuits are studied.
IndexTerms: CNFET,Full adder,MOSFET.

1. INTRODUCTION

Nanometer technologies become more popular because chip density and the operating frequency has increased and to make portable devices which are operated on battery should consume less power. CMOS technology has become popular in electronic designers due to its low power consumption and it is cheaper because it requires low area on chip. Now the original limits of CMOS have been reached.

The consumption in static power increases as the leakage current increases in the short channel device. So at the device level leakage current is handled effectively rather than the circuit level. So the alternatives are like CNT FET, Tunnel FET, MUG FET etc. latest generation of CMOS technology are introduced with higher performance of the circuit and low cost per function. Now a day's scaling of planar devices of CMOS is up to 22nm in deep submicron. Continuously scaling in transistor will not possible because of materials used and limitations in processing technology. Scaling can be done by following methods

1) Scaling the supply voltage
2) Reducing operating frequency
3) Smaller silicon area. But due to this the propagation delay increases and the driving capability of the system can be degrade.

Full adder is the important elements of any circuit of any DSP related processors and it will effect more on the performance of that device. The overall performance of any system can be improved by increasing the performance of the full adder .

2. RELATED WORK

2.1 Hybrid full adder

Pankaj Kumar , Rajender Kumar Sharma[1] proposed the hybrid full adder. In full adders sum and carry blocks are very crucial.So full adder design gives better performance if the design of sum and carry blocks proper with low power consumption. In this system the outputs of the sum and carry blocks are depend on the input signal C. The pass transistor logic which uses Swing Restored Complementary is used in the circuit. The input signal C and the complement of it C' are used to drive the multiplexers instead of the inter-mediate signals. In this structure XOR or XNOR gates, NAND gate, modified NOR and multiplexers are used. To select the outputs of the sum and carry block multiplexers are inserted at the output. Internally no any signal is generated and due to that there is no generation of the delay and so it will provide full output voltage swings.

Three CMOS inverter are used to get the complement of any input signals. Multiplexers are designed using the transmission gate. NAND and modified NOR gates requires only three transistors. So this system become compact, faster and requires less power. In this system power consumption and propagation delay is less so power delay product increases. Also this proposed system gives good result under variations in temperatures and supply voltage. This proposed full adder is compared with the existing full adders with different parameters like propagation delay, power consumption and most important Power Delay Product (PDP) by using different technologies like UMC 90-nm and UMC 55-nm with no load conditions and buffers are inserted at input and outputs and additional capacitance are inserted at the output.[1]

2.210T full adder

Vishesh Dokania [2]proposed the 10T full adder. It is mainly focus on ultra low power consumption with appropriate output voltage levels. It first investigates the minimum energy points for FO4 inverter circuit which is helpful for designing ultra low power circuitary.MEP inFO4 inverter circuit is at VDD=0.15V.

The proposed 1-bit full adder uses two blocks, 1)sum block 2) the carry block. It uses one multiplexer and two XOR gates. To implement the sum block two XOR gates are used. By using four MOSFETs the output of first XOR is used as a input of the second XOR gate and input C. This XOR gate generates output of the Sum block (SUM). For a selector circuitry carry block uses 2 MOSFETs. For the selection line of the carry block the output of the 1st XOR gate is used . Less no of transistors are used in this design so by proper sizing of the transistor ultralow power consumption design can be obtained. The performance of this circuit is measured under noise immunity set up by injecting noise to one of the input of the circuit and Monte Carlo setup for robustness of the circuit in variations. It gives less average power consumption, shorter propagation delay, lower leakage power and has higher noise immunity. This proposed 10T full adder is preferred in portable devices and wearable devices where low power consumption is major requirement and performance is lower requirement as it consumes minimum energy.[2]

2.2 Multi-digit ternary ripple-carry adders

Chetan Vudadha[3] proposed multi-digit ternary ripple-carry adders using carbon field effect transistor technology(CNFET).In this half carry and half sum is generated using half adders. Output of the half adders are used to calculate carry out at each digit-adder stage . Low power encoders and sum generator are used to calculate final sum at each digit adder satge.Encoder converts intermediate binary signal to ternary output. It generates logic 0 and logic2 by making direct connection to GND and VDD.Carry are generated delay optimization technique. Using optimization in the carry propagation path delay has been reduced. Previous multi digit adders are implemented using HSPICE. By using this techniques power consumption is reduced up to 52% also there is reduction in power delay product up to 58%.In this system noise immunity is better.[3]

2.4 Adiabatic full adder

Mohammad Reza[4] Taheri proposed adiabatic full adder cells using CNFET technology. They mainly focus on improving leakage power using quasi-adiabatic circuits which is based on energy recovery approach. CNFET is similar to the silicon MOSFET with high current density and carrier mobility, less parasitic capacitance, switching energy per transition and operating voltages. Two types of adiabatic circuits are available fully adiabatic and quasi adiabatic .The proposed method uses quasi adiabatic structure as it is less complex, more popular feasible. They introduce 2N-2P buffer logic for the adiabatic circuit. In this two cross coupled pFET and two nFETs are used. The energy is recovered by wait, evaluate, hold and recovery phases. Full adder is constructed using various gates from that some are cascaded. Some of the transistors are uses between number of paths to reduce the no. of transistors, ultimately it reduces the area on silicon die. Adiabatic full adder introduced saves power when operated on low frequency. An increase in operating frequency power saving reduces so it is suitable up to 1 GHZ operating frequency. Adiabatic full adder consumes less power and it is robust for various process variations.[4]

2.5 A Low-Voltage Full Adder

Keivan Navi [5] proposes the The full adder circuit using two half adders that are made up of XOR gate, OR gate and AND gate.In this type as the CNTFET works on voltage of 0.3V so the threshold voltage of the device is 0.27 v approximately. As the device is operating at 0.3 v therefore the automatically power consumption is very less and there is no effect on the current. And also it will not affect on the fan out of circuit.[5]

2.6 Ternary full adder

F. Jafarzadehpour, P. Keshavarzian [6] proposed ternary full adder using carbon field effect transistor technology(CNFET).It uses the simple control of threshold voltage to construct the full adder called as ternary adder. In this circuit power consumption is less ,complexity is less also power delay product is less. Here proper noise margin is maintained. Multiple valued logic (MVL) has become more popular due to its less area required on chip so ultimately it reduces the area and it increases the performance speed in arithmetic operations. So to reduce the no of interconnections multi valued logic is used multi valued logic is capable to carry large no of information as compared to the binary logic. Interconnections plays important role in circuit design of 2 valued circuits because they required more area on chip that is up to 70 %. To extract the different in formations from the i/ps different design of decoders are used. Then this data is used for the generation of sum and carry. So the performance of the decoded data is improved by interchanging the binary circuits with the ternary AND and OR gates .So ultimately there is reduction in power consumption because it requires less area so the system performance and speed increases. In this type of adder, binary Nor gate is taken place by ternary NOR ,here assumption is made that NOR gates uses binary i/ps. and complements of this gates can be calculated by using inverters In this type of design the carry and sum generation blocks are different. Due to this type of design no. of gates required are more. In this design ,threshold voltages of different values are achieved by different CNTFETs with different chirality vector. [6]

2.7High performance full adder

Mohammad Hussein Moaiyeri proposed a full adder circuit which gives high performance as well as high speed made by CNFET used for low voltage application. The Sum and Cout blocks of this adder are symmetric uses same hardware configuration to produce the parallel Sum and Cout signals . To implement the sum function a 3-input XOR circuit of 10 CNFETs is used which does not uses complementary inputs.As complentary inputs are not used to s to complement the original inputs ,inverters are required which automatically reduces the power consumption and delay. By using CNFET nanotechnology, the problem of intrinsic threshold voltage drop can be resolved. The second circuit which generates the Cout signal is based on a direct implementation. It is similar to the Sum but in its critical path it uses only two CNT pass-transistors and it has no complementary inputs. In this type critical paths are short and it consist only two CNFETs. By implementing this type of adder it generates very low propagation delay and sensitive to process variations which leads this design more suitable for low voltage application [7]

Conclusion

Seven different Full Adder Circuits are compared by their parameters. These different techniques are explained in Section 2 . The main parameters discussed in this paper were power consumption and less propagation delay. So such types of full adders are more suitable for low power applications, low propagation delays, portable devices as well as sensitive to process variations.

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