Digital audio filter using VHDL

1. Prof. Akbar Ali , 2.Tejaswini Meshram,3.Triveni Chapekar , 4.Shubham Rokade ,5.Deepali Ramteke

PROFESSOR, DEPARTMENT OF ELECTRONIC AND TELECOMMUNICATION, ANJUMAN COLLEGE OF ENGINEERING AND TECHNOLOGY, NAGPUR

[1]STUDENT, WE DEPARMENT OF ELECTRONIC AND TELECOMMUNICATION, ANJUMAN COLLEGE OF ENGINEERING AND TECHNOLOGY, NAGPUR

[2]STUDENT, WE DEPARMENT OF ELECTRONIC AND TELECOMMUNICATION, ANJUMAN COLLEGE OF ENGINEERING AND TECHNOLOGY, NAGPUR

[3]STUDENT, WE DEPARMENT OF ELECTRONIC AND TELECOMMUNICATION, ANJUMAN COLLEGE OF ENGINEERING AND TECHNOLOGY, NAGPUR

[4]STUDENT, WE DEPARMENT OF ELECTRONIC AND TELECOMMUNICATION, ANJUMAN COLLEGE OF ENGINEERING AND TECHNOLOGY, NAGPUR

ABSTRACT

Nowadays digital filters square measure substitution analog filters that square measure wont to take away the unwanted part from the signal and increase the S/N magnitude relation. at first digital filters were enforced on PDSP and ASIC.

But currently thanks to the lower prize and customized style prospects, FPGA primarily based system is a lot of common than the PDSP and ASIC. What is most of the FPGA are often reprogram thus the kind of filter enforced are often modified as per the need by programming completely different filter coefficients. Filters play vital role in digital signal process its applications square measure Video process, image process and conjointly in wireless communication.

Low pass digital finite impulse response (FIR) filter is intended and enforced by victimization eight coefficients and tap sin the look. The entire system square measure coded in VHDL language .We show the Implementation of Audio process by victimization VHDL. The reconciling channel is connected to the signal for noise cancellation. Therefore reduces delay of the signal and improve the character of the signal.

The major application range will be with in the computerised correspondences by interfacing a number of totally different laden utilizing intrinsically inputs and outputs, every with varied info channels that may speak with each other increasingly over a speedy correspondence be part of. The basic issue of this paper is that the execution of the filtered signal victimization accommodative filter .These method includes the functions of ADC and DAC.

INTRODUCTION

The basic issue of this paper is the execution of the filtered signal using adaptive filter. The DSP processors and application-specific integrated circuits (ASICs) area unit the everyday electronic circuits which supply a compact size, high packing density, low cost, low power and low power demand.

However, due to lack of flexibility and their performance for variable structures, it's not economical for reconfigurable and convertible signal process. The utilization of high-speed analog to digital converters and digital to analog converters with field-programmable gate arrays has been a prospering replacement that is employed to beat the restrictions associated with DSP processors and application specific microcircuit.

The use of FPGAs for DSP applications has specific benefits over Digital signal Processor or victimization ASICs to implement varied signal process applications with higher speed, flexibility and accuracy. FPGA consists of the many fastened options like DSP blocks, embedded processors, and memory blocks. Therefore, it provides the manufacturers to customize their style for good implementation. MATLAB is an powerful tool to develop a different kind of signal processing algorithm in an efficient way. It is a fourth generation programming language .It provides a high-speed link between personal computers and FPGAs.

Apart from MATLAB-FPGA communication using the developed algorithm, it also contributes to FPGA designing and it also provides the facility to compare and verify the accuracy of an algorithm using two different implementations i.e. using VHDL and MATLAB. It is also applicable for loading parameters and on-chip verifications by inputting a variety of signals.

Advantage of FPGA is that it is an efficient Integrated Design Environment (IDE) supporting VHDL or Verilog design flows and manages the designs through simulation to synthesis. It provides the facility to design at RTL level featuring design entry, synthesis, verification and implementation sub-flows. It facilitates the integration of I/O with the product design as well as the bi-directional integration of the PCB design flow.

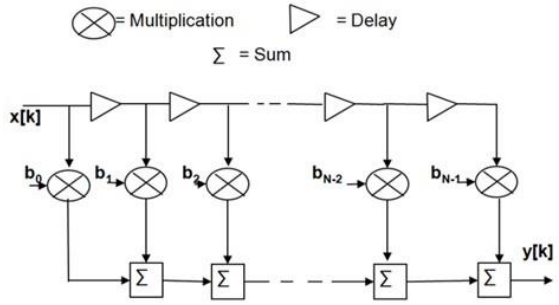
FPGA Advantage enables design simulation, creation with debugging and analysis, management, synthesis and documentation as a smooth operation from one step to the next.

2. DIGITAL FILTER BASICS

Digital Filters are mainly classified into two types: Infinite Impulse Response or Recursive Filters ii. Finite Impulse Response or Non recursive Filters. Finite Impulse Response (FIR) Filters are those whose output depends on past and present input only.

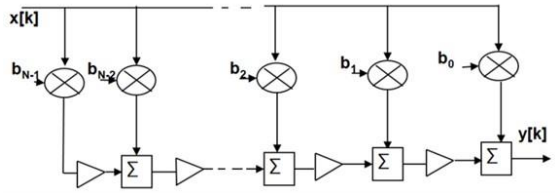
They don’t contain feedback from output. The basic mathematical equation governing the output of such filter .Some of the other form includes Cascade and Lattice structure realizations. The order of a filter depends on the number of delay lines present in the architecture 0f filter. And b[0],b[1]… b[N] are called the Filter coefficients.

Some other types of the FIR filters include Windowed Sink, Moving average etc. Output of Recursive or IIR Filters {y[n]=b(0)*x[n]+b(1)*x[n-1]+…….b(N)*x[n-N](1) }Where h[n] is the impulse response of filter usually called the filter coefficients in case of FIR filters. It can be seen from the filtering architecture that the basic operation consists of multiplication and addition which are the two most important mathematical operations and as well performed with the assistance of Multiply & Accumulate units (MAC) TYPE OF FILTER: CRITERION FOR choice one. FIR: Stable response, linear part two. IIR: Faster process, economical. A) Butterworth: Flat response, Higher transition breadth, higher order B) Chebyshev: Exhibit ripples, faster rattle down, lower order.



Deriving Filter Coefficients & Checking response victimisation Mathematical package a method of finding the h(n) is to derive them from the 'Z' domain transfer perform. The Z-transform is extremely helpful role within the analysis and characterization of the linear time-invariant systems. This is often as a result of the distinction equations characterizing the distinct system as reworked into pure mathematics equations, that as a lot of easier to control.

The two sided Z-transform of discrete-time function f(nT) is given



as, y[n]=b(0)*x[n]+b(1)*x[n-1]+…….b(N)*x[n-N](1)

$$F(Z)=\sum_{n=-\infty}^{\infty} f(nT)z^{-n}$$

Where h[n] is the impulse response of the filter popularly called the filter coefficients in case of FIR filters. It can be seen from the basic filtering architecture that the basic operation consists of multiplication and addition which are the two major mathematical operations and are well performed by the Multiply & Accumulate units (MAC)

TYPE OF FILTER		CRITERION FOR SELECTION
1	FIR	Stable response, Linear phase
2	IIR	Fasterprocessing, economical.
A	Butterworth	Flat response, Higher transition width, higher order
B	Chebyshev	Exhibit ripples , faster roll off , lower order.

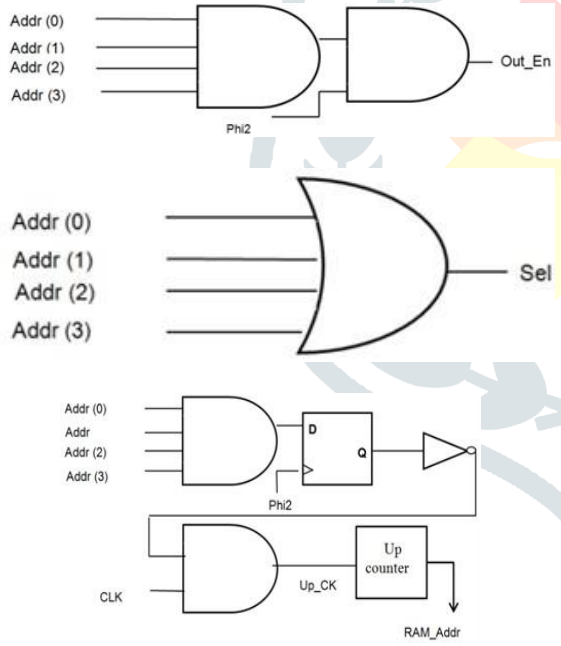
Deriving Filter Coefficients& Checking response victimisation Mathematical package a method of finding the filter coefficients is to derive them from the 'Z' domain transfer perform. The overall equation is as :a0 + a1 z-1 + a2 z-2+……..+an w-n H(z) = 1 + b1 z-1 + b2 z-2 + …… + bn z-n .

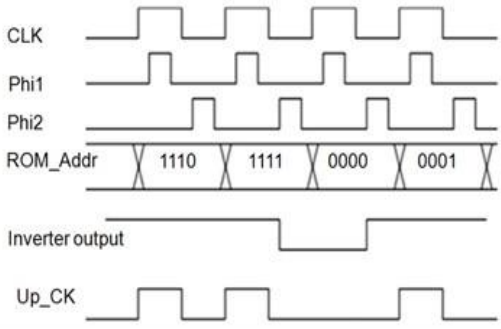
3. Controller design

The processor needed to be driven in a logical method, and due to the simplicity of the operation of the filter, few logic gates were able to deliver the required operations instead of using Finite State Machine (FSM). The intermediate signals which required for the operation are shown in Fig. 4.

The output change signal was obtained from the read only memory Address bits that is that the output of 4-bit up-counter as shown in Fig.4 (a). victimisation 2 AND gates would make sure that it'll solely enabled once read-only memory address reaches to "0000" (for 4-bits address length) providing that clock signal. To confirm that the electronic device uses the correct price, Associate in Nursing logic gate was wont to management the choose line as shown in Fig. 4(b).

The address generator for RAM address is shown in Fig.4(c). Once the ROM's price reached to "0000", the output from the primary logic gate turned to '0' and hold on within the flip-flop awaiting phi2 to be declared high for cathartic the hold on price. The hold on price passes through the electrical converter and adjusted into '1'. Having '1' input to the second logic gate disabled the up-counter.
An illustration of the continuance system used is shown in Fig. 5. It conjointly shows that the Up_ CK that is being suppressed so as to implement the 99-bonk continuance.
Fig. four management signals: a) output change signal to change output latch, b) choose signal for electronic device, c) address





4. Results and verification

The Verifications of results were required to see the model developed model match with the set specifications.

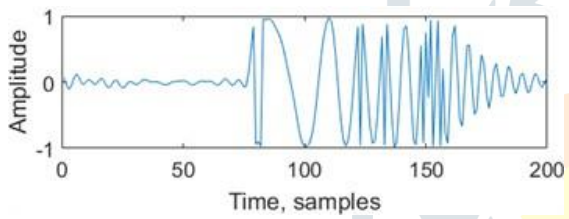
The results has got to be compared with the MATLAB results. An equivalent specifications of the filter and the input stimulus were used to analyze the filtered output in MATLAB. The results obtained in MATLAB . It's ascertained from that the results obtained in ModelSim and MATLAB area unit absolutely matched.

In order to demonstrate additional, a 16-tap low-pass filter design, the frequency of twenty four kilocycle, pass-band at four.8 kilocycle and stop-band at half-dozen kHz and the graphical user interface was developed in MATLAB to get the filter coefficients as per specifications. The impulse perform and step functions area unit applied to each systems.

The simulation result obtained from the processor-VHDL model was fully matched with the MATLAB results as shown in Fig. nine and offers guarantee that the system was enforced properly .The system are often tested for any order of FIR filter for low-pass, high-pass, band-pass or band-reject specifications.

Hence, this results in making a versatile and universal filter for signal process applications. It should be noted that each one elements of the design area unit describe because of the employment of generic in VHDL. This results in an equivalent design be applicable for the frequency ranges apart from oftenness.

.



Conclusions

The FIR filters area wide utilized in digital signal process and might be enforced victimization programmable digital processors. The design of the processor was apply in VHDL at register transfer level (RTL) and therefore the acquire results verified with MATLAB in according with the specifications of a filter. During this model was engineered employing a single number and accumulator that shows the economical style.

The control signals were generated using the simple combinational circuits prefer than complex state diagrams. The model is versatile and might be operated for numerous FIR filters with completely different specifications. The FIR filters square measure wide utilized in digital signal process and might be apply mistreatment programmable digital processors.

The use of one multiplier factor and versatile style will cut back the general price and adaptability is affected as a result of complicated computations. The model is employed for the period applications like, audio signal process. The design was developed mistreatment generic in VHDL that makes it frequency-independent because of parameterized parts and thus is used for inaudible frequencies also.

The relevance of FPGA within the field of inaudible signal process reviewed so, the implementation of FIR filters on FPGA is the requirement of the day as a resultof FPGAs will offer increased speed. {this is |this is often |this is} because of the actual fact that the hardware implementation of a great deal of multipliers can be done on FPGA that square measure restricted just in case of programmable digital processors.

Moreover, high mistreatment laptop performance, low cost, low power needs as compared to DSP processors. Keeping this motivation ,the given work is any extended to the versatile inaudible signal process and noise reduction with band cacophonous. In these field of inaudible signal process, FPGA are going to be a dominant platform and a lot of robust and effective architectures is developed in future.

In these field of ultrasonic signal processing, FPGA will be a dominant platform and more strong and effective architectures can be developed in future. The different architectures can be switched as per requirement.

REFERENCES

[1]Takalashi Y., Sekine T. and Yokoyama M. 70MHz Multiplier less FIR Hilbert Transformer in standard CMOS Library, IEICE ,2007.

[2]Choi, Seak C. and Lee H.A Partial Self-Reconfigurable Adaptive FIR Filter System, 2007.

[3] "Digital Signal Processing", Ramesh Babu, 4th edition.

[4]Mirzaei S., Hosangadi A. And Kastner R. FPGA Implementation of High Speed FIR Filters Using Add and Shift Method, , 2006

[5] "The Scientists & Engineers guide to Digital Signal processing", Steven .W .Smith.

[6]Prokis J. G, Manolakis D. G. Digital Signal Processing, 3rd Edition, PHI publication 2004.
[7] Takahashi Y. and Yokoyama M. New cost-effective VLSI implementation of multiplierless FIR filter using common subexpression elimination, Proc. IEEE Int. Symp. On Circuits and Systems (ISCAS 2005), pp.845-848, May 2005.

[8]Burrus C S, Digital Filters Structures described by Distributed Arithmetic, IEEE Transactions on Circuits and Systems, vol. CAS-24, page: 12, December 1977.

[9] E.C Tan. "Variable low pass wave-digital filters", Electronics letters, vol.18 No.8, pp.324-326.

[
10] S.S Ahuja &.S.C Dutta Roy. "Variable Digital Filters", IEEE trans. Circuits.