A LOW POWER COMPARATOR DESIGN FOR 8-BIT FLASH ADC IN 90-nm CMOS

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Abstract

The main focus of this paper is to design a "LOW POWER FLASH ADC" For ultra-wide and applications using CMOS 90-Nm Flash ADC consists of a reference generator, array of comparators, 1-out-of N code generator, fat tree encoder and output D-latches. The demanding issues in the design of a low power flash ADC is the design of low power latched comparator. The proposed comparator in this paper is designed using 90-nm technology at 0.8V DC voltage source using Cadence tool. The simulation results of a 8-bit ADC is shown for a sampling frequency up to 1.2GHz showing an average power dissipation of 7.67mW.

Keywords— Flash ADC, preamplifier based latch comparator, low power consumption.

I. INTRODUCTION

Analog to digital converters plays a prominent role to interact with the real world. Flash ADC is the fastest ADC in comparison with other ADC architecture. Flash ADC is the best choice in high speed low resolution application. It is the highly used in high data rate links, high speed instrumentation, radar, digital oscilloscopes and optical communication. Since flash ADC is operating in parallel conversion method, maximum operating frequency in the range of gigahertz is possible.

In this paper we are designing a low power, high speed comparator. Here we are combining two recently published research papers to achieve the low power and high speed ADC. In a low power flash ADC with 8-bit resolution uses inverter based comparator which consumes a less power of 300micro watt at a sampling rate of 50MS/s. in a speed flash ADC with 8-bit resolution uses differential clocked comparator architecture. Even though the sampling speed is 1GS/s, the comparator block alone consumes 2mW of power. The present work collaborates the above explained two papers in order to fill the gap by proposing a 8bit flash ADC for high speed applications and slightly higher power compared to the inverter based ADC. The proposed ADC and employs a modified version of the comparator block presented in to achieve low power and high speed of operation.

The main purpose of this paper is to increase speed of the flash ADC by utilizing less hardware. The proposed ADC architecture is described in section I. Flash ADC Design and Implementation is explained in Section II. Section III has embedded all the components to have our flash ADC with the results. The conclusion is drawn in section IV.

II. ADC ARCHITECTURE

A flash ADC consists of resistors, sample-hold, comparators, and encoder as shown in Fig 1. The reference voltage is divided into equally spaced values, each of which is fed to comparator. The input is compared with these $2^{N}-1$ different reference values to generate a thermometer code [1]. Flash ADC consists of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.

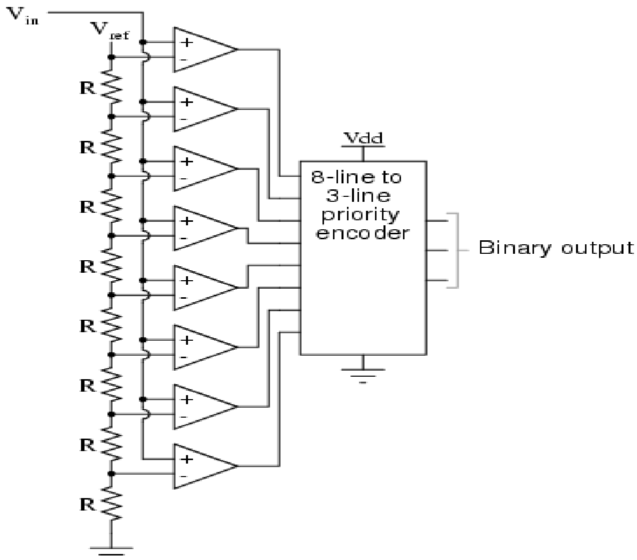

Figure 1. Proposed Flash ADC

V_{ref} is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit (not shown in the schematic). As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs. Flash ADCs are made by cascading high-speed comparators. Each comparator represents 1LSB, and the output code can be determined in one complete cycle. Conceptually, the flash architecture is quite straightforward: a set of $2^{n}-1$ comparators are used to directly measure an analog signal to a resolution of n bits. These values are spaced one least-significant bit ($LSB=FS/2^{n}$) apart. The comparator outputs simultaneously present $2^{n}-1$ discrete digital output states. Following the method described above, the authors have designed each part of the Flash ADC individually, tested each part and then embedded together to have an efficient Flash ADC. The design details and its implementations are presented in the next Section.

III. FLASH ADC DESIGN AND IMPLEMENTATION

The details of the different parts described above are designed in this section and the results obtained are also presented in this section

A. cmos comparator design

A high-performance comparator is considered here and is shown in Fig.2, which comprises of three stages such as the
input preamplifier, a positive feedback or decision stage, and an output buffer. The preamp stage amplifies the input signal to improve the comparator sensitivity and isolates the input of the comparator from switching noise coming from the positive feedback stage (this is important). A comparator
design begins with considering input common-mode range,
power dissipation, propagation delay, and comparator gain.

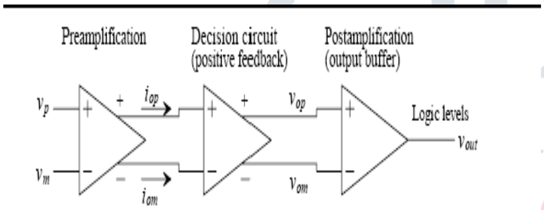

Figure 2. Block Diagram of a Voltage Comparator

IV. PREAMPLIFIER

The stage-1 of proposed comparator shown in figure2 working as a preamplifier. The preamplifier amplifies the difference between input voltage and the reference voltage generated by the resistive ladder of the ADC. The preamplifier is a circuit which is used to amplifies the signal so that it can easily drive the load. In most latched comparator design of preamplifier s are also used to avoid the kick back effect from the latch and input referred offset.

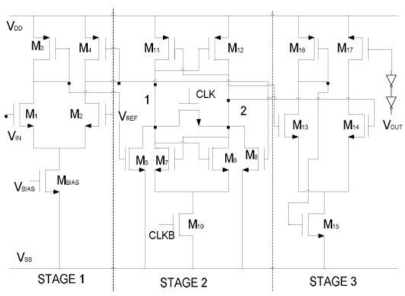

Fig. 2: Circuit diagram of Comparator

V. Latch

The stage-2 of proposed comparator shown in figure2 works as a latch. Basic function of the latch in any circuit is as a ememory element, which is used to store the value. Latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. The latch stage consists of a cross coupled pair of PMOS & NMOS transistors. The latch works iin two phases. 1- when the clock is CLOCK is LOW and the other is when the CLOCK is HIGH.

VI. Design of 8-bit flash ADC

In this section the proposed 90-nm CMOS technology based 8-bit flash analog to digital converter is described the 8-bit flash ADC consist of following block 1.comparator 2.one out of n-code generators and 3.ROM

System specification

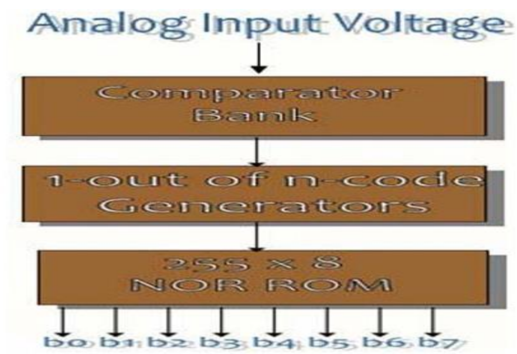

Figure 1. Block diagram of a 8-bit flash ADC

VII. Advantages

- Flash converters are extremely fast compared to many other types of ADC, which usually narrow in on the “correct” answer over series of stages
- Compared to these, a flash converter is also quite simple and, apart from the analog comparators, only requires logic for the final conversion to binary.
- Very fast.
- Can convert data even at high frequency

VIII. Disadvantages

- Needs many parts
- Lower resolution
- Expensive
- Low accuracy

IX. Application

- data acquisition
- satellite communication
- radar processing
-
- sampling oscilloscope
- high densidity diskdrives
- automative

X. Problem identification

For best accuracy, often a track-and-hold circuit is inserted in front of the ADC input. This is needed for many ADC types (like successive approximationADC), but for flash ADCs there is no real need for this, because the comparators are the sampling devices.

XI. Conclusion

In this paper, the design and the simulation results of 0.8V 1.2GS/s 8-bit low power flash ADC are represented
This scheme consumes a very less power which consumes a less power of about 50% of the previous referred approaches. This architecture can be extended to high speed applications because the comparator used in this ADC can work up to 5 GS/s. As the ADC has high input bandwidth, low power consumption and high linearity, this ADC is most suitable for high speed communication applications up to 1.2GS/s.

XII. References

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