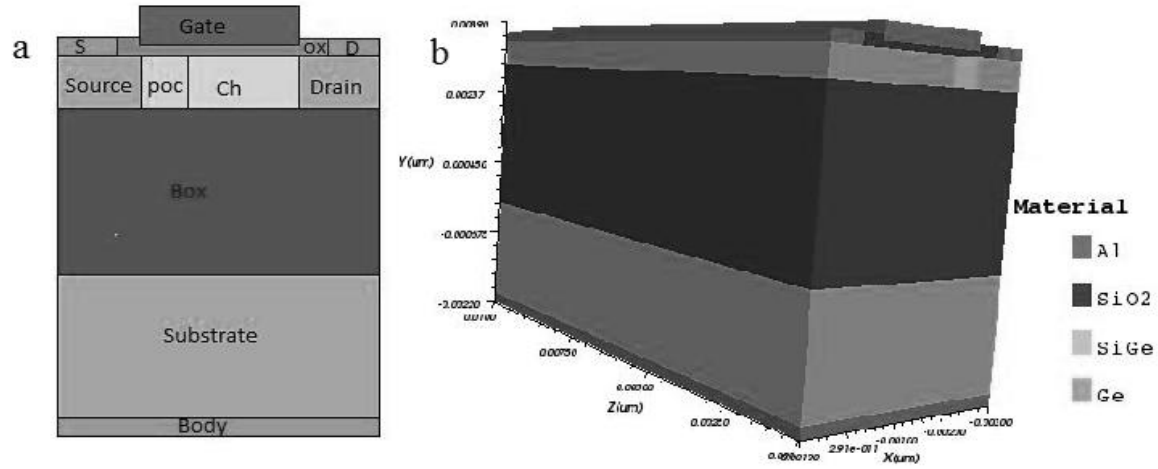

Figure 1(a) 2-D view of pocket $Si_{0.7}Ge_{0.3}$ JLTFET with Ge wafer; (b) 3-D view of pocket $Si_{0.7}Ge_{0.3}$ JLTFET with Ge wafer

Figure 1a & 1b shows 2D and 3D structure of pocket Ge-SiGe JLTFET indicating device region view and material region view. The design is implemented using TCAD simulator.

3. Results Analysis

The curve of Id versus Vgs for p+ pocket Si_xGe_{1-x} nJLTFET is drawn with different gate contact/oxide materials. A good value of I_{on}/I_{off} is observed in Figure 2(a) for Pt as gate material and HfO_2 as gate oxide in comparison to Al/SiO2 combination. The use of high-K dielectric material HfO_2 reduces hot-electron effect that further reduces overall leakage current. The p+ pocket $Si_{0.7}Ge_{0.3}$ region reduces static leakage current with good level of ON-state current showing a steep subthreshold slope. Low value of leakage current and steep subthreshold characteristics of proposed Ge-Si_xGe_{1-x} nJLTFET, overcome the scaling limits with smaller dimensions. Similar characteristics as shown in Figure 2(b) p+ pocket Si_xGe_{1-x} nJLTTFET is obtained in saturation region (Vds=1V). The proposed p+ pocket Si_xGe_{1-x} nJLTFET shows the ideal drain current (Id) versus source-drain voltage (Vds) characteristics with variations in Vgs in range of 0-1V as shown in Figure 3 (a) & (b).

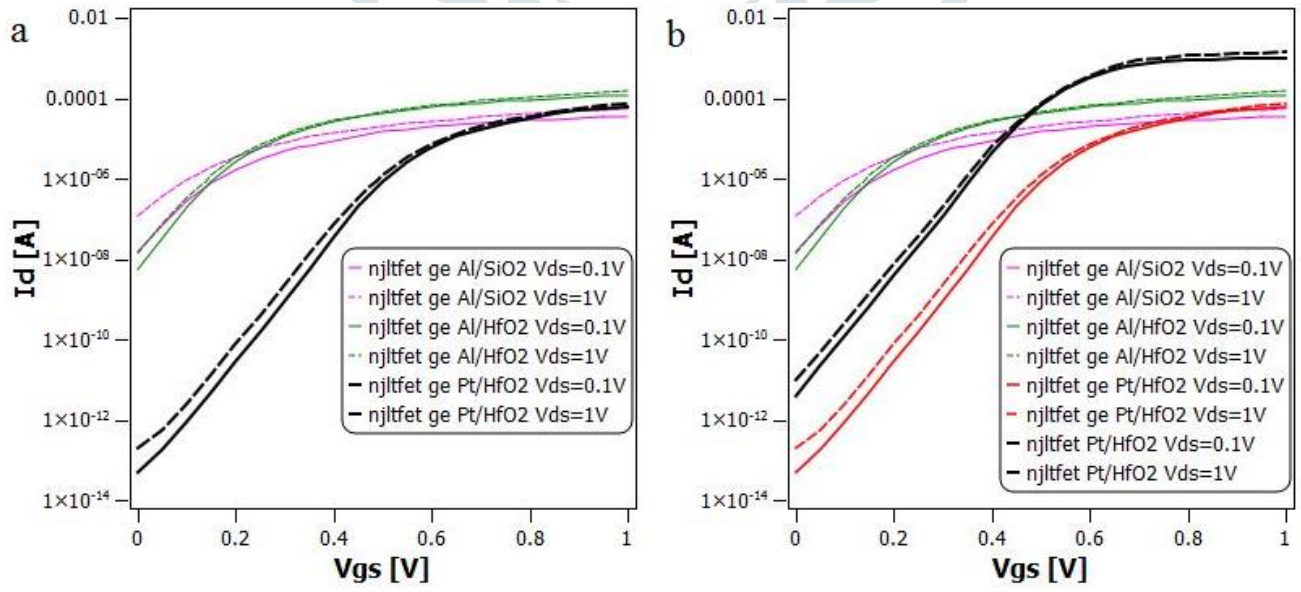

Figure3(a) Id vs Vgs of p+ pocket $Si_{0.7}Ge_{0.3}$ nJLTFET with different gate contact and oxide region; (b) Id vs Vgs p+ pocket $Si_{0.7}Ge_{0.3}$ nJLTFET with other TFET structures