CMOS 0.35 µm Low-Dropout Voltage Regulator using Differentiator Technique

[1]Shailika Sharma, [2]Himani Mittal,
[1,2]Electronics & Communication Department,
[1,2]JSS Academy of Technical Education,Gr. Noida, India

***Abstract*—This paper is a review paper to full on chip CMOS Low dropout voltage regulator. The 2.8-V LDO Voltage regulator (SoC) with a 200mV dropout in 0.35 µm CMOS technology with a load current of 50mA in the presence of 100 pF load on chip. A better transient analysis and fast turn on response is obtained. This architecture is composed by having a compensation scheme to provide better stability.**

***IndexTerms*— Linear voltage regulators, fast path, Analog integrated circuits, pole-zero compensation scheme, dominant pole, differentiator.**

I. INTRODUCTION

A Power management system requires low drop-out in circuit. Therefore a battery operated device requires low dropout voltage regulators to increase the power efficiency. They are similar to linear voltage regulators but with constant voltage at the output and better power efficiency. A power management system constitutes of control logic, linear regulators and switching regulators. Linear regulators depending upon the type of orientation of pass device different types of LDO can be made. Different types of regulators are there : conventional by using BJT or PMOS type, linear regulator with source follower , for improve version of source follower or Replica, with common source driver.

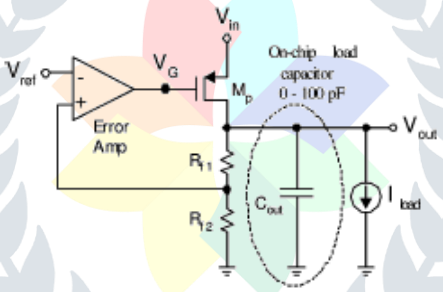


Fig 1 : Basic LDO voltage regulator.

One of the most challenging problems in designing LDO is the stability problems due to the closed loop and the parasitic components associated with the pass transistor and the error amplifier. In fact to compensate the loop stability a large external capacitor is often connected at the output.

Here for better stability without external capacitor a compensation technique is used. Pole-zero cancellation technique is used as compensation for better stability at low currents. To also decrease the board real estate, overall cost and make it SoC suitable. A 2.8-V LDO Voltage regulator with a 200mV dropout in 0.35 µm CMOS technology with a load current of 50mA is simulated in the presence of 100 pF load on chip .

II. DIFFERENT COMPENSATION TECHNIQUES FOR STABILITY PURPOSES

1. ***Internal zero generation using a differentiator***

An auxiliary fast loop (differentiator) provides both a fast transient detector path as well as internal ac compensation. The simplest coupling network might be a unity gain current buffer. C_f senses the changes in the output voltage in the form of a current that is then injected into pass transistor gate capacitance.

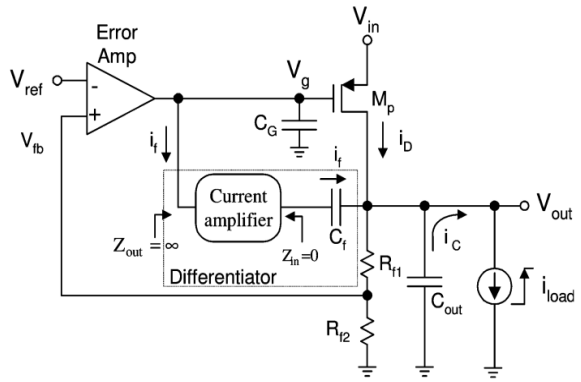


Fig 2 LDO topology with differentiator for fast transient path.

2. Capacitive feedback for frequency compensation

It introduces a left hand plane zero in the feedback loop to replace the zero generated by ESR of the output capacitor. The capacitor is split into two frequency-dependent voltage-controlled current sources (VCCS) and grounded capacitors.

Instead of adding a pole–zero pair with zero at lower frequency than the pole, in this technique only a zero is added. It needs a frequency dependent voltage control current source (VCCS).

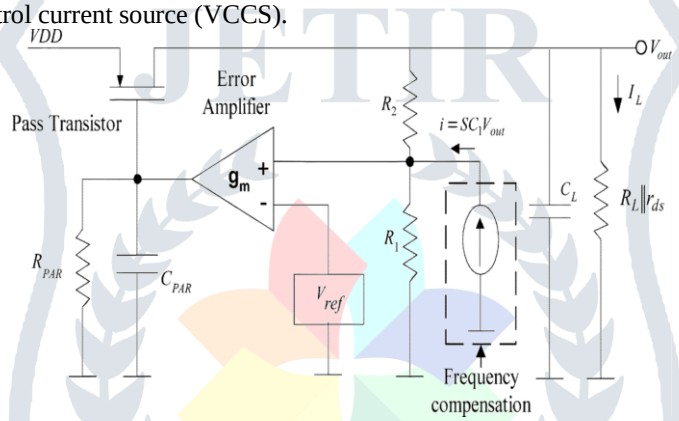


Fig 3: A frequency compensation scheme for LDO voltage regulators

3. DFC frequency compensation

It is a pole-splitting compensation technique especially designed for compensating amplifier with large-capacitive load. DFC block composed of a negative gain stage with a compensation capacitor Cm2, and it is connected at output of the first stage. Another compensation capacitor Cm1 is required to achieve pole-splitting effect. The feedback-resistive network creates a medium frequency zero for improving the LDO stability.

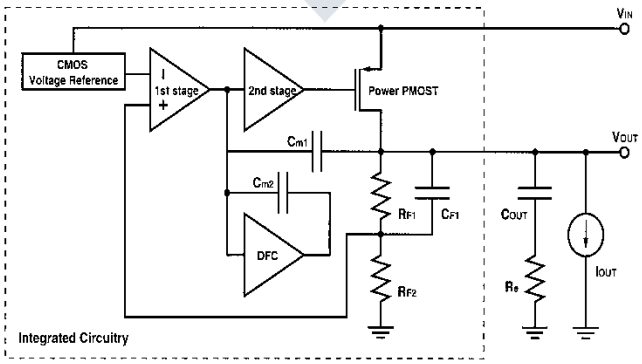


Fig 4: A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation

4. Pole-zero tracking frequency compensation

To have pole-zero cancellation, the position of the output pole po and compensation zero zc should match each other. The resistor is implemented using a transistor Mc in the linear region, where its value is controlled by the gate terminal.

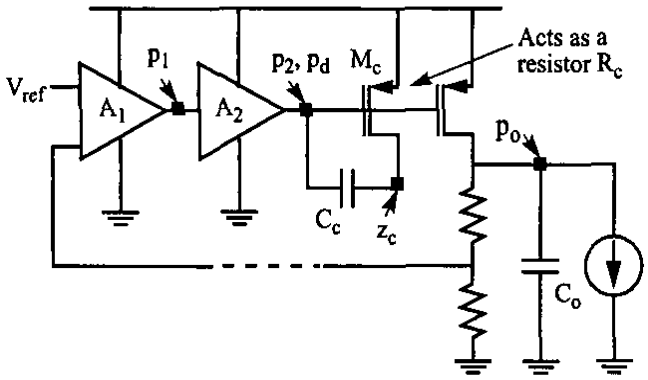


Fig 5: Pole-zero tracking frequency compensation for low dropout regulator.

III. LDO REGULATOR ARCHITECTURE

There are two major design considerations for this design of an external capacitorless LDO regulator: 1) small over/under shoots during transients and 2) the regulator's stability. As discussed above to solve these issues, a compensating left-hand plane (LHP) zero is introduced. The downside of that technique is the generation of an RHP zero . Some techniques reporting the elimination of that zero have been used for long time; a technique based on the approach reported in is used here for LDO's stabilization.

The transistor-level design is shown in Fig.5. A three-current mirror operational transconductance amplifier $M_0 - M_3$ and $M_E$forms the error amplifier. The low-impedance internal nodes of the three-current mirror operational transconductance amplifier (OTA) drive the parasitic poles out to high frequencies; well pass the desired GBW product. The error amplifier's parasitic poles do not significantly affect the performance of the regulator as long as they are at least three times greater than the loop's GBW product, and the error amplifier can, therefore, be designed to meet other desired parameters such as the output noise, power consumption, and dc gain.

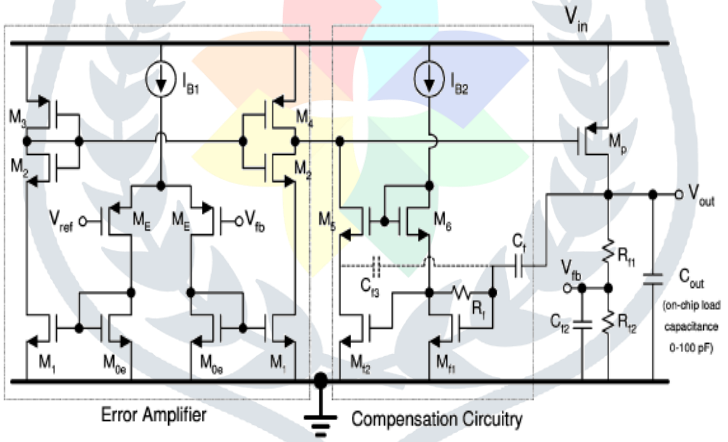


Fig 6 Transistor-level implementation of the proposed LDO's architecture

Transient Response Compensation

In the off-chip capacitorless LDO voltage regulator, the relatively small and load-dependent on-chip output capacitor cannot be used to create the dominant pole since the output pole must reside at high frequency. Thus, the dominant pole must be placed within the error amplifier control loop, and transient control signal must propagate through an internal dominant pole before or at the gate of the pass transistor. The pass transistor comprises the most important element supplies current to the load impedance and as a result develops the desired output voltage. Transistor gate capacitance and output resistance of error amplifier acts as a current to voltage converter, and thus, has an equivalent propagation delay. The larger the gate capacitance is, the larger the propagation delay will be. In the case of the pass transistor, the effective input gate capacitance is extremely large. Therefore, a circuit is needed that improves the speed of charging the gate of the pass transistor.

An auxiliary fast loop (differentiator), as shown in Fig.2 compensates LDO regulator. The differentiator forms the backbone of the architecture providing both a fast transient detector path as well as internal ac compensation. The simplest coupling network might be a unity gain current buffer senses the changes in the output voltage in the form of a current. The current is then injected into pass transistor gate capacitance by means of the coupling network. The compensating circuitry splits the poles, similarly to the regular Miller compensating scheme, and improves loop speed at the same time.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

It is implemented using BSIM-3 supporting 350 nm technology power supply of 3V with dropout of 200 mV. Transient analysis, AC analysis, line regulation, load regulation, turn on response, Percentage deviation of line regulation, load regulation. Results are here.

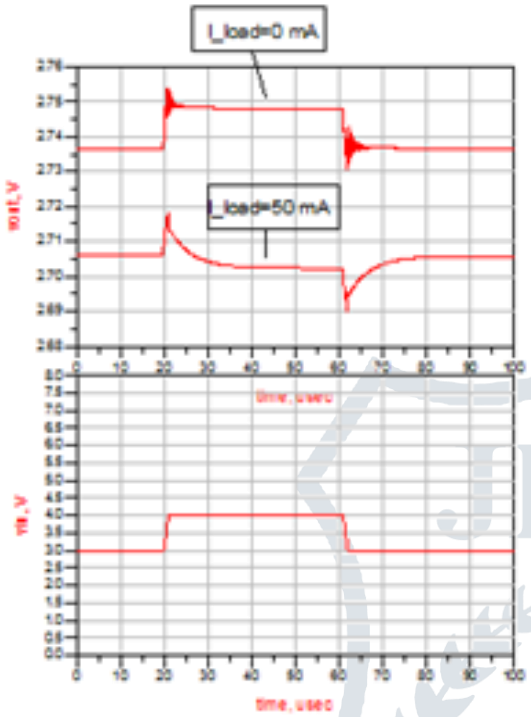
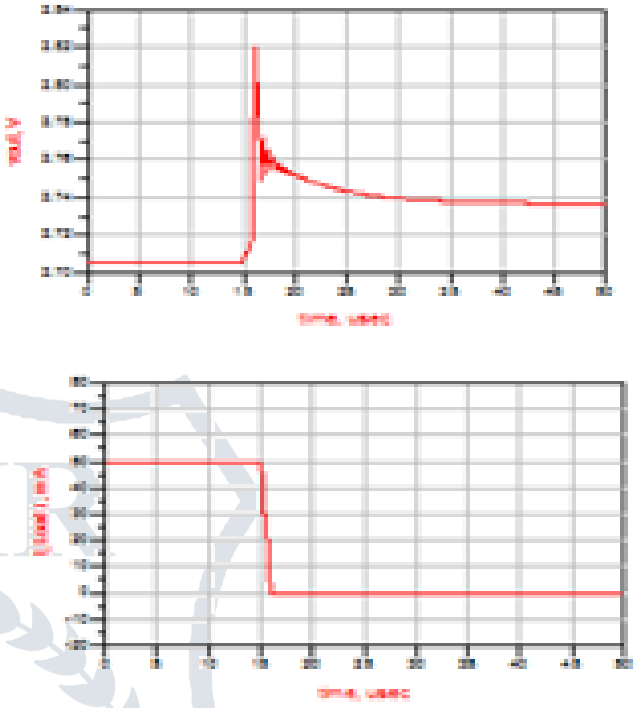
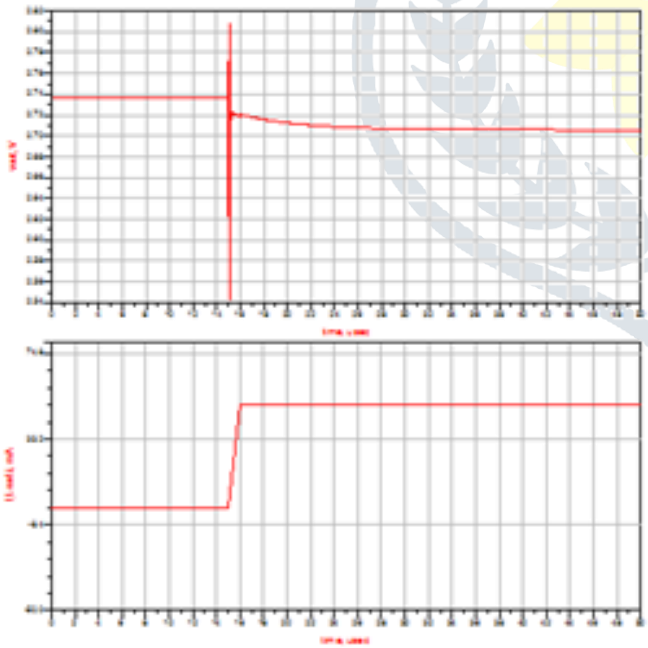


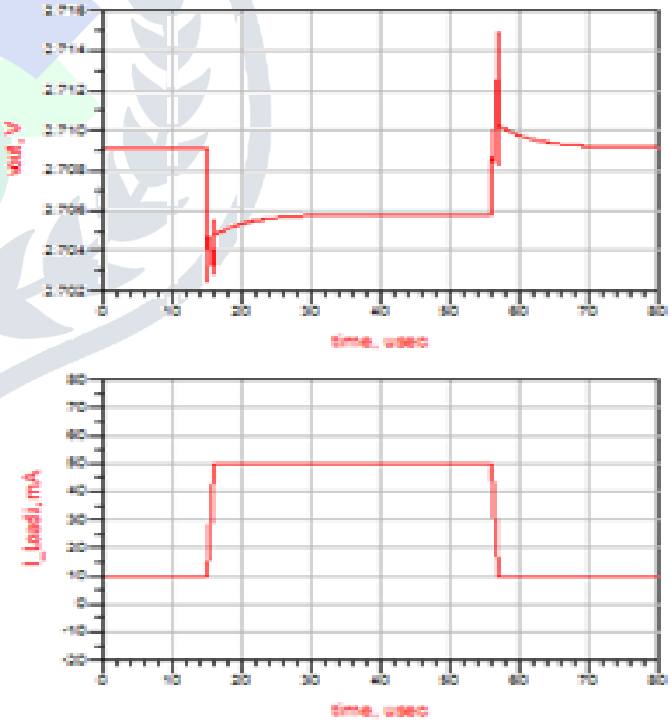
Fig 7: Measured Line transients



(b)

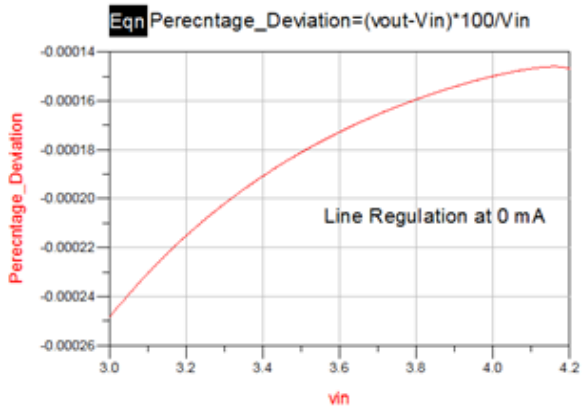


(a)

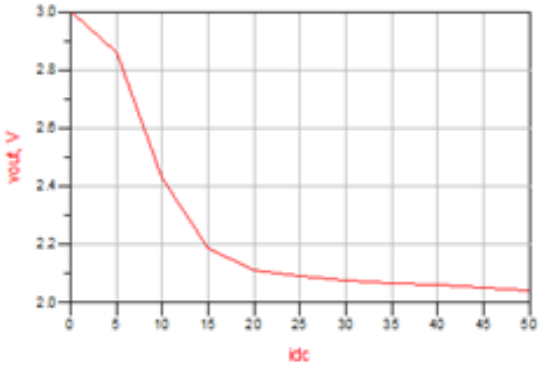


(c)

Fig. 8. Measured transient response: (a) 0–50 mA, (b) 50–0 mA, (c) 10–50 mA to 10 mA.

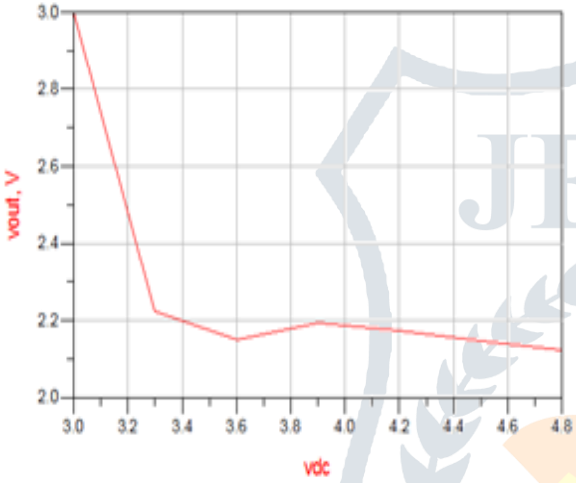


(a)



(c)

Fig 9: (a) Percentage deviation line regulation (b) Line regulation (c) Load regulation



(b)

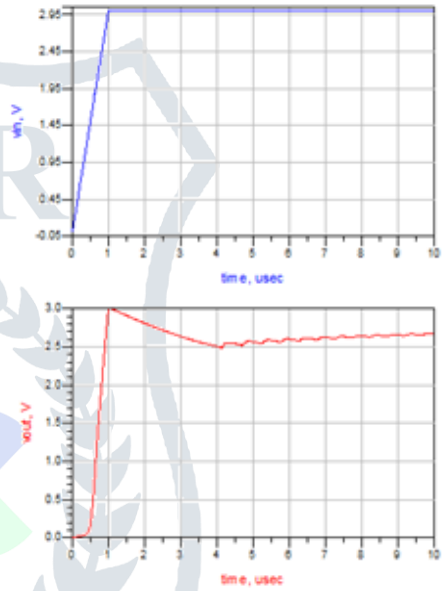


Fig 10: Turn on response

V. CONCLUSION

Experimental results show that the proposed LDO voltage regulator exceeds current work in the area of external capacitorless LDO regulators in both transient response and ac stability with 200 mV droput while the load capacitor can be as large as 100 pF. The proposed regulator consume low power, provides a low dropout voltage and fast settling time. SoC designs would benefit from the reduced board real estate, pin count, and cost achievable with the proposed off-chip capacitorless full CMOS LDO regulator.

REFERENCES

[1] Shailika Sharma, Himani Mittal, "Implementation of a Capacitor less Low Dropout Voltage Regulator on chip (soc)", IJTEL vol3 issue3, june 2014.

[2] G. Patounakis, Y. W. Li, and K. Shepard, "A fully integrated on-chip DC-DC conversion and power management system," IEEE J. Solid-State Circuits, vol. 39, no. 3, pp. 443–451, Mar. 2004.

[3] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency," IEEE J. Solid-State Circuits, vol. 37, no. 10, pp. 1691–1701, Oct. 2003.

[4] R. K. Dokaniz and G. A. Rincon-Mora, "Cancellation of load regulation in low drop-out regulators," Electron. Lett., vol. 38, no. 22, pp. 1300–1302, Oct. 24, 2002.

[5] V. Gupta, G. Rincon-Mora, and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in Proc. IEEE Int. Syst. Chip Conf. , Santa Clara, CA, Sep. 2004, pp. 311–315.

[6] C. K. Chava and J. Silva-Martinez, "A robust frequency compensation scheme for LDO voltage regulators," IEEE Trans. Circuits Syst. I, Reg.Papers, vol. 51, no. 6, pp. 1041–1050, Jun. 2004.

[7] P. R. Gray and R. G. Meyer, "MOS operational amplifier design—A tutorial overview," IEEE J. Solid-State Circuits, vol. SC-17, no. 6, pp. 969–982, Dec. 1982.

[8] B. K. Ahuja's, "An improved frequency compensation technique for CMOS operational amplifiers," IEEE J. Solid-State Circuits, vol. SC-18, no. 6, pp. 629–633, Dec. 1983.