Design & Simulation of Non-Volatile SRAM Using Magnetic Tunnel Junction

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***Abstract* – FPGA circuits have developed rapidly, because of their flexibility, their ease of use and the low cost to design a function with them. SRAM is volatile, both the configuration and information stored is lost. By working at high writing and reading speed, MRAM (Magnetic RAM) technology is one of the best solutions to bring complete non-volatility to the FPGA technology while keeping the power dissipation low. An MRAM can be re-programmed 10^{12} times and has a large retention time up to 10 years. The objective of our project is to contribute one such storage device by making Non-Volatile SRAM based on Magnetic Tunnel Junction (MTJ).**

***Keywords*—Magnetic Tunnel Junction (MTJ), Tunnel Magneto resistance (TMR), Non-volatile logic.**

I. INTRODUCTION

In recent years, the SRAM memory is volatile memory. Its store data during power is ON. When power is OFF, stored data is loss. The aim of this proposed model to change VOLATILE SRAM into NON-VOLATILE SRAM using MTJ (Magnetic Tunnel Junction). A nonvolatile storage device at present is the one using spin-transfer-torque (STT) magnetic tunnel junction (MTJ) devices. Most FPGA circuits use SRAM based flip-flop as internal memory. But since SRAM is volatile, both the configuration and information stored is lost. By working at high writing and reading speed, MRAM (Magnetic RAM) technology is one of the best solutions to bring complete non-volatility to the FPGA technology while keeping the power dissipation low.[1][2]

II. STATIC RANDOM ACCESS MEMORY

Static Random Access Memory is a type of semi-conductor memory, uses bi-stable latching circuitry to store each bit. SRAM inhibits data remanence but is still volatile in the conventional sense that data is eventually lost when the memory is not powered. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations.[2]

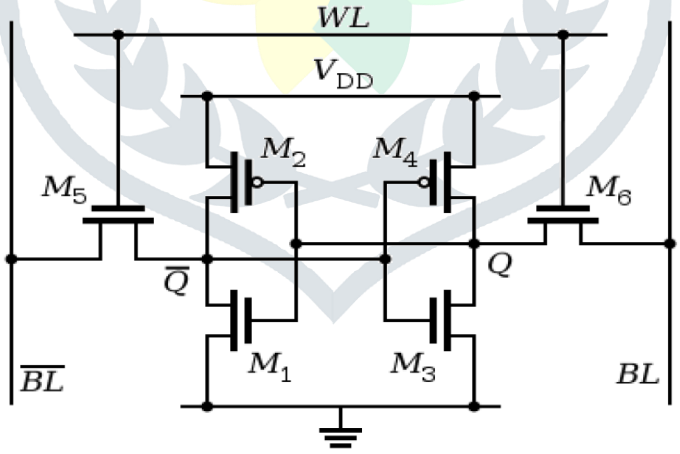

Figure 1: SRAM CELL

Access to the cell is enabled by the word line which controls the two access transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines. They are used to transfer data for both read and write operations. SRAM is used in personal computers, workstations, routers and peripheral equipment.

III. MAGNETIC TUNNEL JUNCTION

MTJ uses differentiate between the two logic states. It contains two Ferro-magnetic layers which are separated from each other by a thin layer of insulator also known as barrier.

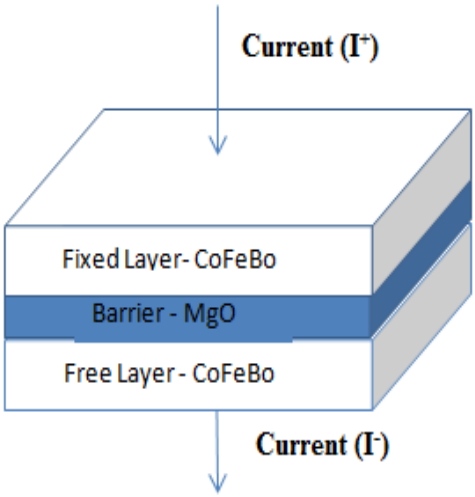

Figure 2: Magnetic Tunnel Junction

The ratio between the two resistances at zero bias is called as TMR ratio. Higher the TMR ratio, lower the resistance area.

$$TMR = (R^{AP} - R^{P}/R^{P}) \times 100\%$$

Where, R^{AP} is the electrical resistance in the anti-parallel state and R^{P} is the electrical resistance in the parallel state.

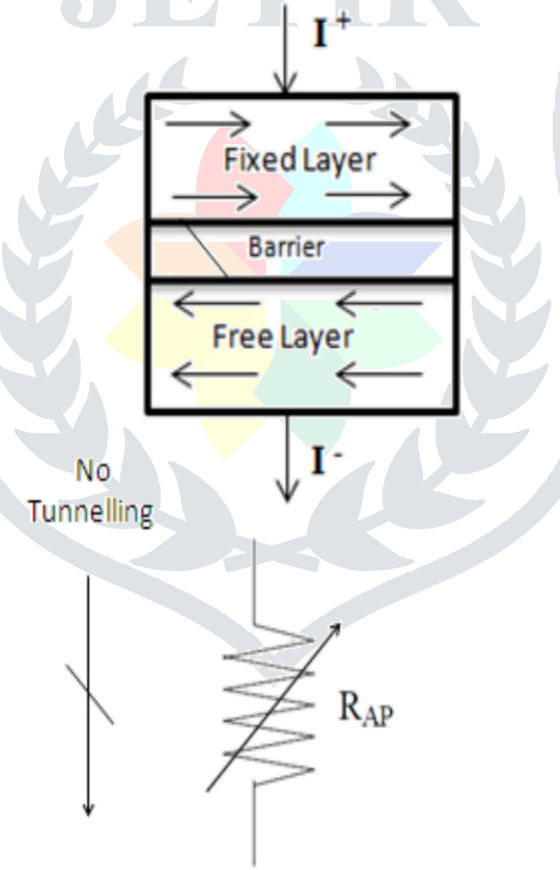

Figure 3: Anti-parallel field formed between the two layers.

Whereas when the fields formed between the two layers is parallel then low resistance is formed between the two layers and hence tunneling occurs.

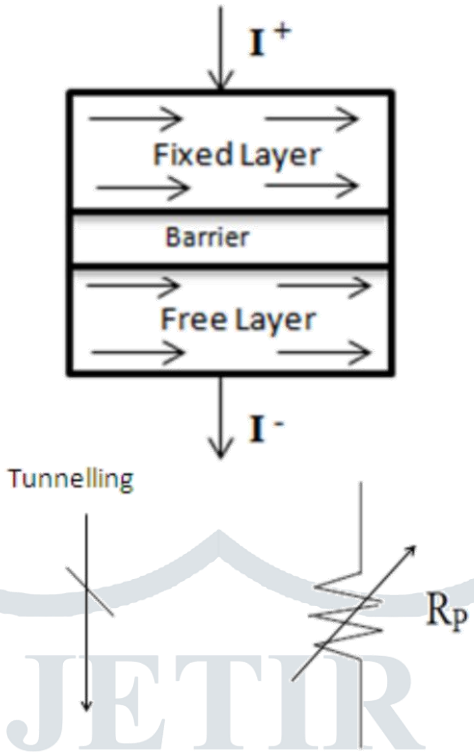

Figure 4: Parallel field formed between the two layers.

IV. Tool To Be Used For Stimulation

LT spice is a new SPICE that was developed to simulate analog circuits fast enough to make simulation of complex SMPS systems interactive. SPICE simulators are the only way to check circuitry prior to integration onto a chip. Analog circuit simulation has been inseparable from analog IC design. The SPICE simulation allows measurements of currents and voltages that are virtually impossible to do any other way.

V. Design Using LT Spice

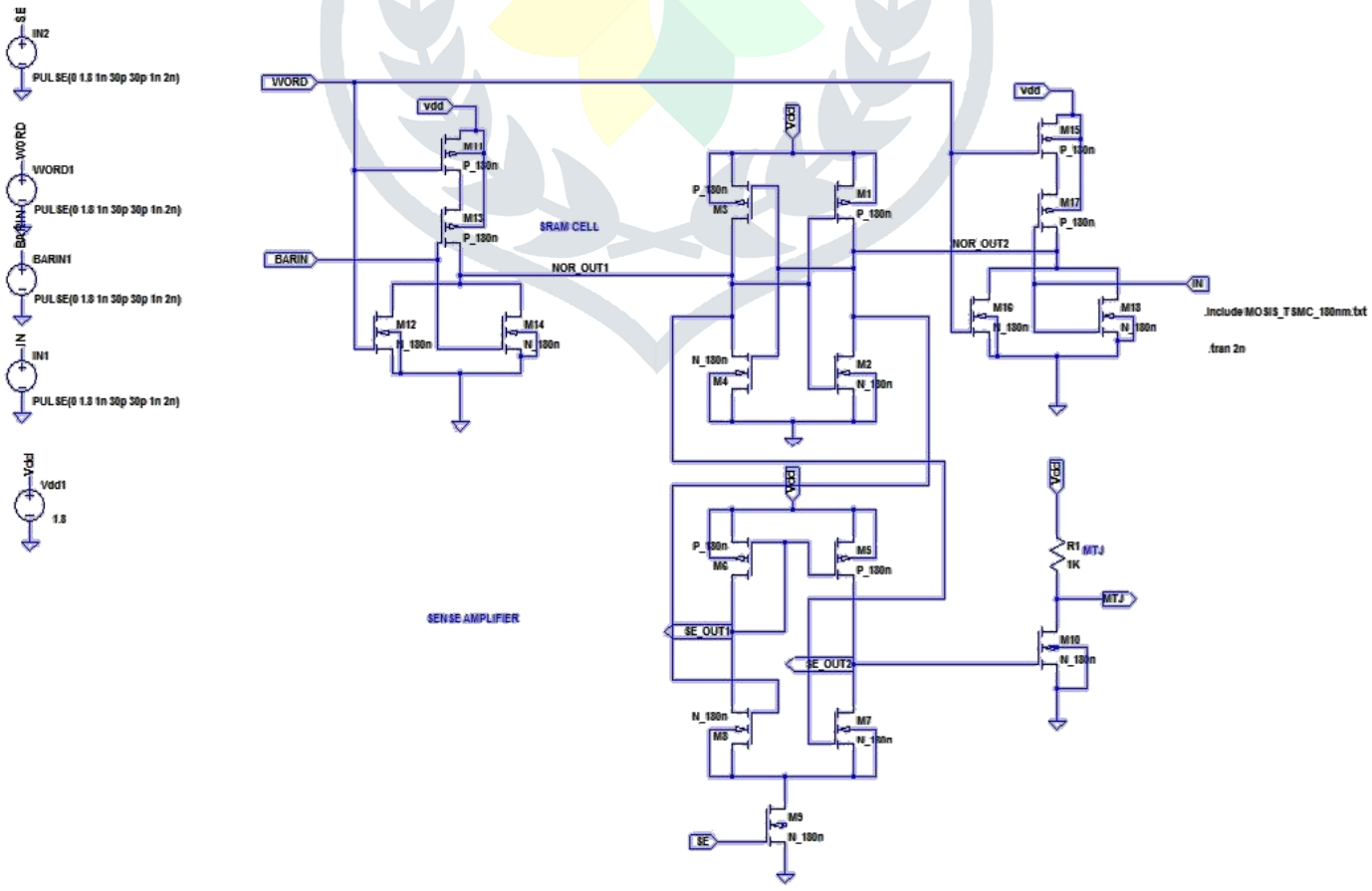

Figure 5: Schematic Circuit of Non-Volatile SRAM Based On MTJ

VI. RESULTS

Figure 6: Transient Response of Non-Volatile SRAM

VII. CONCLUSION

MTJ-based implication gates as basic elements which inherently realize a logic-in-memory architecture called stateful logic for which the memory and logic computing are combined based on existing STT-MRAM architectures. This opens an alternative path towards non-volatile MTJ-based computing devices and systems. Due to non-volatility and also because of eliminating extra charge-based logic gates, the MTJ-based stateful logic is expected to exhibit low power consumption, high logic density, and high speed operation simultaneously.

VIII. REFERENCES

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