DDS Based on Pipelined CORDIC Algorithm with Communication System

[1]Nita Patil, [2]Prof. Mrs. J.H.Patil

[1] Nita patil, Student of E & TC Dept.,P.S.G.V.P.Mandal's D N Patel College of Engineering,Shahada,Nandurbar ,
[2]Prof. J.H.Patil , Assit. Prof. Of E & TC Dept. ,P.S.G.V.P.Mandal's D N Patel College of Engineering,Shahada,Nandurbar,

Abstract—– **The theoretical analysis gives an overview of the functioning of DDS, especially with respect to noise and spurs. Different spur reduction techniques are studied in detail. Four ICs, which were the circuit implementations of the DDS, were designed. One programmable logic device implementation of the CORDIC based quadrature amplitude modulation (QAM) modulator was designed with a separate D/A converter IC. For the realization of these designs some new building blocks, e.g. a new tunable error feedback structure and a novel and more cost-effective digital power ramp generator, were developed. Implementing a DDS on an FPGA using Xilinx's ISE software.**

***IndexTerms*—CORDIC, DDS, NCO, FPGA, SFDR.**

I. INTRODUCTION

Frequency synthesis is an extremely important technology used in the field of telecommunications. A direct digital synthesizer (DDS) plays a vital role in microwave/radio frequency designs and projects that need a signal source which have no disturbances and little to no noise. A DDS, similar to a numerically controlled oscillator (NCO), is used to generate a sinusoid signal, or any other waveform of utmost clarity, that can switch frequencies very easily and quickly. It is a partial digital design which can be easily designed and implemented and yet provide a fine-tuning resolution.

In the field of electrical engineering, a DDS is usually preferred over an analog signal generator for capabilities such as the following [1]:

1. Extremely fast frequency tuning while keeping the phase continuous with no overshoots or undershoots
2. No need for manual tuning or tweaking with the accompanying redundancies
3. Digitally controlled environment that can be easily tested and reconfigured from anywhere at any time
4. Frequency resolution in the micro-hertz range
5. Immunity to many ambient problems (e.g., temperature, dust between components, dielectric presence, etc.)

The purpose of this paper is to help design such a DDS on an FPGA. With the growing needs of flexibility, extreme accuracy and effectiveness, FPGAs have started to play a very big role in the domain of digital circuit design. FPGAs are generally similar to development boards that are able to operate any circuit designed for them. They also have many switches and ports on the board that help in testing and debugging. The biggest advantage of using an FPGA is that designs can be created and changed over a very short period of time and unlike with application specific integrated circuits (ASICs), the designer does not have to wait many months for the circuit to be fabricated.

II. OVERVIEW OF CORDIC

CORDIC (for Coordinate Rotation DIgital Computer), also known as the digit-by-digit method and Volder's algorithm, is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions. It is commonly used when no hardware multiplier is available (e.g., simple microcontrollers and FPGAs) as the only operations it requires are addition, subtraction, bit shift and table lookup.

The CORDIC algorithm only performs shift and add operations and it can be easy to implement and also suitable for FPGA based design. It is necessary to analyze the various hardware architecture of CORDIC for the present research work. This work has considered four different hardware architectures of CORDIC. Its speed and area performance has been analyzed.

If the sine and cosine functions have been implemented in digital hardware, it needs more number of multipliers for many algebraic methods. FPGAs are suitable for hardware implementation of CORDIC algorithm as with other hardware circuitry.

CORDIC, as mentioned earlier, stands for Coordinate Rotation Digital Computer. It computes the rotation of vectors using simple additions and shifts. The mode operated is either rotation mode or vectoring mode. CORDIC can operate either in circular coordinate system, or in linear coordinate system, or in hyperbolic coordinate system.

The basic equation of CORDIC for ith iteration is given below, which is for circular coordinate system and for rotation mode of operation.

$$Xi+1 = [Xi - Ci * Yi * 2-i] * Ki$$
$$Yi+1 = [Yi + Ci * Xi * 2-i] * Ki$$
$$Zi+1 = Zi - Ci * \arctan(2-i)$$

Ci is the direction of rotation which has a value of either 1 or – 1 depending on whether the rotation is positive or negative. Ki is the scaling factor of ith iteration stage and it can to be computed at the end of all iterations since it comes out as a Product of all stages.

The theoretical value of K is given as

$$K = \pi i \ Ki = 0.60725$$

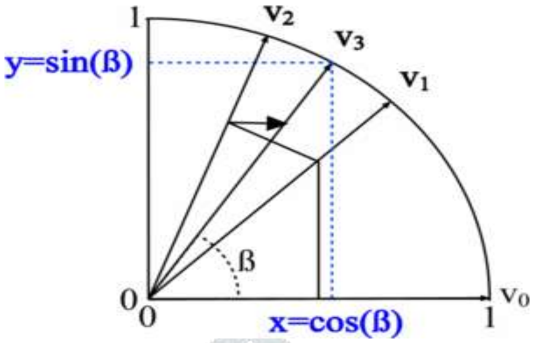

Figure 1 CORDIC algorithm in progress.

Fig. 2 shows the CORDIC stage for ith iteration

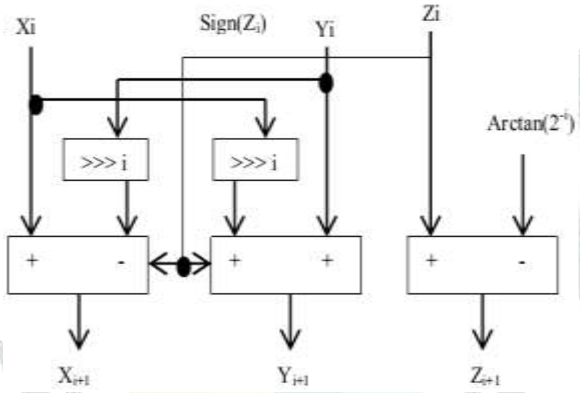

Figure 2 CORDIC stage for ith iteration

Pipelined CORDIC, has advantage over other fully dedicated architectural CORDIC (FDA) since it improves the speed of operation and also gives out varying outputs at every clock cycle, for varying inputs. The ith iteration stage of pipelined CORDIC is similar in structure to that of one in FDA except that registers are used to store the input and output values of ith iteration[1]. Figure 3 shows a stage of pipelined CORDIC. In designing dedicated pipelined architectures, one of either IN_REGS or OUT_REGS is eliminated to improve latency of the design.

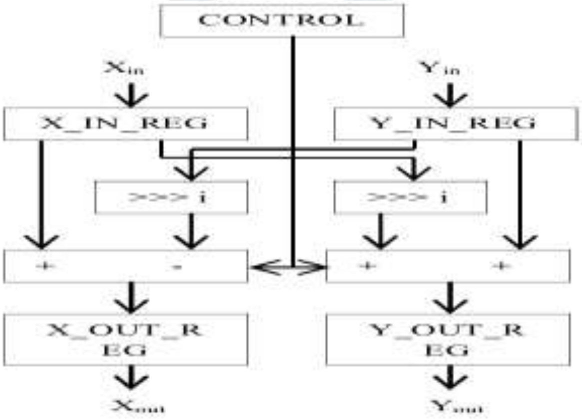

Figure 3 Pipelined CORDIC stage for ith iteration

III. LITERATURE SURVEY

1. Ayas Kanta Swain, and K. K. Mahapatra, (2013)[1]. FPGA Implementation of Pipelined CORDIC Based Quadrature Direct Digital Synthesizer with Improved SFDR - Direct Digital Synthesizers (DDSs) or Numerically Controlled Oscillators (NCOs) are nowadays prominently used in the applications of RF signal processing, satellite communications, etc. This paper brings out the FPGA implementation of one such DDS which has quadrature outputs. The proposed design, which is based on pipelined CORDIC, has considerable improvement in terms of spurious free dynamic range (SFDR) compared to other existing designs at reduced hardware. The design is implemented on Xilinx XC3S500E-4FG320 FPGA, fabricated in 90 nm process technology. The design has utilized 487 slices and 967 4-input look up tables (LUTs) as its hardware count. The maximum sampling frequency of the proposed design is 107.216 MHz. The SFDR of proposed DDS is -96.31 dBc.

2. T.Menakadevi¹, M. Madheswaran (2012) [2] Direct Digital Synthesizer using Pipelined CORDIC Algorithm for Software Defined Radio-This paper proposes Design and Implementation of CORDIC algorithm for Direct Digital Synthesizer. COordinate Rotation DIgital Computer (CORDIC) algorithm is an interesting technique for phase to sine amplitude conversion. The algorithm proposed in this design is to utilize dynamic transformation rather than ROM static addressing. The proposed CORDIC design is based on Pipeline data path Architecture. By using pipeline architecture, the design is able to calculate continuous input, has high throughput, and doesn't need ROM or registers to save constant angle iteration of CORDIC. CORDIC algorithm provides fast and area efficient computations of sine and cosine functions without using ROM LUTs. This paper is focused on the Direct Digital Synthesizer using CORDIC approach, to increase the speed with minimum area requirement in FPGA. To prove the better performance of proposed DDS architecture it is compared favorably with several existing DDS architectures.

3. Maher Jridi (2009)[3] Direct Digital Frequency Synthesizer with CORDIC Algorithm and Taylor Series Approximation for Digital Receivers- In this document we are presenting a new approach to design an optimised Direct Digital Frequency Synthesizer (DDFS) for complex demodulation used in digital receivers. For that, we suggest an adaptation of the phase to sine converter by combining the two following techniques:

1) an optimized COordinate Rotation DIgital Computer (CORDIC) algorithm
2) the principle of Taylor series approximation.

To validate our proposed approach, a DDFS with 8 Hz tuning frequency resolution and 20 bits output data (for sine and cosine waves) is being implemented in Xilinx FPGA device giving a maximum operating frequency of more than 306 MHz and a Spurious Free Dynamic Range (SFDR) of 112 dBc. To prove the good performances of the proposed approach, we compared it favourably with several existing DDFS architectures.

IV. DIRECT DIGITAL SYNTHESIZERS UNITS

DDFS is a fine resolution sinusoidal waveform generator which can generate signals with stable performance, in terms of amplitude, phase and frequency. DDFS implementation mainly relies upon integer arithmetic, allowing implementation on any hardware platform. The traditional DDFS architecture is shown in Fig. 4.

It consists of a phase accumulator, a phase to amplitude converter and a digital-to-analog converter (DAC).

The phase accumulator is a digital circuitry consisting of an adder with a feedback and an input as frequency control word (FCW). The phase accumulator receives an input called FCW which is linearly incremented in accordance with clock. The output of phase accumulator is fed into the phase to amplitude converter which is a sine/cosine generator that converts digital phase values into its equivalent digital sinusoidal amplitude. Most of the methods use the ROM based look-up table for sine/cosine generation. The linearly increasing output of the phase accumulator provides the address to the ROM to access the sine/cosine amplitude values stored in the lookup table [7]. The digital amplitude values from the phase to amplitude converter are then fed into the DAC to obtain the required sinusoidal output. The spectral purity of the sinusoidal output of the DDFS is dependent on the word size of the ROM and number of words in the look-up table.

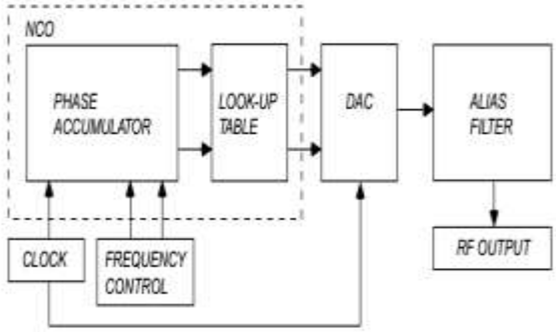

Figure 4 A Direct Digital Synthesizer

The FCW is added with the same value on each clock signal and the value is accumulated in the latch. For digital realization, the phase is quantized as

$$\theta = n/2^N$$

Where N is the size of the frequency control word and n is the value to be stored in maximum range selector register that takes on integer numbers in the range $0 \le n \le 2^N$.

The conventional implementation of DDS is a brute-force approach using a lookup table (Nicholas 1988). In this approach, the lookup table size grows exponentially as more bits are used to represent the sine and cosine waveforms, although a memory compression method applied to reduce the size of the lookup table.

V. PROPOSED DESIGN OF DDS

NCO comprises the increment register and phase accumulator logic. The increment register stores the binary value of frequency control register. The phase accumulator adds the phase increment value to its accumulator output value. The calculated accumulator output is used to address the look-up table which outputs the digital sample values of sine wave at current phase value.

In this study, the analog conversion of digital samples is not the main discussion area. The main discussion is done on the generation of digital samples according to the desired frequency and phase offset values. The basic DDS dataflow diagram is illustrated in Fig 4. The presented figure does not include digital to analog conversion structures.

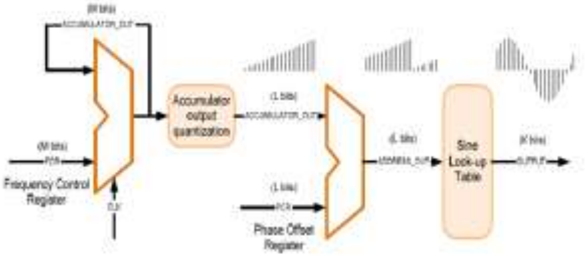

Figure 5 Basic DDS Data Flow Diagram

The frequency of the waveform depends on the reference clock frequency, the phase increment register value and length of phase accumulator. The waveform frequency is calculated using the formula given below.

$$F_{out} = \frac{FCR \times F_{ref}}{2^m}$$

The output of the DDS includes the spurious signals. The spurious signal sources can be ordered as below:

1. The reference clock
2. Phase truncation
3. Angle to amplitude conversion
4. Digital to analog conversion

The reference clock is the principal input for DDS. All the signal generation processes are done synchronously with reference clock. The phase accumulator increases the phase accumulator value at each reference clock cycle.

VI. RESULT & SIMULATION DISCUSSION

Figure.6. shows the simulation result of proposed DDS phase accumulator with 10MHz output frequency. The 32 bit adder output is truncated into 14 bits , only higher order bits are taken. The phase value will not be affected if the truncation is carried out because the phase information is only available in higher order bits.

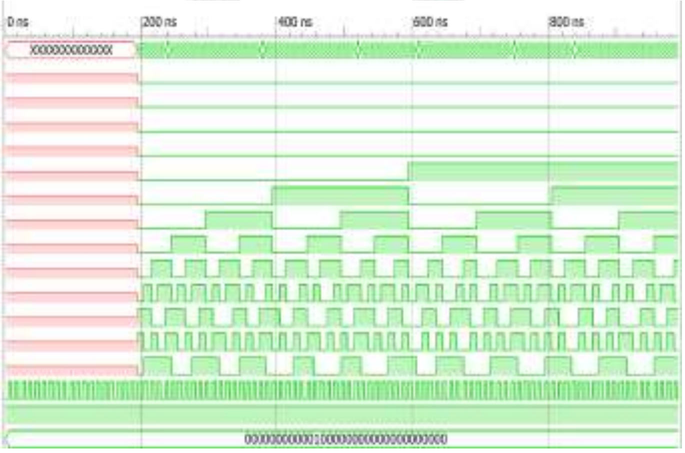

Figure 6 Phase accumulator output for fout = 10MHz

This module produces phase register output which is 13bit wide along with sine and cosine output. Figure.7. Shows the simulation result of pipelined CORDIC architecture. Xilinx ISE simulation tool produces the output in form of digital values.

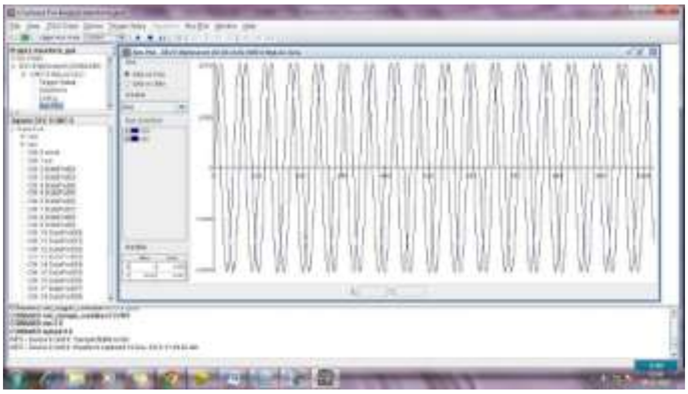

Figure 7 10 MHzSine and Cosine output of CORDIC Module

TABLE I. Proposed Comparison Table with Existing Designs

CORDIC Based DDFS	Madisetti [9]	Swartzlander [10]	Sung [11]	Proposed Design
Maximum Sampling rate (MHz)	80.4	101.8	100	200
SFDR (dBc)	81	90	84.4	120.49
Output Resolution (bits)	16	16	16	32

VII. **APPLICATIONS**

1. Tuning resolution of output frequency
2. Fast hopping of phase which reduces phase related errors
3. Remotely controllable
4. Better match of quadrature output when required.
5. To improves the speed of operation
6. Varying o/p at every clock cycle for varying i/ps.

VIII. ADVANTAGE

1. Pure digital architecture
2. Wide range
3. No setting problems
4. Stable
5. Fast response
6. Easily realized by programmable logic array
7. Easily reprogrammable and reconfigurable
8. Microcontroller adaptive control can be simply added for improving quality.

IX. **DISADVANTAGES**

1. Accuracy depends on integer number in Counters
2. Not suitable for high output frequency

X. CONCLUSION & FEATURE SCOPE

A novel DDFS architecture has been proposed to generate a sinusoidal signal. The proposed method is implemented based on Taylor Series polynomial approximations and improves the spectral purity remarkably. The replacement of look-up table with a digital combinational and sequential circuits results in the reduction of hardware complexity and also aids in faster computation.

Using Xilinx's ISE software and implementing the DDS on a Spartan-6 FPGA, the tutorial stepped through the different phases of an FPGA flow diagram and simultaneously showed screenshots to help orient the user. Finally, the thesis investigated the different results which were obtained when the inputs were varied.

This project does not implement an actual DAC, thus the next step would be to implement the DDS on the FPGA and feed the signal to a DAC and LPF whose output would then be given to an oscilloscope. There are also many algorithms being developed in the industry to reduce the different spurs generated in the DDS. Thus, additional future work for this project could entail implementing some of those algorithms in the design, and comparing a generic to an optimized DDS.

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