Neutral point clamped transformer less grid m connected inverter having voltage buck–boost capability for solar photovoltaic systems

[1]S.Sai Krishna,[2]S.Papa Rao
1PursuingM.Tech, PE Branch, Dept of EEE,Brilliant Institute of Engineering and Technology
2 Asst.Prof,EEE, Dept ,Brilliant Institute Of Engineering and Technology

Abstract: This study proposes a neutral point clamped grid-connected transformerless inverter for solar photovoltaic (PV) systems. This inverter has the capability to function in buck–boost mode. Thus the PV voltage level can be chosen to be of lesser value as compared to that of the existing buck type of inverters. This leads to increment in yield of power when PV modules are required to operate under mismatched conditions owing to possibility of more parallel connection of PV modules. Furthermore, buck–boost nature of the proposed inverter also facilitates operation under considerable variation in PV array voltage caused by wide changes in meteorological conditions. The other advantages of the inverter include: (a) elimination of concerns pertaining to the leakage current issues in transformerless grid-connected solar PV systems, (b) elimination of grid current sensor requirement, (c) elimination of shoot-through fault etc. The operating principle of the developed inverter supported by relevant analysis is presented. Control strategy devised for the inverter is provided. Results of detailed simulation studies carried out on MATLAB/Simulink platform are presented to ascertain viability of the proposed scheme. Exhaustive experimental validation has been carried out by utilizing a scaled down laboratory prototype of the proposed inverter.

1 Introduction

Grid-connected decentralised electrical power generation schemes have gained interest in recent years due to their several advantages, namely, less inertia, local power consumption, easy extendibility, elimination of storage requirement etc. Recent trend is to employ renewable energy sources (RESs) as the driving input for such schemes wherein they are connected to the ac distribution network through suitable power electronic interface [1]. Amongst the available RES, solar photovoltaic (PV) has evolved to be a prominent candidate for such schemes as it is green, available in abundance and inexhaustible [2]. However, the solar PV power being available in dc form requires the service of a dc–ac inverter to form the interfacing link between the PV source and the grid. A single-phase inverter is generally employed to form the aforementioned interface link as decentralised schemes are typically designed for low-power ratings (<5 kW). In recent years, the transformerless inverter topologies have become a popular choice for realising the aforementioned inverter due to their advantages such as low weight, less volume, high efficiency, low cost etc [3, 4]. However, the transformerless inverters lack galvanic isolation between grid and the PV source. This results in flow of leakage current through parasitic capacitances present between the ground and the PV source. The presence of the aforementioned leakage current in transformerless grid-connected inverters leads to

additional losses, distortion of grid current, increased safety and electromagnetic radiation concern [3].

To minimise the leakage current within permissible limit, several topologies for transformerless grid-connected inverter have been reported in this paper. On the basis of the strategies employed for leakage current minimisation, these topologies can be broadly classified into three groups. The first group of topologies attempt to maintain the common-mode voltage to be constant by ensuring that the PV source is made to float with respect to the grid during the freewheeling mode of operation [5–14]. However, the profile of the common-mode voltage in the aforementioned topologiesdepends on the parasitic capacitances (including junction capacitance of switches) present in the leakage current loop, their location and also on the magnitude of the grid voltage [15] and hence minimisation of leakage current within permissible value cannot be guaranteed. Furthermore, these topologies are based on H-bridge inverter structure which can operate only in buck mode, and hence the PV voltage must be greater than the peak amplitude of the grid voltage. Considering the expected variation in the magnitude of the PV voltage with changes in environmental conditions, sufficient margin has to be kept for the designed value of PV voltage. Higher the voltage level chosen, higher number of PV modules needs to be connected in series to form the PV array. With the increase in the number of series connected modules, the power yield from PV array reduces when there is a mismatch in environmental condition being experienced by the different modules of the array [16]. Furthermore, with increment in PV array voltage the magnitude of PV parasitic capacitance also increases thereby increasing the magnitude of the leakage current [3].

The second group of topologies try to minimise leakage current by clamping the common-mode voltage to half of the PV array voltage [15, 17–20]. These topologies also require the designed PV voltage level to be higher similar to that of H-bridge-based inverters and hence suffer from similar limitations pertaining to reduction in power yield from PV array.

The third group of topologies attempt to minimise leakage current by ensuring that either zero or constant voltage gets applied across the parasitic capacitors of the PV array. This is achieved by the following three procedures: (i) connecting the neutral terminal of the grid to the negative bus of the PV array [21–23], (ii) connecting the neutral terminal of the grid to the midpoint of the split capacitor connected across PV array (standard neutral point clamped (NPC) inverters) [24, 25] and (iii) connecting the neutral terminal of the grid to the midpoint of two PV arrays obtained by splitting the PV array into two halves [26–28]. As the neutral point of the grid is connected to the ground, the PV parasitic capacitors either get shorted or they are impressed with constantvoltage equal to half of the PV array voltage. This ensures minimal leakage current flow through PV parasitic capacitances. However, the inverter proposed in [21] is buck-type inverter. The scheme reported in [22] requires the presence of an additional dc–dc converter. The inverter presented in [23] is a buck–boost inverter, but it suffers from the drawback of asymmetrical operation as seen by the grid. The standard NPC-based inverter topologies require double the PV voltage compared with that of schemes based on H-bridge inverter [24, 25] and hence are extremely prone to power yield reduction under mismatched operating conditions. The inverter segment employed in [26] is a buck-type inverter. Furthermore, proper care needs to be taken to ensure permissible injection of dc current into the grid when voltages across the two PV arrays are not equal. The schemes reported in [27, 28] require that both the PV arrays to operate under same conditions to ensure symmetrical current

flow and injection of permissible amount of dc current into the grid. Furthermore, the energy outputs from PV arrays are required to be stored in a capacitor connected in parallel to the PV array over a half cycle of the grid voltage. This demands that two large capacitors be connected across each of the PV arrays to ensure maximum power extraction from both the arrays by reducing the magnitude of voltage ripple across the arrays.

To overcome the aforementioned limitations of transformerless grid-connected inverter topologies, a new scheme is proposed in this paper. The inverter employed in this scheme is based on NPC structure and can operate in buck–boost mode. This unique combination of NPC structure for the inverter and its ability to operate in buck–boost mode bestows the scheme with the following advantages:

PV voltage level can be chosen independent of the grid voltage owing to the involvement of the buck–boost inverter which facilitates to keep the designed voltage of the PV array to be low. Selection of lower value for the designed PV voltage makes the scheme less prone to suffer from low-power yield, whereas the individual PV modules are subjected to mismatched operating conditions.

- The NPC-based structure of the inverter leads to elimination of leakage current problem as PV parasitic capacitors will be impressed with either zero or constant voltage.
- The inverter is tolerant to shoot-through fault.
- The scheme requires six switches out of which four switches operate at grid frequency, whereas only two switches operate at high frequency. Furthermore, only two switches conduct at a given time.

Grid current is not required to be sensed.

The operating principle of the proposed inverter topology is explained in Section 2. Design criteria for various passive elements of the proposed topology are provided in Section 3. The control strategy devised for the scheme is presented in Section 4. To verify the effectiveness of the proposed scheme, detailed simulation studies are carried out and the simulated performance of the scheme is presented in Section 5. A scaled down laboratory prototype of the scheme is developed and exhaustive experimental studies have been carried out to confirm the viability of the scheme. The measured performance of the scheme is presented in Section 6.

2 Operating principle of the proposed inverter

The schematic circuit diagram of the proposed inverter is shown in Fig. 1a. As shown in this figure, a series combination of two capacitors is connected across the PV array. The midpoint of these two capacitors is connected to the neutral/ground terminal of the grid. This ensures that either zero or constant voltage is applied across the parasitic capacitances which exist between the PV array and the ground. The leakage current caused by the presence of aforementioned parasitic capacitances thus gets eliminated. The switches, S2, S3, S5 and S6, are required to have reverse voltage and reverse current blocking capability. Hence these switches can be realised either by employing reverse-blocking insulated gate bipolar transistors (RB-IGBTs) or a series combination of diode and IGBT/ metal–oxide–semiconductor field-effect transistor (MOSFET).

On

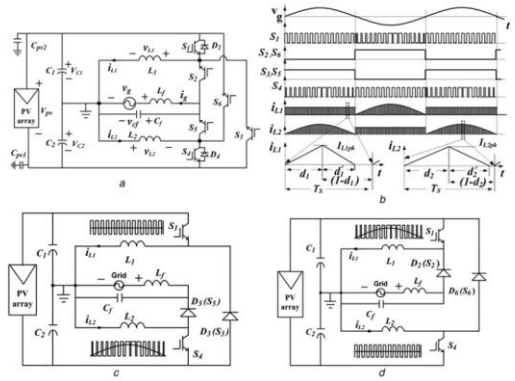


Fig. 1 Schematic diagrams associated with the proposed inverter

a Schematic power circuit diagram of the proposed inverter

b Switching pulses for the six switches of the proposed inverter along with inductor currents, iL1 and iL2

c Equivalent circuit diagram during the positive half cycle

d Equivalent circuit diagram during the negative half cycle

the contrary, switches, S1 and S4, can carry current in forward direction only owing to the structure and operating principle of the inverter. Furthermore, they need not have reverse voltage blocking capability. Hence they can be realised by employing IGBT/ MOSFET with or without having anti-parallel body diode. The combination of inductor, Lf and capacitor, Cf is employed to filter the current injected to the grid. The switching pulses for the six switches are depicted in Fig. 1b. From this figure it can be noted that out of six switches, two switches are operating at switching frequency and four switches are operating at grid frequency. The converter is made to operate in discontinuous conduction mode (DCM). The operation of the inverter is explained as follows.

2.1 Operation in positive half cycle of the grid voltage

In this half cycle, S2 and S6 are kept off while S3 and S5 are kept on as shown in Fig. 1b. The duty ratios of the switches, S1 and S4, are controlled such that voltage across each of the capacitors C1 and

C2 are maintained to be Vmpp/2, wherein Vmpp is the PV array voltage at its maximum power point (MPP). The equivalent circuit

diagram of the inverter in this half cycle is depicted in Fig. 1c. As gating pulses for S3 and S5 are provided for the entire half cycle, they are represented as diodes, D3 and D5, respectively, during this mode of operation.

When S1 is turned on, the current iL1 flowing through the inductor, L1, increases thereby accumulating energy received from C1. When S1 is turned off, the stored energy in L1 is transferred to the capacitor, C2 through S3 resulting in decrement of iL1 . As the voltage across C1 is maintained to be constant, the amount of energy it receives in a switching cycle from the PV array gets transferred to C2 in the same switching cycle. Thus all the energy from the PV array in a switching cycle is transferred to the capacitor C2. A part of this energy is transferred directly from the PV array and the remaining portion via C1 through S1, L1 and S3.

When S4 is turned on, the current, iL2 flowing through the inductor, L2 increases and hence it stores energy received from C2. When S4 is turned off, the stored energy in L2 is supplied to the grid through S5 and iL2 decreases. Thus grid is fed with the maximum available power of the PV array as voltages across these capacitors are maintained at Vmpp/2.

2.2 Operation in negative half cycle of the grid voltage

In this half cycle, S3 and S5 are kept off while S2 and S6 are kept on. The duty ratios of the switches, S1 and S4, are controlled such that voltages across each of the capacitors C1 and C2 are maintained to be Vmpp/2. The equivalent circuit diagram of the inverter in this half cycle is depicted in Fig. 1d. As gating pulses for S2 and S6 are provided for entire half cycle they are represented by diodes, D2 and D6, respectively.

The operation in this half cycle is similar to that of operation in positive half cycle, except that the roles of C2 and C1 are reversed. Here, C2 transfers energy to C1 through S4, L2 and S6, whereas C1 transfers energy to grid through S1, L1 and S2. However, irrespective of reversal of roles between these two capacitors, grid is fed with the maximum available power of the PV array as voltages across these capacitors are maintained at Vmpp/2.

The waveforms for the inductor currents, iL1 and iL2 , along with their zoomed views over an arbitrary switching cycle for operation in DCM are shown in Fig. 1b.

The voltage impressed across inductor, L1, is given by

$$v_{L1} = v_{C1}, \text{ for } 0, t, d_1T_s$$

$$= v_{cf}\, k - v_{c2}(1-k), \text{ for } d_1T_s, t, (d_1 + d_1')T_s$$

$$= 0, \text{ for } (d_1 + d_1')T_s, t, T_s$$

wherein k = 1 in the negative half cycle and k = 0 in the positive half cycle. The magnitude of the peak current, iL1pk, flowing through the inductor, L1, is given by

$$i_{L1pk} = \frac{v_{c1}\, d_1T_s}{L_1} \quad (1)$$

The voltage impressed across the inductor, L2, is given by

$$v_{L2} = v_{c2}, \text{ for } 0, t, d_2T_s$$

$$= -v_{cf}(1-k) - v_{c1}k, \text{ for } d_2T_s, t, (d_2 + d_2')T_s$$

$$= 0, \text{ for } (d_2 + d_2')T_s, t, T_s$$

The magnitude of the peak current, iL21pk, flowing through the inductor, L2, is given by

$$I_{L\,pk} = \frac{v_{c2}\, d_2T_s}{2\, L_2}$$

From the above discussion, it can be inferred that the grid is fed with the maximum available PV power in both the half cycles. Furthermore, in each of the half cycle, the grid is fed from capacitors whose voltages are maintained to be equal thereby eliminating the chance of dc current injection into the grid.

3 Selection criteria of various passive elements

The selection criteria of various passive elements for operation of the proposed inverter in DCM are as follows.

3.1 Selection of L1 and L2

The values of L1 and L2 are chosen so that the proposed inverter operates under DCM, whereas L1 and L2 are required to negotiate peak power. Following the procedure presented in [1], the critical values of L1 and L2 can be expressed as:

$$L_{critical} = \frac{V_{g2m} V_{c2max} T_s}{4 P_{pv\,max} (V_{gm} + V_{c\,max})^2} \quad (2)$$

whereinPpvmax is the maximum power output from PV source, Vcmax is the maximum value of voltage across C1 (or C2), Vgm is the peak value of grid voltage and Ts is the switching time period.

3.2 Selection of C1 and C2

The capacitors connected in parallel with the PV arrays, C1 and C2 are designed, as per guidelines provided in [29], as follows

Ppv max (3)

C1 = C2 = 4p fgVcDVc

whereinVc is the voltage across C1 and C2; Vc is the voltage ripple across C1 and C2; and fg is the grid frequency.

3.3 Selection of Lf and Cf

The grid side filters, Lf and Cf are designed based on expressions provided in [1] and are as follows

TsPpv max

Cf = VgmDV

1

Lf = (2p fc)2Cf

wherein V is the ac voltage ripple in Cf and fc is the cut-off frequency of filter.

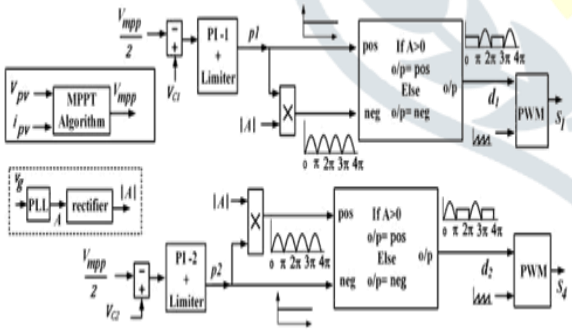


Fig. 2 Control structure of the proposed inverter for operation in DCM

4 Control strategy

The control strategy devised for DCM operation of the proposed inverter is shown in Fig. 2. A conventional maximum power point tracking (MPPT) algorithm is employed to generate reference voltage command for the array to operate the array at its MPP. This reference voltage command, Vmpp, is then halved and given as reference voltage commands for the capacitors, C1 and C2. The measured capacitor voltages, VC1 and VC2 , are then compared with their respective references and the errors are processed and manipulated to generate suitable duty ratios, d1 for switch S1 and d2 for switch S4. The manipulation of the duty ratios are carried out with the help of signal '|A|'. This signal is the rectified version of signal 'A' which is a sinusoidal signal having unit amplitude and is in synchronism with the grid voltage. The signal A is generated by employing a phase lock loop (PLL) algorithm. The steps involved in generation of duty ratios, d1 and d2, are as follows.

4.1 Generation of d1

The duty ratio, d1 needs to be controlled to maintain vC1 at its reference value, Vmpp/2. To achieve this, the error between reference command and the sensed vC1 is processed through the proportional–integral (PI) controller, PI-1 which generates the signal, p1 which is subsequently manipulated to generate the duty ratio, d1 as follows:

(A) Generation of d1 for positive half cycle: During positive half cycle energy is transferred from C1 to C2 through S1, L1 and S3 following the principle of a standard buck–boost dc–dc converter. Hence, the magnitude of d1 for positive half cycle is kept same as that of p1.

(B) Generation of d1 for negative half cycle: During negative half cycle, energy is transferred from C1 to the grid through S1, L1 and S2 as a buck–boost dc–dc converter. As the current injected to the grid needs to be made sinusoidal, the profile of d1 should also be sinusoidal function of time. The time varying sinusoidal profile is incorporated in d1 by multiplying p1 with the rectified unit sinusoidal function, |A|.

4.2 Generation of d2

The duty ratio, d2 needs to be controlled to maintain vC2 at its reference value Vmpp/2. To

achieve this the error between reference command and the sensed vC2 is processed through the PI controller, PI-2 which generates the signal, p2 which is subsequently manipulated to generate the duty ratio, d2 as follows:

(**A) Generation of d2 for positive half cycle:** During this half cycle energy is transferred from C2 to the grid through S4, L2 and S5. To ensure current injected to the grid is sinusoidal, the profile of d2 is made sinusoidally varying function of time by multiplying p2 with the signal, |A|.

(B) Generation of d2 for negative half cycle: During the negative half cycle energy is transferred from C2 to C1 through S4, L2 and S6. Hence, the magnitude of d2 for the negative half cycle is kept same as that of p2.

5 Simulated performance

To verify the effectiveness of the proposed scheme, MATLAB/ Simulink platform is utilised to simulate the scheme. Various components/elements considered for the simulated model are provided in Table 1. The insolation level on the PV array is set as 1000 W/m2 from 0 to 2 s, 800 W/m2 from 2 to 3.5 s and 600 W/ m2 from 3.5 s onwards. The temperature of the PV array is maintained as 30°C from 0 to 5 s and 20°C from 5 s onwards.

The variation in power output from the PV array with aforementioned values of insolation level and temperature is shown in Fig. 3a. The profiles of voltages across capacitors, C1 and C2, are shown in Fig. 3b. From this figure it can be noted that with changes in insolation level and temperature, these capacitor voltages also get adjusted to ensure that the system operates at MPP. Furthermore, irrespective of operating conditions of the PV array, both the capacitor voltages remain to be balanced.

The inductor currents, iL and iL during the starting of the simulation are provided in 1 Figs. 42a and b, respectively. The steady-state profile of iL and iL along with their magnified views are provided in Figs. 14c and 2 d, respectively, to highlight the operation of the converter in DCM.

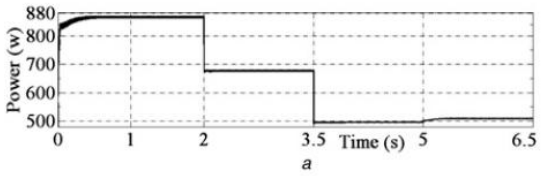
The current being fed to the grid is shown in Fig. 5a. The magnified views of the grid voltage and the grid current during steady-state operation is shown in Fig. 5b from where it can be noted that the grid current is in phase with the grid voltage. The total harmonic distortion (THD) and dc component in grid current is shown in Fig. 5b and it can be inferred that the THD is about 3% and that the dc component is almost zero.

6 Experimental validation

To confirm the viability of the proposed scheme, detailed experimental validations have been carried out on a prototype of the scheme developed for the purpose. A single-phase autotransformer is utilised to step down the grid voltage to the order of 50–110 V in order to demonstrate the operation of the inverter in both buck and boost modes. The phase information of

Table 1 Parameters/elements considered for the simulation study

Parameter	Value
grid voltage, V_g	230 V
$L_1 = L_2$	0.1 mH
$C_1 = C_2$	3300 μF
grid side filters, C_f and L_f	2 μF and 4 mH
switching frequency, F_s	20 kHz
MPPT algorithm	incremental conductance



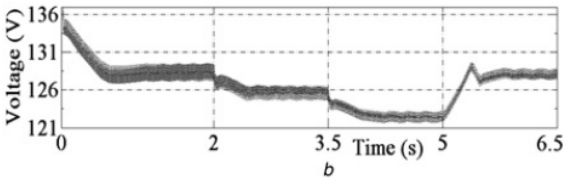


Fig. 3 Simulated performance of the system

a Power output from the PV array

b Voltage across capacitors, C1 and C2

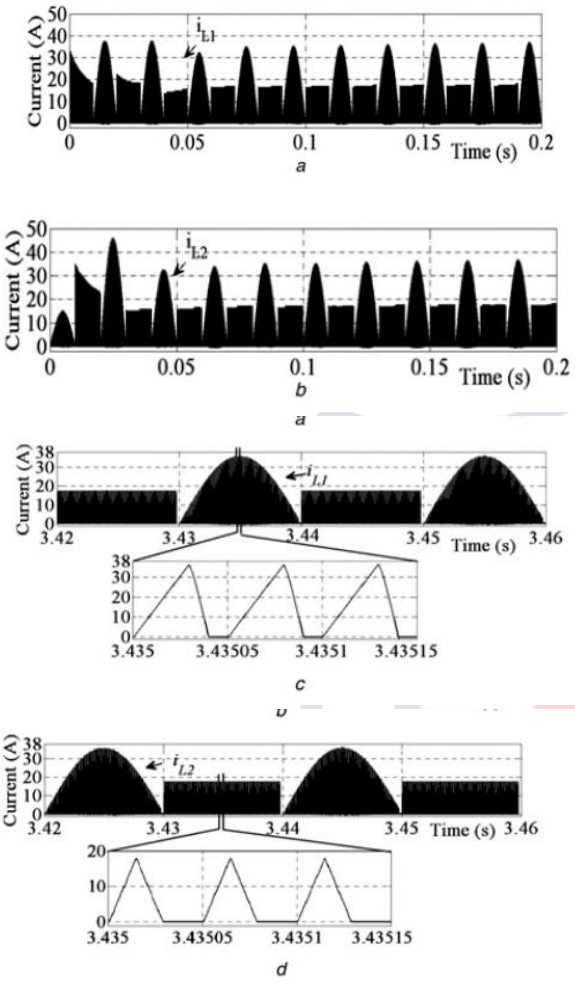


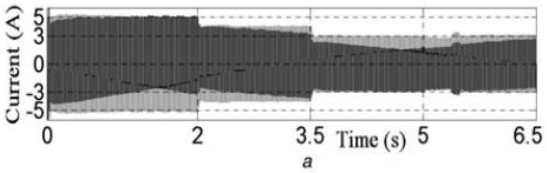
Fig. 4 Simulated performance showing the profiles of iL1 and iL2

a iL1 at starting

b iL2 at starting

c Steady-state profile of iL1 along with its magnified view

d Steady-state profile of iL2 along with its magnified view



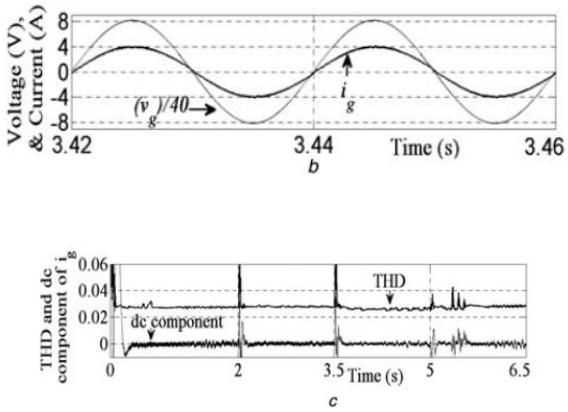


Fig. 5 Simulated performance of the system

a Grid current

b Magnified view of grid voltage and grid current at a given steady-state condition

c THD and dc current component of the grid current.

the grid voltage is obtained by employing enhanced PLL algorithm [30]. The PV array is realised by Agilent make solar array simulator, E4360A. This simulator takes input in the form of Impp, Vmpp, Isc and Voc, wherein Isc is the short-circuit current and Voc is the open-circuit voltage of the PV array. By altering these parameters manually, changes in operating condition on the PV array can be emulated. Other relevant parameters/elements employed to develop the laboratory prototype are given in Table 2. A photograph of the experimental setup is shown in Fig. 6a.

The steady-state response of the inverter while it is being operated in buck mode is shown in Fig. 6b. The grid voltage is set at 50 V.

The MPP values for the PV array are set as, Vmpp = 90 V and Impp = 1.5 A. From Fig. 6b, it can be inferred that both the

Table 2 Parameters/elements employed to realise the laboratory prototype

Parameter	Value/range
PV voltage, V_{pv}	50–100 V
PV current, I_{pv}	0–3 A
capacitors, C_1 and C_2	3300 μF
inverter output filters, C_f and L_f	2 μF and 4 mH
inductors, L_1 and L_2	0.1 mH
MPPT algorithm	incremental conductance
power rating	200 W
switches, S_1 and S_4	IRG7PH42UPbF
switches, S_2, S_3, S_5 and S_6	IXRH40N120
switching frequencies for S_1 and S_4	15 kHz
digital controller	TMS320F28335

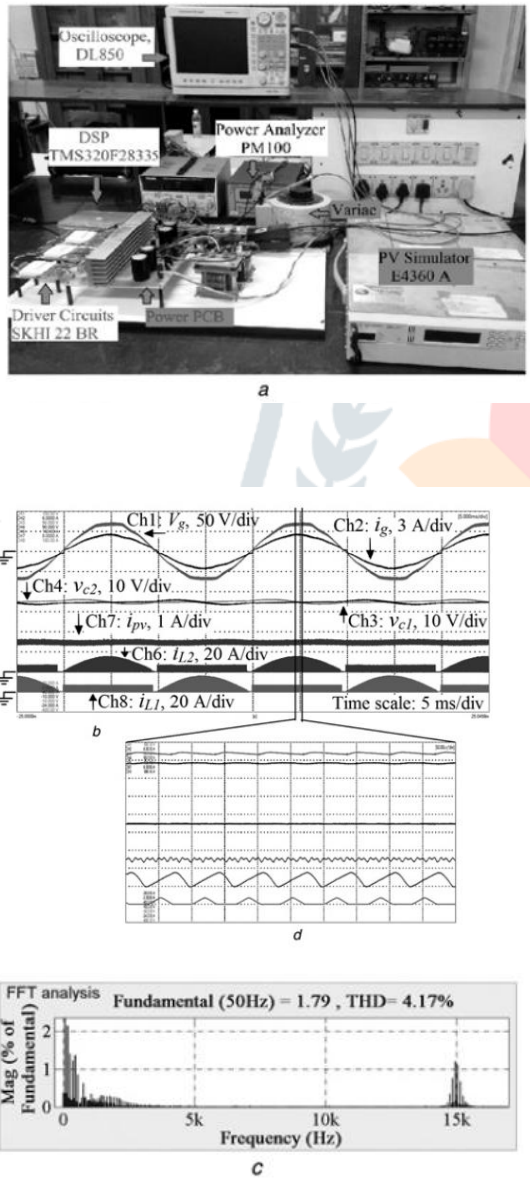
Fig. 6 Experimental validation

a Photograph of the experimental setup

b Steady-state response of the system in buck mode of operation

c Frequency spectrum of the grid current during buck mode of operation

d Magnified view of steady-state response over few switching cycles



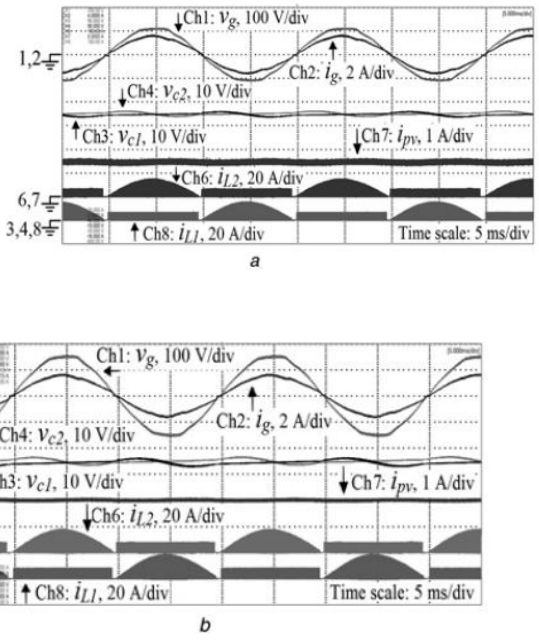


Fig. 7 Experimental results

a Steady-state response of the system while operating in buck–boost mode with grid voltage set at 80 V

b Steady-state response of the system while operating in buck–boost mode with grid voltage set at 110 V

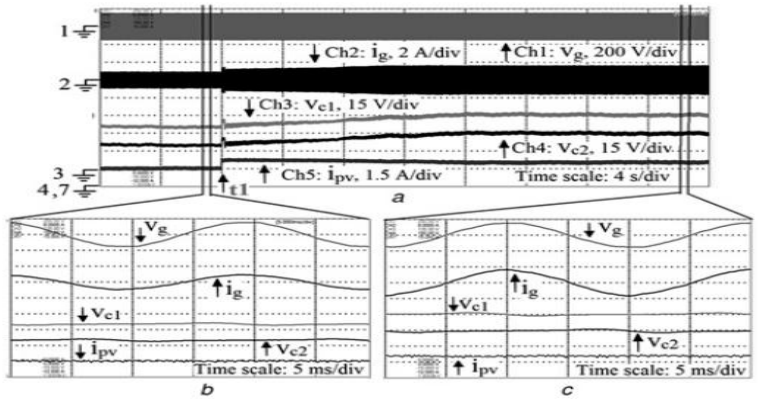


Fig. 8 Experimental results

a Response of the system subjected to step increment in MPP voltage and current

b Magnified view of the steady-state response of the system before changes in MPP condition were made at instant t1

c Magnified view of the steady-state response of the system after changes in MPP condition were made

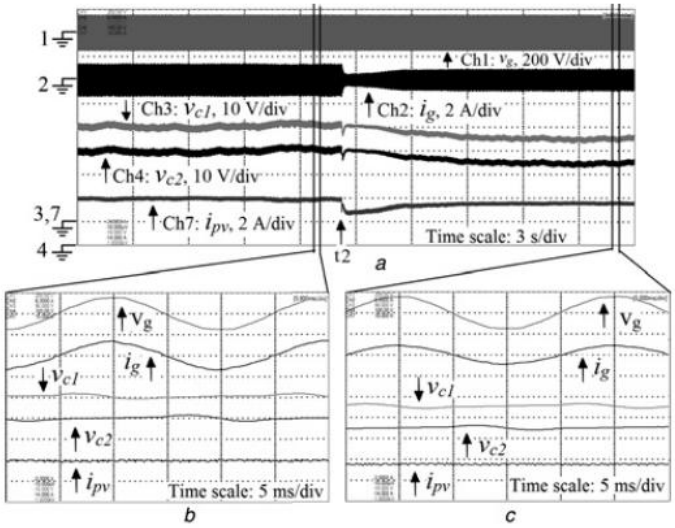


Fig. 9 Experimental results

a Response of the system subjected to step decrement in MPP voltage and current

b Magnified view of the steady-state response of the system before changes in MPP condition were made at instant t2

c Magnified view of the steady-state response of the system after changes in MPP condition were made

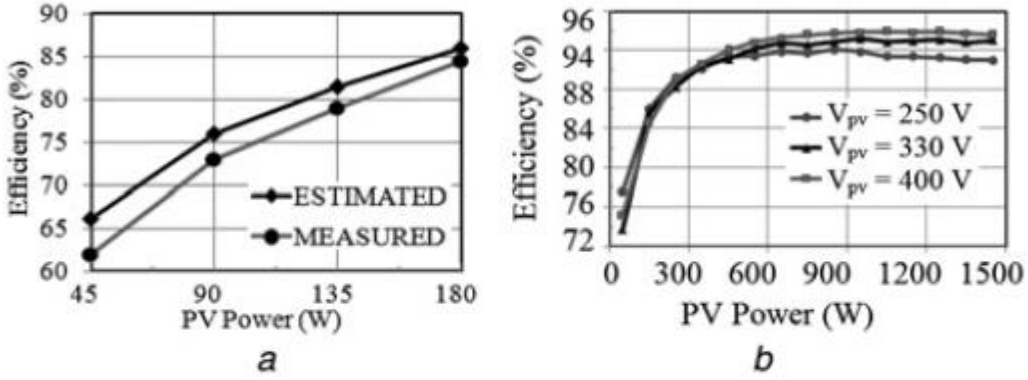


Fig. 10 *Efficiency curves of the proposed inverter*

a Measured and estimated efficiency curves when $V_{pv} = 90$ V and $V_g = 110$ V
b Estimated efficiency curves when $V_g = 230$ Vand $V_{pv} = 250$, 330 and 400 V

capacitor voltages are maintained at 45 V implying that the PV array is being operated at its MPP. The grid current is in phase with the grid voltage and its shape is fairly sinusoidal. Frequency spectrum of the grid current is shown in Fig. 6c which shows that the THD of the grid current is about 4% and the dc component present is about 0.06%. A magnified view of Fig. 6a over few switching cycle is shown in Fig. 6d to highlight operation of the inverter in DCM.

Steady-state response of the system when it is operating in buck– boost mode is shown in Figs. 7a and b. In case of Fig. 7a, the grid

voltage is set at 80 V and the MPP of the PV array is set as, Vmpp = 90 V and Impp = 1.5 A. For the result shown in Fig. 7b, the grid voltage is set at 110 V and the MPP of the PV array is set as,

Vmpp = 90 VandImpp = 2 A. From these measured performances, it can be inferred that the system operates satisfactorily in buck–boost mode ensuring MPPT operation while ensuring that sinusoidal current is being injected to the grid. The THD in grid current shown in Figs. 7a and b is found to be around 4.3 and 4.38%, respectively.

The responses of the system subjected to changes in environmental condition are shown in Figs. 8 and 9. The changes in environmental condition are emulated by changing MPP values of the PV array by appropriately changing the input commands of the solar array simulator, E4360A. The responses of the system subjected to step increment and decrement in MPP values are shown in Figs. 8 and 9, respectively. The grid voltage is set at 110 V for both the cases. For the response shown in Fig. 8a, step increment in MPP values are given at the instant, t1. Till the

instant, t1, the MPP values of the PV array are set at Vmpp =

70 Vand Impp = 1.5 A. From Fig. 8a, it can be inferred that the

system is operated at its MPP with capacitor voltages being maintained at 35 V. Magnified view of Fig. 8a, while the system is operating at steady-state condition with the aforesaid MPP values, is shown in Fig. 8b. At the instant, t1, the MPP values of

the PV array are changed to Vmpp = 90 VandImpp = 2 A. It can be inferred from Fig. 8a that the system tracks the new MPP

satisfactorily. Magnified view of Fig. 8a around a point where the system is operating at

steady-state condition with these new set of MPP values is shown in Fig. 8c. For the response shown in Fig. 9a, step decrement in MPP values are given at instant, t2. Till

the instant, t2, the MPP values are set at Vmpp = 80 VandImpp = 2 A. At the instant, t2, the MPP values are changed to Vmpp = 70 VandImpp = 1.5 A. From Fig. 9a it can be inferred that the inverter is capable of tracking MPP satisfactorily irrespective of step

decrement in MPP values. The magnified views of Fig. 9a around a point when the system is operating at steady state before and after the MPP values being changed are shown in Figs. 9b and c, respectively.

Table 3 Comparison of estimated/calculated circuit losses

Scheme	Loss at 1 kW
H5 [7]	27.71 W [13]
HERIC [14]	23.03 W [13]
H6 [6]	25.37 W [13]
proposed	38 W

Table 4 Comparison of the proposed inverter with other NPC inverters which can operate in buck–boost

	Aalborg [28]	Kasa [27]	Proposed	Remarks
C_{in}	$\frac{1.91P}{2\omega V_c \Delta V_c}$	$\frac{1.91P}{2\omega V_c \Delta V_c}$	$\frac{P}{2\omega V_c \Delta V_c}$	input capacitance requirement is 1.91 times less in the proposed scheme
O. S.	not guaranteed	not guaranteed	guaranteed	Aalborg and Kasa inverters require both the PV arrays to operate at the same condition which may require operation of one of the PV arrays other than its MPP
η, %	98.1	96.5	95	efficiency in the proposed scheme is less, but it can be improved by designing the inverter to operate at continuous conduction mode (CCM)

Cin = input capacitance requirement, O.S.=operational symmetry in positive and negative half cycles of the grid voltage, η=estimated efficiency at 1 kW, Vc and Vc = voltage and ripple voltage across input capacitor, ω = 2πfg, fg = grid frequency and P=total PV power (assuming two PV arrays of Aalborg and Kasa inverters are operating at same condition).

To measure the efficiency of the laboratory prototype, the following procedure has been pursued. The PV array voltage is maintained at the MPP of 90 V as the maximum voltage limit of the available solar array simulator, E4360A employed for the purpose is 90 V. The grid voltage is maintained at 110 V. The power injected to the grid is measured by the power analyser, PM100 which is then divided by the power output from the PV array to obtain the overall efficiency of the system. Power output from the PV array is noted from the display of the solar array simulator, E4360A. The efficiency thus obtained is the global efficiency of the system including losses incurred in all the active and passive components of the inverter. The efficiency curves so determined are shown in Fig. 10a. As the output voltage of E4360A is limited to 90 V, in order to obtain the efficiency for the entire range of operation of the proposed inverter, efficiency is estimated for the system by following the procedure presented in [31, 32]. The estimated efficiency curve of the system while the PV array voltage is maintained at the MPP of 90 V is also plotted in Fig. 10a. From this figure, it can be inferred that the estimated efficiency curve is in close agreement with the measured efficiency curve. Hence it can be concluded that the procedure for determining the estimated efficiency is quite realistic. Subsequently, the overall efficiency curves of the system are estimated for the entire range of its operation and they are depicted in Fig. 10b. From this figure, it can be observed that the efficiency in the order of 94.5% is achieved from the proposed inverter. A comparison of the circuit losses incurred in the proposed inverter with that of three traditional transformerless inverter schemes is provided in Table 3. From this table and Fig. 10b it can be observed that the estimated efficiency of the proposed inverter is ~3% less as compared with the existing transformerless inverters. However, this marginal decrement in efficiency

for the proposed inverter is complemented by its several advantages over its traditional counter parts which are as follows: (a) capability to operate in buck–boost mode thereby allowing wide variation in PV array voltage, (b) tolerant to shoot-through fault thereby improving reliability, (c) elimination of grid current sensor requirement and (d) elimination of leakage current.

A comparison of the proposed inverter with other NPC inverters which can operate in buck–boost mode is provided in Table 4. From this table, it can be inferred that the proposed scheme is advantageous over other two schemes in terms of input

capacitance requirement and assurance of symmetrical operation in both the half cycle of the grid voltage. However, the efficiency of the proposed scheme is slightly less as compared with the other schemes mainly due to its operation in DCM.

7 Conclusion

An NPC transformerless grid-connected inverter for solar PV systems is presented in this paper. The proposed inverter has the capability to operate in buck–boost mode. This feature gives freedom to the designer to select optimised voltage level for the PV array. Wide variation in PV array voltage due to changes in environmental condition can also be accommodated owing to buck–boost nature of the inverter. Apart from these, the other advantages of the inverter includes: (a) elimination of concerns pertaining to the leakage current issue in transformerless grid-connected solar PV systems, (b) elimination of grid current sensor requirement, (c) elimination of shoot-through problem etc. The operation of the inverter supported by relevant analysis is presented. Control strategy devised for the inverter is provided. The effectiveness of the scheme has been ascertained by performing detailed simulation studies. Experimental validation of the proposed scheme is carried out by utilising a laboratory prototype developed for the purpose.

8 Acknowledgment

This work was supported by the National Centre for Photovoltaic Research and Education, funded by the Ministry of New and Renewable Energy, Government of India.

9 References

1 Prasad, B.S., Jain, S., Agarwal, V.: ‘Universal single-stage grid-connected inverter’, IEEE Trans. Energy Convers., 2008, 23, (1), pp. 128–137

2 Jinn-Chang, W., Kuen-Der, W., Hurng-Liahng, J., et al.: ‘Small-capacity grid-connected solar power generation system’, IET Power Electron., 2014, 7, (11), pp. 2717–2725

3 Kjaer, S.B., Pedersen, J.K., Blaabjerg, F.: ‘A review of single-phase grid connected

inverters for photovoltaic modules’, IEEE Trans. Ind. Appl., 2005, 41, (5), pp. 1292–1306

4 Woo-Jun, C., Kyu-Tae, K., Yong-Won, C., et al.: ‘Evaluation and analysis of transformerless photovoltaic inverter topology for efficiency improvement and reduction of leakage current’, IET Power Electron., 2015, 8, (2), pp. 255–267

5 Yang, B., Li, W., Gu, Y., et al.: ‘Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system’, IEEE Trans. Power Electron., 2012, 27, (2), pp. 752–762

6 Yu, W., Lai, J.-S., Qian, H., et al.: ‘High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated ac-module applications’,

IEEE Trans. Power Electron., 2011, 26, (4), pp. 1253–1260

7 Victor, M., Greizer, F., Bremicker, S., et al.: ‘Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into a alternating current voltage’. DE Patent DE102004030912 (B3), January 2006

8 Xiao, H.F., Liu, X.P., Lan, K.: 'Zero-voltage-transition full-bridge topologies for transformerless photovoltaic grid-connected inverter', IEEE Trans. Ind. Electron., 2014, 61, (10), pp. 5393–5401

9 Wenfeng, C., Haoze, L., Yunjie, G., et al.: 'Hybrid-bridge transformerless photovoltaic grid-connected inverter', IET Power Electron., 2015, 8, (3), pp. 439–446

0 Gu, B., Dominic, J., Lai, J., et al.: 'High reliability and efficiency single-phase transformerless inverter for grid connected photovoltaic systems', IEEE Trans. Power Electron., 2013, 28, (5), pp. 2235–2245

11 Ji, B., Wang, J., Zhao, J.: 'High-efficiency single-phase transformer-less PV H6 inverter with hybrid modulation method', IEEE Trans. Ind. Electron., 2013, 60, (5), pp. 2104–2115

12 Islam, M., Mekhilef, S.: 'H6-type transformerless single-phase inverter for grid-tied photovoltaic system', IET Power Electron., 2015, 8, (4), pp. 636–644

13 Zhang, L., Sun, K., Xing, Y., et al.: 'H6 transformerless full-bridge PV grid-tied inverters', IEEE Trans. Power Electron., 2014, 29, (3), pp. 1229–1238

14 Schmidt, H., Christoph, S., Ketterer, J.: 'Current inverter for direct/ alternating currents, has direct and alternating connections with an intermediate power store, a bridge circuit, rectifier diodes and a inductive choke'. DE Patent DE10221592 (A1), December 2003

15 Zhang, L., Sun, K., Feng, L., et al.: 'A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters', IEEE Trans. Power Electron., 2013, 28, (2), pp. 730–739

16 Bastidas-Rodriguez, J.D., Franco, E., Petrone, G., et al.: 'Maximum power point tracking architectures for photovoltaic systems in mismatching conditions: a review', IET Power Electron., 2014, 7, (6), pp. 1396–1413

17 Xiao, H.F., Lan, K., Zhou, B., et al.: 'A family of zero-current-transition transformerlessphotovoltaic grid-connected inverter', IEEE Trans. Power Electron., 2015, 30, (6), pp. 3156–3165

18 Xiao, H.F., Lan, K., Zhou, B., et al.: 'A quasi-unipolar SPWM full-bridge transformerless PV grid-connected inverter with constant common-mode voltage', IEEE Trans. Power Electron., 2015, 30, (6), pp. 3122–3132

19 Huafeng, X., Xipu, L., Ke, L.: 'Optimised full-bridge transformerless photovoltaic grid-connected inverter with low conduction loss and low leakage current', IET Power Electron., 2014, 7, (4), pp. 1008–1015

20 González, R., López, J., Sanchis, P., et al.: 'Transformerless inverter for single-phase photovoltaic systems', IEEE Trans. Power Electron., 2007, 22, (2), pp. 693–697

21 Gu, Y., Li, W., Zhao, Y., et al.: 'Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems', IEEE Trans. Power Electron., 2013, 28, (2), pp. 793–805

22 Shen, J.-M., Jou, H.-L., Wu, J.-C.: 'Novel transformerless grid-connected power converter with negative grounding for photovoltaic generation system', IEEE Trans. Power Electron., 2012, 27, (4), pp. 1818–1829

23 Schekulin, D.: 'Grid-Connected photovoltaic system'. Germany Patent DE197 32 218 Cl, March 1999

24 Xiao, H., Xie, S.: 'Transformerless split-inductor neutral point clamped three-level

PV grid-connected inverter', IEEE Trans. Power Electron., 2012, 27, (4), pp. 1799–1808

25 Taallah, A., Mekhilef, S.: 'Active neutral point clamped converter for equal loss distribution', IET Power Electron., 2014, 7, (7), pp. 1859–1867

26 Shimizu, T., Hashimoto, O., Kimura, G.: 'A novel high-performance utility-interactive photovoltaic inverter system', IEEE Trans. Power Electron., 2003, 18, (2), pp. 704–711

27 Kasa, N., Iida, T., Iwamoto, H.: 'Maximum power point tracking with capacitor

identifier for photovoltaic power system', Proc. Inst. Electr. Eng., 2000, 147, (6), pp. 497–502

28 Wu, W., Ji, J., Blaabjerg, F.: 'Aalborg inverter – a new type of 'buck in buck, boost in boost' grid-tied inverter', IEEE Trans. Power Electron., 2015, 30, (9), pp. 4784–4793

29 Billy, M.T.H., Henry, S.C.: 'An integrated inverter with maximum power tracking for grid-connected PV systems', IEEE Trans. Power Electron., 2005, 20, (4), pp. 953–962

30 Karimi-Ghartemani, M.: 'A unifying approach to single-phase synchronous reference frame PLLs', IEEE Trans. Power Electron., 2013, 28, (10), pp. 4550–4556

31 Drofenik, U., Kolar, J.W.: 'A general scheme for calculating switching- and conduction-losses of power semiconductors in numerical circuit simulations of power electronic systems'. Proc. Int. Power Electronics Conf. (IPEC'05), 2005, pp. CD-ROM

32 Wiechmann, E.P., Aqueveque, P., Burgos, R., et al.: 'On the efficiency of voltage source and current source inverters for high-power drives', IEEE Trans. Ind. Electron., 2008, 55, (4), pp. 1771–1782