Phase-Shift Control for High-Voltage DC-Based System with Modular Multi-Level DC/DC Converter

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Abstract: Dc-based distributions and dc-based micro grids are recognized as the promising solutions for future smart-grid systems due to their clear advantages of flexibility for photovoltaic and fuel cells interface, without frequency stability, high conversion efficiency, and easy system control. The Modular Multilevel Converter (MMC) represents an emerging topology with a scalable technology making high voltage and power capability possible. The MMC is built up by identical, but individually controllable sub modules. A control scheme with a new sub module capacitor voltage balancing method is also proposed in this paper. Modular multilevel converters, based on cascading of half bridge converter cells, can combine low switching frequency with low harmonic interference. They can be designed for high operating voltages without direct series connection of semiconductor element. The high switch voltage stress in the primary side is effectively reduced by the full bridge modules in series. In this paper by investigating by investigating the topology derivation principle of the phase-shift-controlled three-level dc/dc converters, the modular multilevel dc/dc converters, by integrating the full bridge converters and three-level flying capacitor circuit, the proposed concept is implemented to control of DC motor using modular dc-dc converter with MATLAB/SIMULINK software.

Keywords: Input Voltage Auto Balance, Modular Multilevel DC/DC Converter, Phase-Shift Control Scheme, Zero-Voltage Switching (ZVS).DC Motor

I. INTRODUCTION

The modular multilevel converter (MMC)-based high voltage directs current (HVDC) system is a new type of voltage source converter (VSC) for medium or high voltage direct current power transmission. Recently, it has become more competitive because it has advantages over normal VSC-HVDC system such as low total harmonic distortion, high efficiency, and high capacity [1, 2]. The operation of the MMC-HVDC system has been investigated by many authors over the world. In [3-5], the authors presented the control strategies for eliminating the circulating currents and maintaining the capacitor voltage balancing of the MMC. The dynamic performances of the MMC-HVDC system have been analyzed in [6]. Similar to other HVDC systems, the stable and reliable operation of the system must be researched carefully, especially when the system operates under fault conditions. In [6-8], the authors showed out the control methods of the MMC-HVDC system under the unbalanced voltage conditions. Almost all of them only focus on the use of proportional-integral (PI) current controllers in the synchronous rotating reference frame (dq-frame) for enforcing steady-state error to zero.

However, the use of these PI current controllers will be difficult under the unbalanced voltage conditions because ofthe complex control of the positive and negative sequence components of the currents [6-8].Recently, the simple proportional-resonan (PR) current controllers in the stationary reference frame (αβ-frame) have been developed to overcome this problem [10]. The most important performance of the PR current controllers is that the currents are controlled directly in the αβ-frame. Therefore, the complicated analysis of the positive and negative sequence components of the currents is ignored. In this paper, the flying capacitor and full-bridge converters are combined and integrated to derive the advanced modular multilevel dc/dc converters for the high step-down and high power dc-based conversion applications. Due to the charging and discharging balance of the built-in flying capacitor, the input voltage auto balance ability is naturally realized, which halves the switch voltage stress and overcomes the input voltage imbalance. Furthermore, the phase-shift control strategy can be adopted to achieve the soft-switching operation and reduce the switching losses. The concept of modular

multilevel dc/dc converters may provide a clear picture on high-voltage dc/dc topologies for the dc-based distribution and micro grid systems.

II. DERIVATION LAW OF MODULAR MULTILEVEL CONVERTERS

The derivation process of the proposed modular multilevel dc/dc converters is discussed in this section. It is well known that the neutral-point-clamped (NPC) converters and flying capacitor-based converters are the major multilevel topologies for the high-voltage and high-power applications. For the conventional NPC converters with pulse width modulation control, the abnormal operation condition, such as the mismatch in the gate signals, may cause the voltage imbalance of the input capacitors. Therefore, the converter reliability is impacted. Furthermore, the phase-shift control scheme is not suitable for the conventional NPC converters, which leads to large switching losses. Fortunately, by inserting a small flying capacitor parallel connected with the clamping diodes, the input capacitor voltages are automatically shared because the flying capacitor can be directly parallel with the series input capacitors alternatively. More importantly, the phase-shift control strategy can be easily applied to achieve zero-voltage-switching (ZVS) operation without adding any other power components. The phase-shift controlled three-level dc/dc converter is plotted in Fig. 1(c). From another point of view, the phase-shift-controlled TLC can be regarded as the combination and integration of the three-level NPC converter as given in Fig. 1(a) and the three-level flying capacitor-based circuit as shown in Fig. 1(b), where the input capacitors and active power switches are reused and shared to reduce the circuit complexity. As a result, the advantages of the NPC converter and flying capacitor-based circuit are kept whereas their inherent disadvantages are effectively avoided. Many further improvements are made for the combined phase shift-controlled TLC by adding some active or passive components to extend the soft-switching operation range.Based on the previously summarized combined multilevel derivation principle, it is innovative and attractive to consider the possibility of combination of the other fundamental multilevel topologies. For example, the cascaded full-bridge converter, or the ISOP full-bridge converter, and the three-level flying capacitor-based converter are combined and integrated to derive the advanced modular multilevel dc/dc converters, which is detailed illustrated in Fig. 2. The time sequence of the leading leg in the phase-shift-controlled full-bridge converters is kept constant and only the phase of the

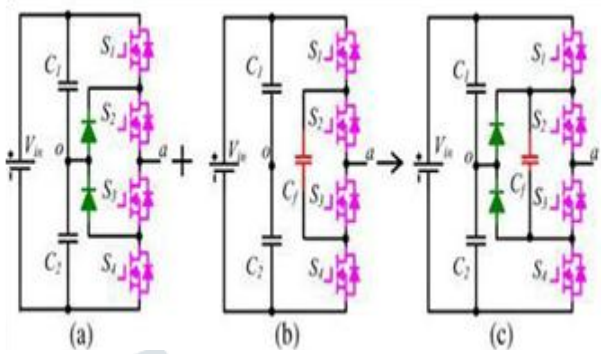


Fig.1. Derivation of novel TLC: (a) NPC TLC, (b) flying capacitor-based TLC, and (c) phase-shift-controlled combined TLC.

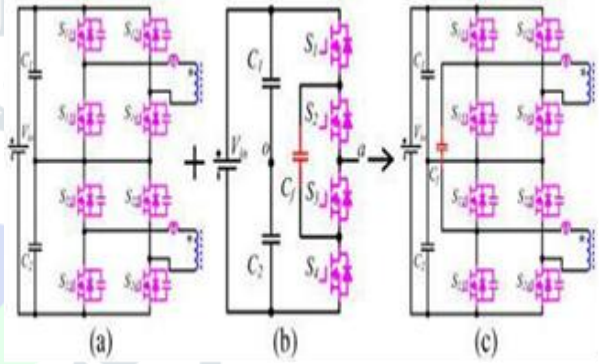


Fig.2. Derivation of the proposed modular multilevel dc/dc converter: (a) cascaded full-bridge converter, (b) flying capacitor-based TLC, and (c) proposed modular multilevel dc/dc topology.

lagging leg is shifted to regulate the output voltage. This indicates that the leading legs of the cascaded full-bridge converter can be assembled with the three-level flying capacitor-based converter to achieve the input voltage auto balance. And the lagging legs of the cascaded full bridge converter are still kept unchanged to provide adequate control freedom to achieve fast and accurate output voltage regulation. Consequently, for the proposed modular multilevel dc/dc converters, the big concern of the input-voltage imbalance existed in the ISOP converters is completely overcome due to the built-in flying capacitor. More importantly, the derived modular multilevel dc/dc concept can be easily put forward to N-stage converters by stacking the full-bridge power modules in series in the primary side to satisfy the growing bus voltage in the dc-based distribution and micro grid systems. In view of the phase-shift-controlled topologies, the aforementioned optimized strategies for the phase-shifted-controlled TLCs

can be directly transferred to the derived modular multilevel dc/dc converters to generate a family of high performance topologies for the high-voltage and high-power applications. It can be concluded that this modular multilevel converter concept is one of the general solutions for the high-voltage and high-power dc/dc topology origination

III. OPERATIONPRINCIPLE AND INPUTVOLTAGE AUTOBALANCE MECHANISM

For the secondary side of the derived modular multilevel dc/dc converters, the current-type full-wave rectifier, full-bridge rectifier, current doubler rectifier, and other advanced current-type rectifiers can be employed. In this section, the widely adopted current-type full-wave rectifier is applied as an example to explore the circuit performance of the proposed modular multilevel configuration, which is illustrated in Fig. 3. In the primary side, the capacitors C1and C2are used to split the high input voltage, S11−S14are the power switches of the top full-bridge module, S21−S24form the bottom full-bridge module,Cs11−Cs24are the parasiticcapacitors of the power switches, and Llk1and Llk2 are the leakage inductors of the transformersT1andT2, respectively.

In the secondary side, Do11,Do12,Lf1, and Co1 are for the top full-bridge module and Do21,Do22,Lf2, and Co2 are for the

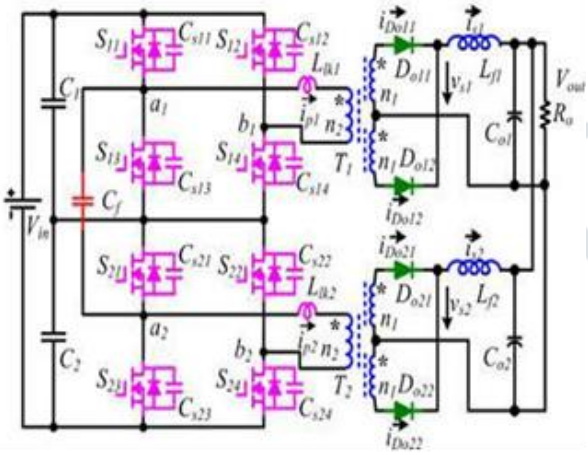


Fig.3. Proposed modular multilevel dc/dc converter with input voltage auto balance ability.

bottom full-bridge module. i_{p1},i_{p2},i_{Do11},i_{Do12},i_{Do21}, and $i_{Do22}$are the primary and secondary currents through the windings of the transformers with the defined direction in Fig. 3. And $i_{s1}$and i_{s2} are the filter inductors currents

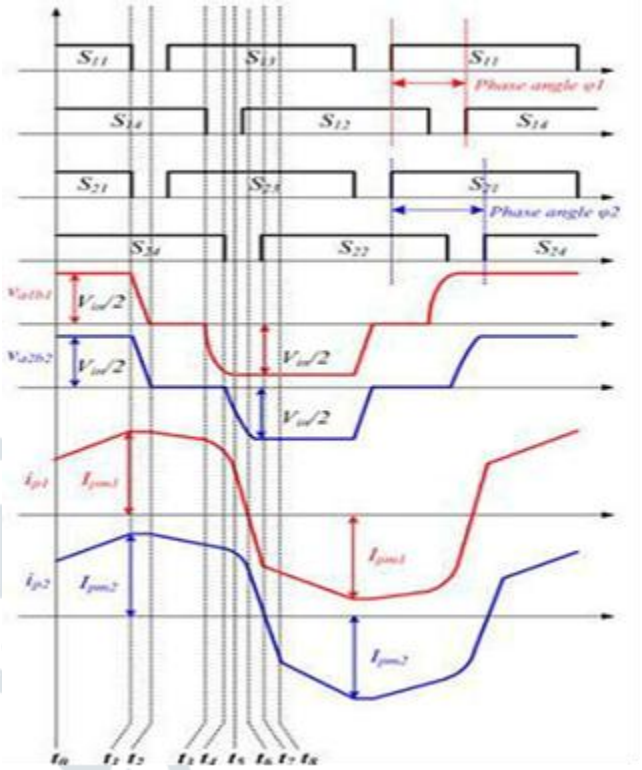


Fig.4. Key waveforms of the proposed converter.

A. Operation Analysis

The phase-shift control scheme is employed in the proposed converter to realize the ZVS performance of all the power switches, where S_{11},S_{13},S_{21}, and S_{23} are the leading-leg switches and S_{12},S_{14},S_{22}, and S_{24} are the lagging-leg switches. The key waveforms of the proposed converter are shown in Fig. 4. For the top full-bridge module,S_{11} andS_{13} act with 0.5 duty cycle complementarily with proper dead time td, so as for the switches S_{12} andS_{14}. The phase-shift angle between the leading and lagging switch pairs is defined as ϕ_1. The gate signal pattern of the bottom full-bridge module is similar to that of the top full-bridge module with the phase-shift angle ϕ_2. Meanwhile, the leading switches pair S_{11} andS_{13} turns ON and OFF simultaneously with the switch pair S_{21} andS_{23}, while the phase-shift angles ϕ_1 and ϕ_2 are decoupled control freedoms for the output voltage regulation. The mode 0 $<\phi_1-\phi_2<t_d$ is taken into consideration when analyzing the operation of the converter, and the equivalent operation circuits are depicted in Fig. 5. In order to simplify the analysis, the following assumptions are made: 1) all the power switches and diodes are ideal; 2) the parasitic capacitors$C_{s11}-C_{s24}$of the switches have the same value as Cs; 3) the voltage ripples on the divided input capacitorsC_1,C_2 and flying capacitors C_f are small due to their large capacitance; 4) the turns ratio of both transformers is N= n_2:n_1; and 5) the input voltage is balanced and the auto balance mechanism will be depicted later. There are 15 operation stages in one switching period. Due to the

symmetrical circuit structure and operation, only the first eight stages are analyzed as follows.

Stage1 [t_0,t_1]: Before t_1, the switches S_{11},S_{14},S_{21}, and S_{24}arein the turn-on state to deliver the power to the secondary side. The output diodesD_{o11} andD_{o21} are conducted and the output diodesD_{o12} andD_{o22} are reverse biased. The flying capacitor C_f is in parallel with the input divided capacitor C_1 to make V_{Cf} equal toV_{C1}.

$$i_{p1}(t) = i_{p1}(t_0) + \frac{V_{in}/2 - NV_{out}}{L_{lk1} + N^2 L_{f1}}(t - t_0) \quad (1)$$

$$i_{p2}(t) = i_{p2}(t_0) + \frac{V_{in}/2 - NV_{out}}{L_{lk2} + N^2 L_{f2}}(t - t_0) \quad (2)$$

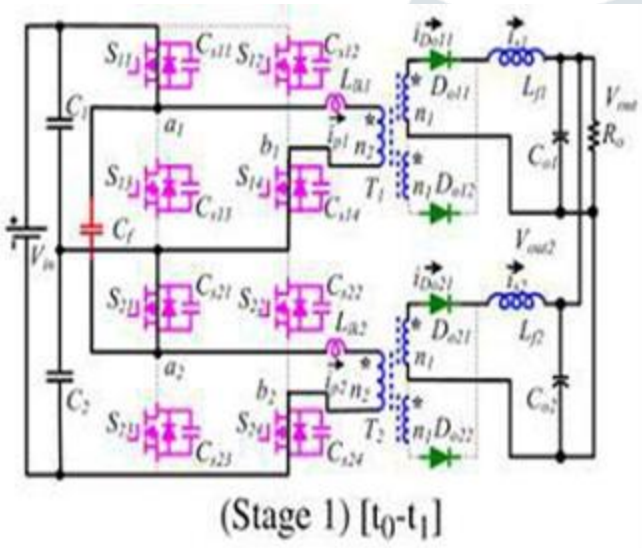


Fig.5.Stage 2 [t1,t2]:At t1, the turn-off signals of the switches S11and S 21are given. ZVS turn off for these two switches are achieved due tothe capacitors Cs11 andCs21. Cs11 andCs21 are charged andCs13 andCs23 are discharged by the primary currents.

$$i_{p1}(t) = \frac{i_{s1}(t)}{N} \quad (3)$$

$$i_{p2}(t) = \frac{i_{s2}(t)}{N} \quad (4)$$

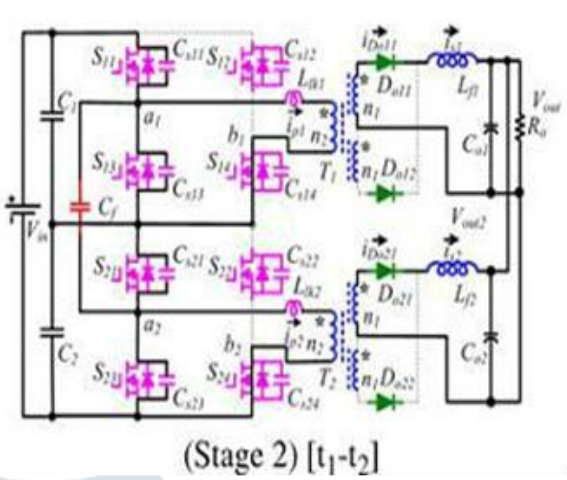


Fig.6.

Stage3[t2,t3]:At t2, the voltages of Cs13 andCs23 reach 0 and the body diodes ofS13andS23are conducted, providing then ZVS turn-on condition forS13andS23. The flying capacitor Cf is changed to be in parallel with the input divided capacitor C2. The primary currents are derived by

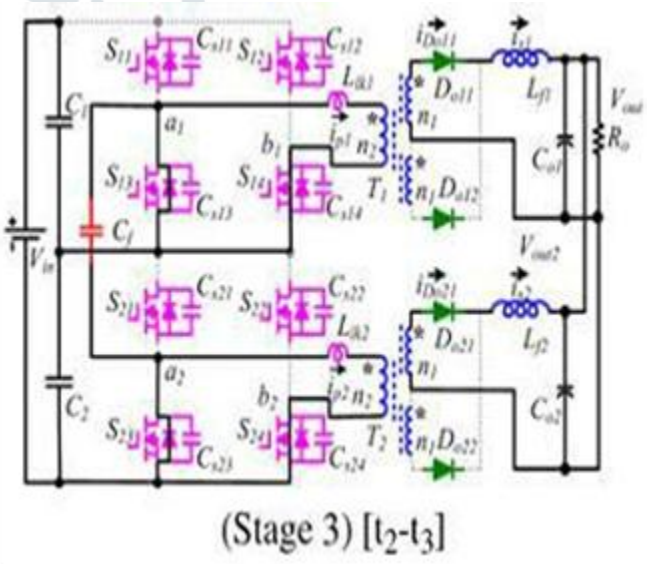


Fig.7.

Stage4[t3,t4]:At t3,S14turns off with ZVS.Cs14is charged andCs12 is discharged, leading to the forward bias of Do12;$i_{p1}$is regulated by

$$i_{p1}(t) = i_{p1}(t_3)\cos\omega(t - t_3)$$

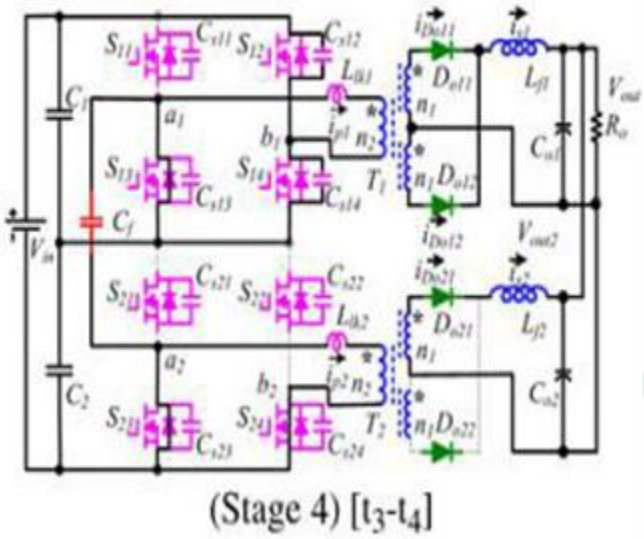
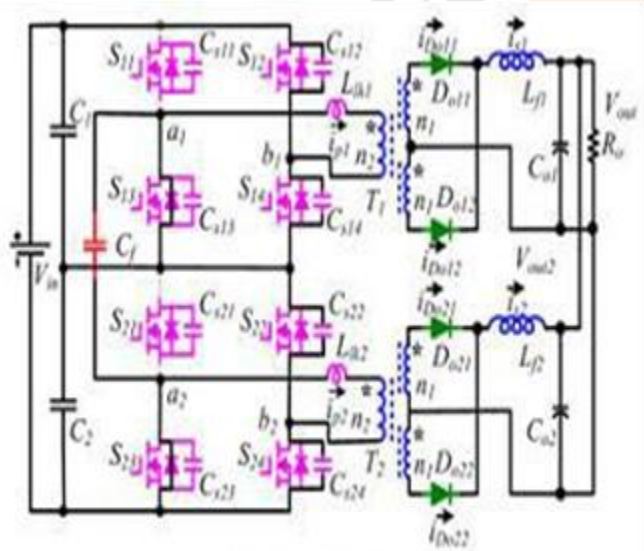


Fig.8.

Stage5 [t_4,t_5]: At t_4, the turn-off signal ofS_{24}comes. ZVS turn-off performance is achieved forS_{24}. Similar to the previous time interval, D_{o21} and D_{o22} conduct simultaneously, thus leading to the transformer T_2 short-circuit.$i_{p2}$is regulated by



$$i_{p2}(t) = i_{p2}(t_4)\cos\omega(t - t_4) \qquad (6)$$

Fig9:

Stage 6 [t_5,t_6]: Att_5,$C_{s12}$is discharged completely and the antiparallel diode of S_{12} conducts, getting ready for the ZVS Turn-on ofS_{12}. During this time interval, i_{p1} declines steeply duo to half-input voltage across the leakage inductorL_{lk1}. i_{p1} is given by

$$i_{p1}(t) = i_{p1}(t_5) - \frac{V_{in}/2}{L_{lk1}}(t - t_5) \qquad (7)$$

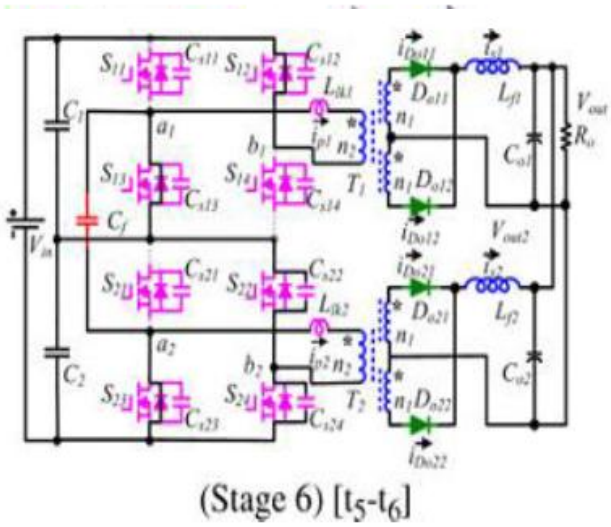


Fig 10:
Stage 7 [t6,t7]:At t6,ip1 decreases to 0 and increases reversely with the same slope throughS12 andS13. Cs22 is discharged completely and the anti parallel diode ofS22conducts. ip2 declines rapidly duo to half-input voltage across the leakage inductor Llk2.ip2is given by

$$i_{p2}(t) = i_{p2}(t_6) - \frac{V_{in}/2}{L_{lk2}}(t - t_6) \qquad (8)$$

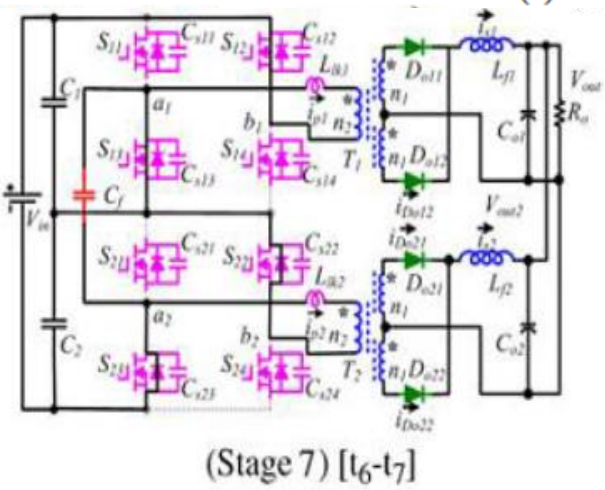


Fig.11:
Stage 8 [t7,t8]:At t7,ip2 decreases to 0 and increases reversely throughS22 andS23. The current through the output diodeDo11 decreases to 0 and turns off. The output diodeDo21 turns off aftert8, and then a similar operation works in the rest stages

B. Input Voltage Auto balance Mechanism

The input voltage imbalance is one of the major drawbacks for most multilevel converters and ISOP converters, which is mainly caused by the asymmetry of the component parameterdifference and the mismatch of control signals. It has been carried out that the transformer turns ratio difference (N), leakage inductance distinction (L_{lk}), and

phase-shift angle mismatch (φ) are the main reasons for the input voltage imbalance in the steady state for the ISOP phase-shift-controlled converters. The effect of these factors is summarized in Table I, which shows that $N_1 > N_2$ or $L_{lk1} > L_{lk2}$ or $\varphi_1 > \varphi_2$ leads to the voltage VC1on the top input capacitorC1higher than the voltageV_{C2}on the bottom capacitorC2and vice versa. As the parameter difference increases, the voltage gap betweenVC1andVC2increases correspondingly. The input voltage auto balance mechanism of the proposed modular multilevel dc/dc converter is displayed in Fig. 6 and detailed elaborated as follows. According to the steady operation of the proposed converter, for the leading-leg switches, the switchesS11andS21have the same time sequence and the switchesS13 andS23 are operated synchronously. WhenS_{11} andS_{21} are turned ON,S_{13}andS_{23} are turned OFF accordingly, and the flying capacitor Cf is connected in parallel with the top input capacitor C_1 as plotted in Fig. 12(a). This makes V_{cf}equal toV_{c1}. In the same way, as given in Fig. 12(b), the flying capacitor $C_f$is in parallel with the bottom input capacitor C_2, when$S_{13}$and $S_{23}$are in turn-on state. This denotes that V_{cf}andV_{c2} are the same. The connection of Cf with C_1 or C_2 alternates with high switching frequency, which leads to the voltages on both the input capacitors automatically shared and balanced. It is important to point out that the flying capacitor does not connect with the lagging-leg switches directly. As a result, the operation of $C_f$hardly affects the states of the lagging-leg switches. Then, both the two phase-shift anglesφ_1 and φ_2 can be taken as control freedoms to regulate the output voltage.

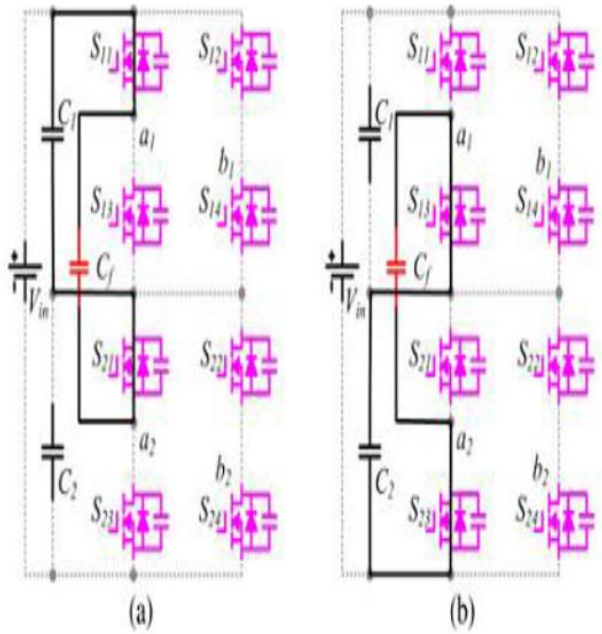


Fig.12. Input voltage auto balance mechanism: (a)Cf in parallel withC1 and(b) Cf in parallel withC2.

IV. CONVERTER PERFORMANCE ANALYSIS

A. Voltage Stresses of Switches

In the primary side, the voltage stress of the power switches S11−S24is half of the input voltage owing to the series structure and the auto balance mechanism. As a result, the low voltage-rated power devices are available in the high input applications to restrict the conduction losses.

B. ZVS Soft-Switching Condition

Leading Legs: ZVS turn-off is achieved for the leading switches due to their intrinsic capacitors. In order to realize ZVS turn-on, enough energy is needed to charge and discharge the intrinsic capacitors. During the dead time interval [t1−t2], S11 andS21 are turned OFF; Cs11 andCs21 are charged andCs13 andCs23 are discharged as shown in Fig. 13. According to the Kirchh offs law, the following equations are derived:

$$i_{Cs11} + i_{Cs13} = i_{p1} - i_{Cf} \quad (9)$$

$$i_{Cs21} + i_{Cs23} = i_{p2} + i_{Cf} \quad (10)$$

It is reasonable to assume that $i_{p1}$and i_{p2} are nearly constant during this period due to the short dead time. When the sum of VC_{s13} and VC_{s21} is not equal to V_{cf}, $C_f$may be charged or discharged. The current iCf affects the ZVS performance of the power switches according to (11) and (12): 1) when $C_f$is discharged, i_{cf}flows in the positive direction, and ZVS performance of S_{21} and S_{23} is improved but deteriorated for S_{11} andS_{13}; and 2) when $C_f$is charged, i_{cf}flows reversely, which improves the ZVS performance of S_{11} and S_{13}but deteriorates that of $S_{21}$and S_{23}. Fortunately, $C_f$is much larger than Cs, making i_{cf}small. Besides, the output filter inductance is reflected to the primary side and is in series with the resonant inductance. The energy of both the filter inductors and the resonant inductors is sufficient to achieve ZVS for the leading switches. The output filter inductance is so large enough that the leading switches can realize ZVS turn-on even at light loads.

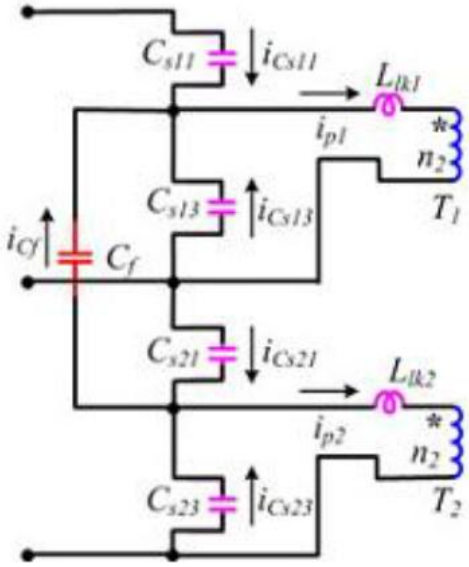


Fig.13. ZVS equivalent circuit of leading switches during dead time.

Lagging Legs: Similar with the leading switches, the lagging switches are able to realize ZVS turn-off by utilizing their intrinsic capacitors. However, only the energies of the resonant inductors are employed to achieve ZVS turn-on for the lagging switches. In order to accomplish ZVS

$$\frac{1}{2}L_{lk}\left(\frac{I_o}{N}\right)^2 > \frac{1}{2}\cdot 2C_s\left(\frac{1}{2}V_{\text{in}}\right)^2 = \frac{1}{4}C_sV_{\text{in}}^2 \quad \textbf{(11)}$$

As the resonant inductance is quite smaller than the filter inductance, the achievement of the ZVS turn-on for the lagging switches is more difficult than the leading switches at light loads.

C. Duty Cycle Loss

During interval [t3–t7], Va1b1 is negative, and ip1 transits from the positive direction to the negative reflected filter inductance current. The secondary diodes Do11 andDo12 conduct simultaneously, making the secondary rectified

$$D_{\text{loss1}} = \frac{2(t_7 - t_3)}{T_s} \approx \frac{8L_{lk1}I_{o1}}{NV_{\text{in}}}. \quad (12)$$

For the bottom full-bridge module, the duty cycle loss is similar to the top full-bridge module as given by

$$D_{\text{loss2}} = \frac{2(t_8 - t_4)}{T_s} \approx \frac{8L_{lk2}I_{o2}}{NV_{\text{in}}} \quad (13)$$

V. SIMULATION RESULTS

Simulation results of this paper is shown in bellow Figs.14 to 20

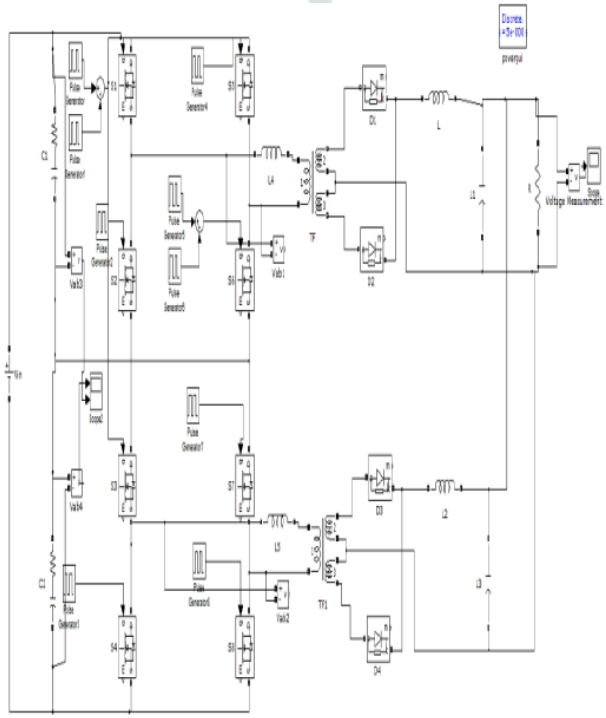


Fig.14. Matlab/Simulink circuit of proposed system without flying capacitor.

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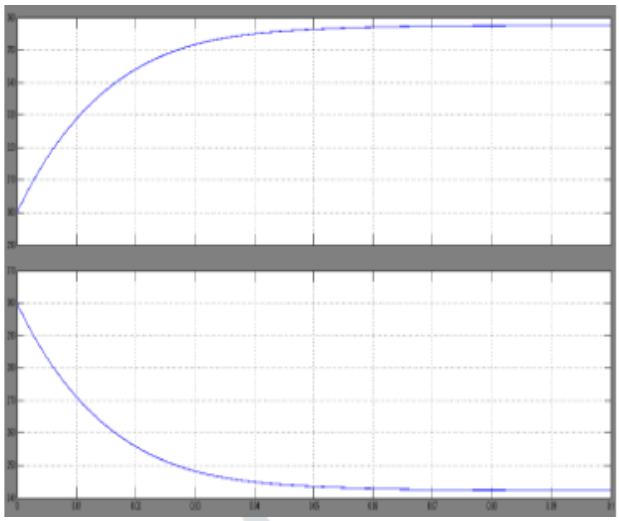

Fig.15.simulation waveform of proposed system input voltage without flying capacitor.

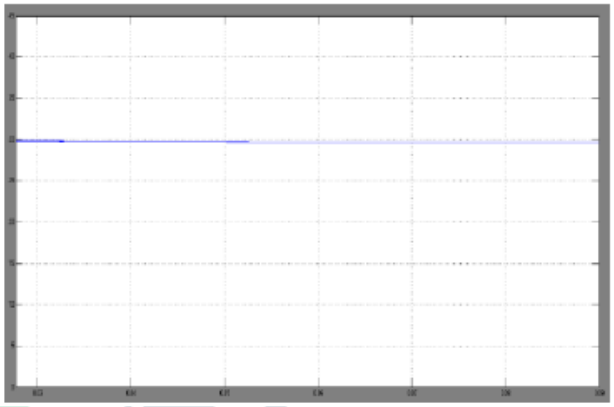

Fig.16. simulation waveform of proposed system output voltage without flying capacitor.

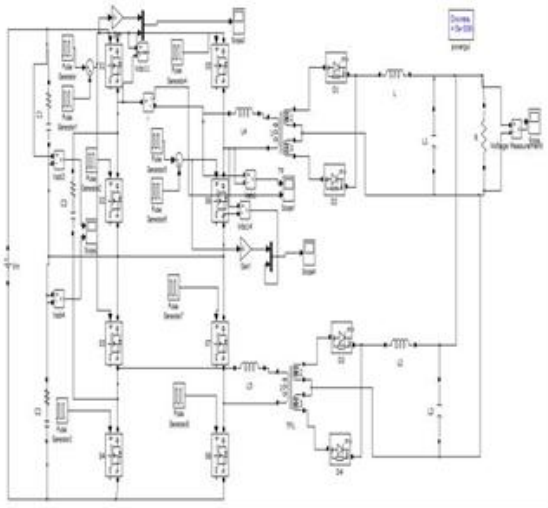

Fig.17.Matlab/Simulink circuit of proposed system with flying capacitor.

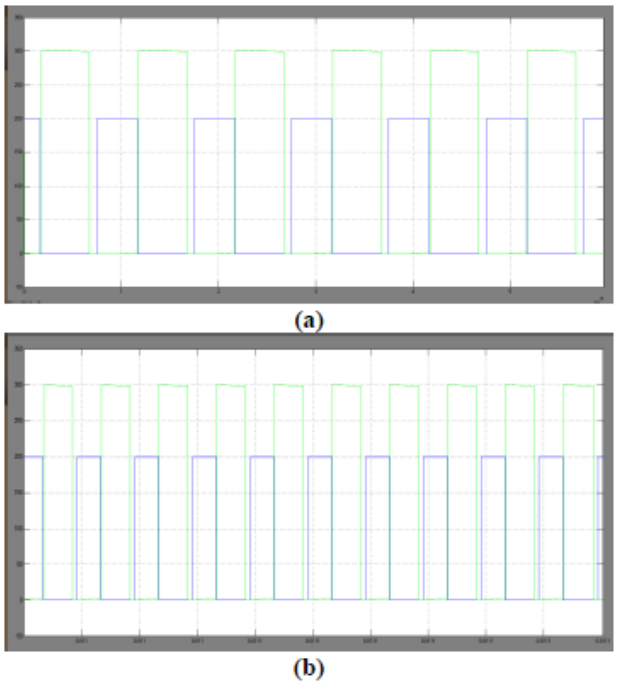

Fig.18. Simulation results of ZVS operation: (a) ZVS operation for S11 and (b) ZVS operation for S14 .

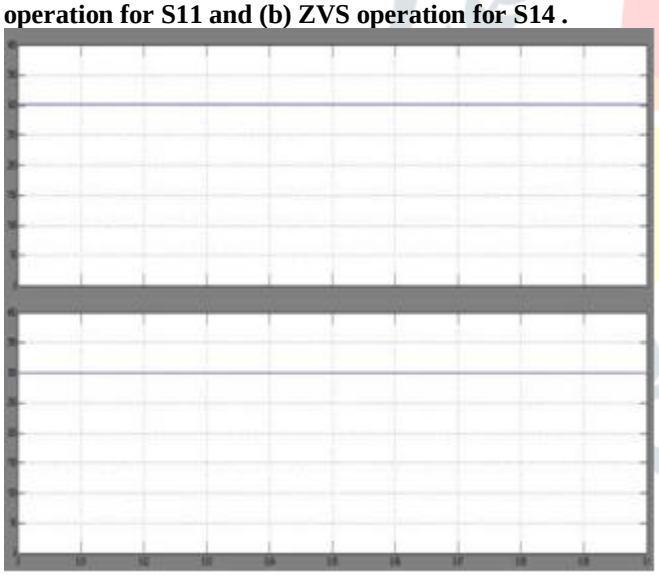

Fig.20.simulation waveform of proposed system input voltage with flying capacitor.

VI. CONCLUSION

In this paper, proposed modular multi-level converter dc/dc converter is analyzed for the high step down and high power dc based systems, by integrating the full bridge converters and three-level flying capacitor. The presence of inherent capacitors automatically shared the input voltage and balanced without any power components and control loops. Hence it is cost effective By the input voltage balance reduces the voltage stress. By this zero voltage switching performance can be ensured hence switching losses can be decreased. The MMC can be developed for N-stages to achiechve for better performance.

VII. REFERENCES

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