Analysis Of A Pspice Simulation Model of QFGMOS

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ABSTRACT:

This paper has been devoted to the study of quantitative analysis of a PSpice simulation model of Quasi floating-gate MOSFET.

Keywords: Quasi floating-gate MOSFET, Floating-gate MOSFETs, PSpice simulation model.

1. INTRODUCTION:

The Floating-gate MOSFETs (FGMOS) have been used extensively for low voltage analog applications due to the unique feature of reducing the effective threshold voltage from its conventional value with the application of bias voltage (S. Sharma [8]). This voltage is applied by a large capacitance to one of its multiple-input terminals while other input for signal application. However, the large capacitance requirement for threshold voltage programmability increases the need for silicon area, reducing the effective transconductance and gain-bandwidth (GB) product in addition to reducing the frequency response of the resulting circuit (S. Sharma [8]). Moreover, the Floating-gate MOSFETs structure has a tendency to trap a significant amount of charge during the fabrication process which can lead to DC offset problems. Such drawbacks of Floating-gate MOSFETs (FGMOS) based structures are overcome with minor modifications in its structure resulting in a new device known as Quasi floating gate MOSFET (QFGMOS) (J. R. Angulo [6]). This new device for low voltage analog circuits was introduced by Carlos Urquidi [1]. Several ways have been proposed to implement the required QIRs (I. Seo [4]).

The equivalent circuit of the *N*-input N-type Quasi floating-gate MOSFET is shown in Fig.(1). The structure of Quasi floating-gate MOSFET is very similar to that of Floating-gate MOSFETs where the signal inputs are also capacitively connected to the floating gate. In QFGMOS we do not need large biasing capacitors for threshold voltage tuning required in FGMOS. Instead, we connect the floating gate to any of the supply rails through a very large resistance. For practical purposes, the Quasi floating-gate (QFG) of an NMOS transistor is tied to V_{DD} via a reverse-biased diode-connected PMOS transistor that acts as a large value resistor while the Quasi floating-gate (QFG) of a PMOS transistor is tied to V_{SS}.

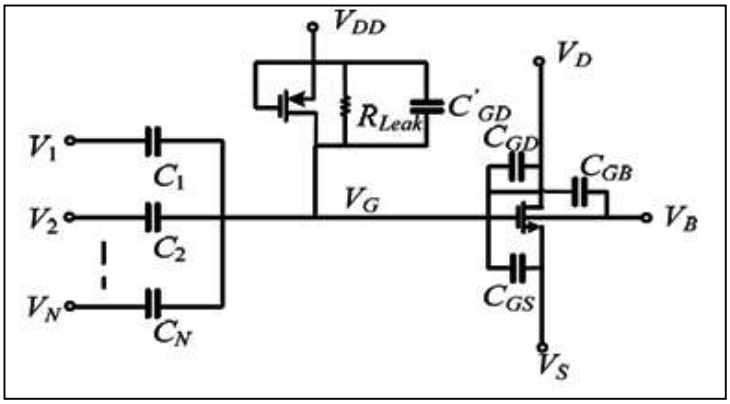

Figure 1: Equivalent circuit of QFGMOS

A reverse-biased diode-connected NMOS transistor (J. R. Angulo [5]). This pull-up (pull-down) resistor sets the DC voltage on the Quasi floating-gate (QFG) to either power rail, thus, eliminating the problem due to accumulated charge on the floating gate during the manufacturing process and also reducing the supply voltage requirements. Moreover, the use of larger resistances effectively floats the Quasi floating-gate for low frequency signals, thus, does not affect AC operation for signals in this frequency range. Moreover, the limitations of Floating-gate MOSFETs (FGMOS) are overcome as there is no need for larger biasing capacitors resulting in smaller chip area and better frequency response (J. R. Angulo) [6].

2. PSpice Simulation Model:

Circuit simulators such as PSpice can also be used to verify the behavior of Quasi floating-gate MOSFET (QFGMOS) structures. The PSpice simulation model of Quasi floating-gate MOSFET (QFGMOS) can be obtained by including some electrical components in the standard MOS model as was done for FGMOS in order to simulate Quasi floating-gate MOSFET (QFGMOS) behavior. The equivalent circuit of a Quasi floating-gate MOSFET (QFGMOS) is a number of capacitors placed between its different terminals, as shown in Fig. 1. All these capacitors need to be bypassed by very high value resistors to avoid the problem of floating nodes during simulation. The values of resistors and capacitors are chosen in such a way that the respective time constants become equal [2], [3], [7]. Now, the final model of a multi-input Quasi floating-gate MOSFET (QFGMOS) suitable for PSpice simulation is shown in Fig. 2.

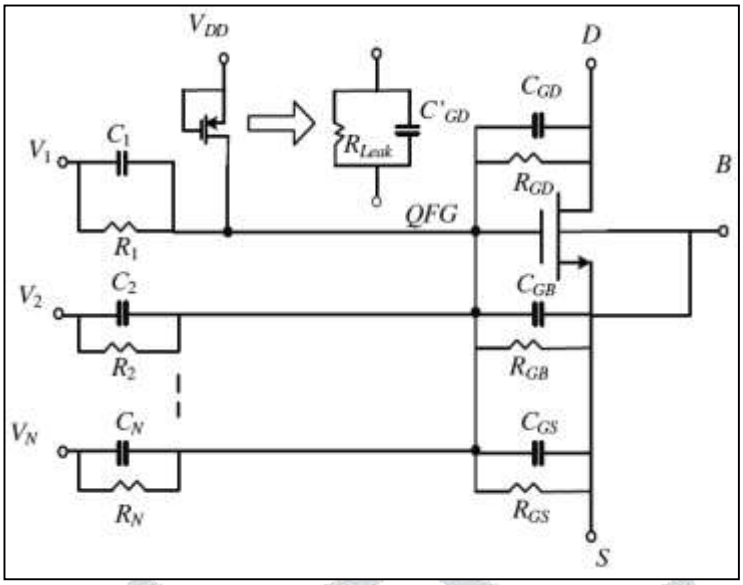

Figure 2: Model of multi-input QFGMOS

The simulation model of Quasi floating-gate MOSFET (QFGMOS) of Fig. 2 has been used to simulate the characteristics of Quasi floating-gate MOSFET (QFGMOS) transistor shown in Fig. 3.

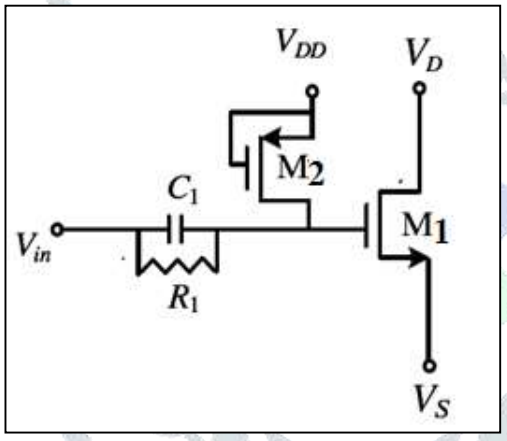

Figure 3: QFGMOS transistor

For simulation of characteristics, we have taken C_1 = 0.1 pF, R_1 = 200 MΩ, and *W/L* of M_1 = 39 µm/0.13 µm and *W/L* of M_2 = 1.3 µm/0.13 µm at supply voltage of ± 0.5 V.

The drain characteristics of Quasi floating-gate MOSFET (QFGMOS) for different values of input signal are shown in Fig.4.The output resistance of Quasi floating-gate MOSFET (QFGMOS) varies from 0.5 kΩ at V_{in} of 0.5 V to 11 kΩ at V_{in} of -0.1 V.

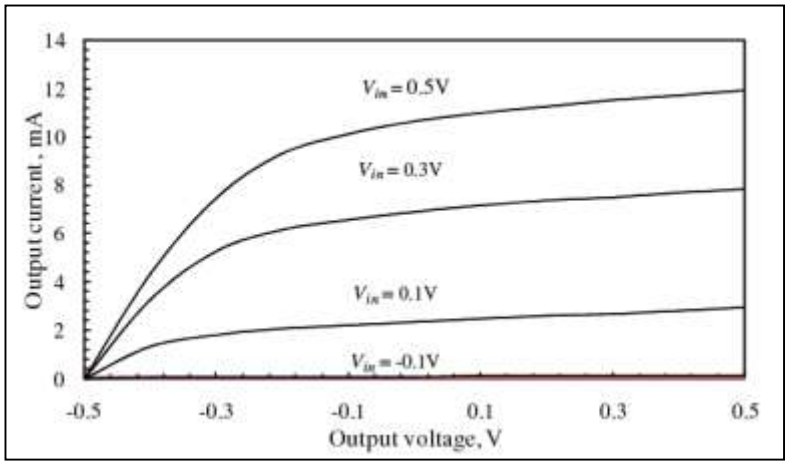

Figure.4: Drain characteristics of QFGMOS

The comparative transfer characteristics of Quasi floating-gate MOSFET (QFGMOS), Floating-gate MOSFETs (FGMOS) and conventional MOS are shown in Fig.5.

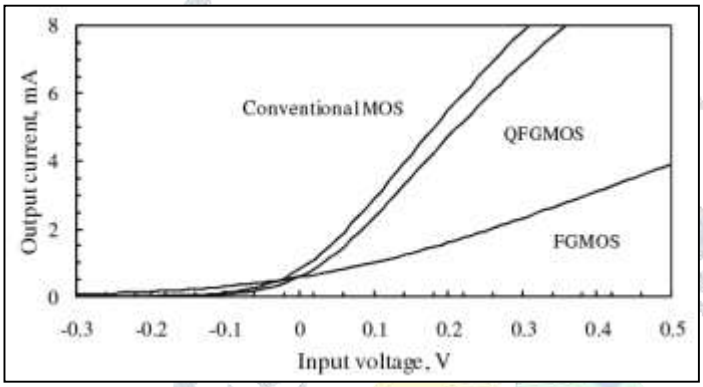

Figure 5: Transfer characteristics of QFGMOS

As evident from the figure, the threshold voltage in a QFGMOS transistor is less than the threshold voltage of conventional MOSFET. It is because of the fact that at same value of input voltage say 400 mV Quasi floating-gate MOSFET (QFGMOS) conducts more current (109 μA) as compared to conventional MOS (106 μA). Further, the threshold voltage of Quasi floating-gate MOSFET (QFGMOS) transistor is more than the threshold voltage of Floating-gate MOSFETs (FGMOS) because of the presence of bias voltage (V_{bias}) the gate of Floating-gate MOSFETs (FGMOS).

3. CONCLUSION:

In this paper, the PSpice simulation model of Quasi floating-gate MOSFET (QFGMOS) is presented to simulate the drain characteristics of Quasi floating-gate MOSFET (QFGMOS) which are obtained to be similar to the drain characteristics of conventional MOSFET and Floating-gate MOSFETs (FGMOS). The transfer characteristics of Quasi floating-gate MOSFET (QFGMOS) are also compared with that of conventional MOSFET and Floating-gate MOSFETs (FGMOS). It is found that the threshold voltage in a (QFGMOS) transistor is less than the threshold voltage of conventional MOS but more than the threshold voltage in Floating-gate MOSFETs (FGMOS).

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