Parallel-Connected Five-Level PWM Inverters

J.Sridevi, Associate Professor, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad
P.Praveen Kumar, PG Student, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad

***Abstract*—Multilevel PWM inverters have significant ad- vanta over the conventional one because of the capability of operating the mo with nearly sinusoidal current waveforms and higher output voltages order to increase the power rating of the inverter, connection in para would be effective in the present case. In high-power applications, instance, the carriers should be synchronized to the modulating sinuso waves. Moreover, for the interphase reactor, lower order harmo application is pro- hibited. In practice, to improve the harmo characteristics of the parallel-connected five-level inverter, modulation strategies have been devised and designed in this paper. found that the dc current flow through the dc power supplies can controlled by means of phase shifting of the injected third or harmonics. In the case of a static var compensator (SVC),the out capacitor voltages can be controlled by means of this technique.**

***Index Terms*—Five-level, harmonic injection, multilevel, par- alle connection, PWM inverter.**

I. Introduction

Multilevel pwm inverters, including five-level ones, have significant advantages over conventional one because of the capability of operating the motor with nearly si- nusoidal current waveforms and higher output voltages. Con- sequently, interest in actual applications is increasing. In dis- cussing practical applications, still larger capacity inverters are also anticipated, such as those for large ac motor drives. In order to increase the capacity of an inverter, connection in parallel is an effective method at present [1]. In general, a multilevel in- verter could also be obtained by connecting the inverters in par- allel with different phases for the carriers, and certain techniques and control methods should be considered when doing this. In high-power applications for instance, the carriers should be syn- chronized to the modulating sinusoidal waves. In addition, each three phase waveform should be built in a quarter-wave sym- metry as well as a half-wave symmetry. Moreover, for the inter- phase reactor, lower order harmonic application is prohibited. So far, various PWM techniques have been studied and many pa- pers have been published. In general, these can be classified into two types: One uses sine-triangular PWM schemes and the other uses space vector PWM ones. It is said that the latter is often preferred due to its simplicity both in hardware and software[2]. However, in the case of connection in parallel discussed in this paper, the current equilibrium between two legs of the inverter should be preserved. It is well known that in the case of para llel connection, both currents can readily be kept balanced by two sine-triangular PWM's that are shifted by 180 degrees to each other [3].

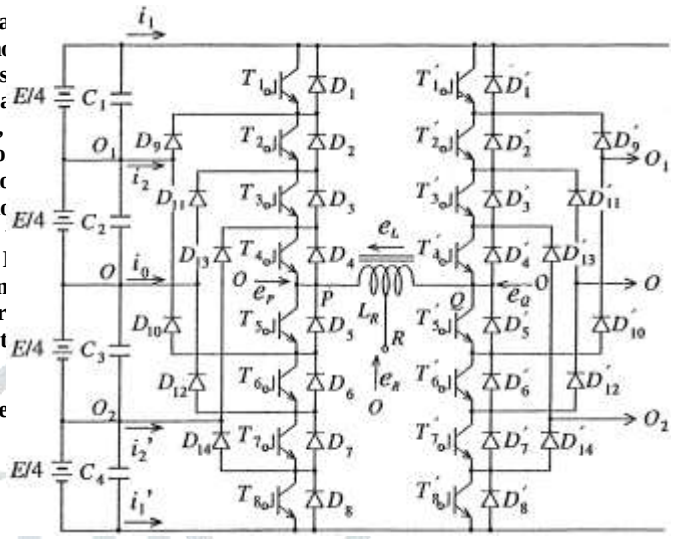


Fig. 1. Circuit configuration of five-level inverters in parallel.

This scheme can easily be realized by the con- ventional sine-triangular PWM scheme. For these reasons and because of its simplicity, this paper will be discussed with the sine-triangular PWM scheme. To improve the harmonic char- acteristic of three phase multilevel inverters, a few modulation strategies have been designed and are discussed.

II. Circuit Configuration

Fig. 1 shows one phase of a multilevel PWM inverter cir- cuit configuration with five-level inverters connected in parallel. IGBT's T_1 to T_8 are the main switches of phase u in the power circuit. D_1 to D_8 and D_1' to D_8' are the conventional feed- back diodes. D_9, D_{14} and D_9' D_{14}' are the clamp diodes. T_{iu} is the interphase reactor for each current. The input power supply is divided into four supply voltages with capacitors C_1 to C_4. Each voltage is a quarter of the total input voltage. In this in- verter system, the inside power supplies with capacitors C_2 or C_3 should also supply active power if the load is a conventional ac motor and the like. In such a case, the input dc supply can not be simply divided by the capacitors alone. In this situation, the input power is provided by four independent dc power supplies.

Fig. 2 shows the waveforms of the first modulation strategy for the nine-level PWM inverter discussed in this paper. Because of its simplicity, this modulation is mentioned first. This figure is for a symmetrical modulation, where each carrier waveform has symmetry with respect to the zero axis, and so it is termed a symmetrical modulation. The carriers e_{cr1}, e_{cr2}, e_{cr3} and e_{cr4}

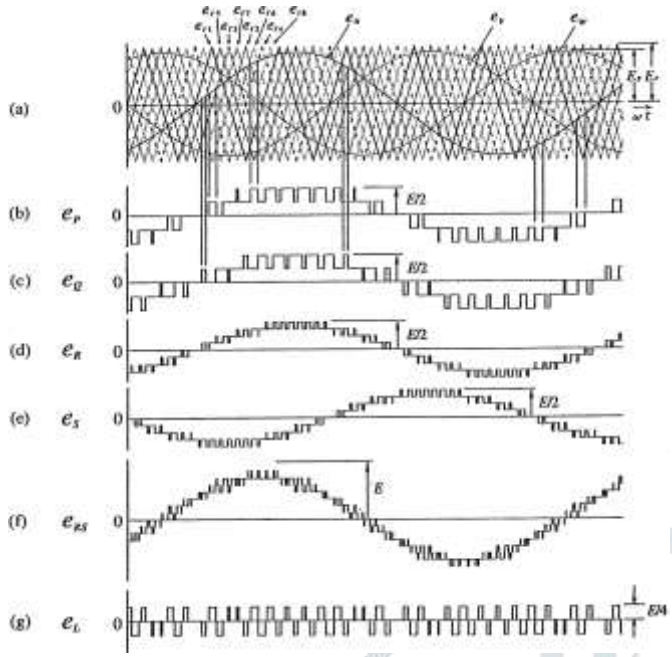


Fig. 2. Waveforms for symmetrical modulation.

shown with heavy lines, are used for the left-side arm which are displaced by $\pi/2$ or π radians from each other. The other carriers e_{r5} to e_{r8} shown with light lines are used for the right side arm. By comparing the voltage levels of each carrier with the sinusoidal reference wave e_m, we can obtain the output terminal voltage e_y as shown in Fig. 2(b) Thus

when $e_m \geq e_{rk}$, e_{rl}, e_{rm} and e_{rn},
T to T4 turn-on $e_y = E/2$,
when $e_{rk} \geq e_m \geq e_{rl}$, e_{rm} and e_{rn},
T3 to T turn-on $e_y = E/4$,
when e_{rk} and $e_{rl} \geq e_m \geq e_{rm}$ and e_{rn},
T1 to T8 turn-on $e_y = 0$,
when e_{rk}, e_{rl} and $e_{rm} \geq e_m \geq e_{rn}$,
T4 to T3 turn-on $e_y = -E/4$,
and when e_{rk}, e_{rl}, e_{rm} and $e_{rn} \geq e_m$,
T to T5 turn-on $e_y = -E/2$,
where k, l, m or n represent an arbitrary number among the subscripts r_1 to r_4 of the four carriers e_{r1} to e_{r4}. (1)

For the right-side arm carriers, a similar procedure is executed. The resultant pole voltage waveform at the terminal N is given by Fig. 2(c). Since both terminal waveforms e_P and e_Q are formed from the same sinusoidal reference signal, each fundamental component has the same voltage value. By means of the interphase reactors, the mean value between the terminal voltages e_P and e_Q can be given as e_R. Accordingly, the voltage e_R becomes a nine-level voltage and the magnitude is

$$e_R = (e_P + e_Q)/2. \quad (2)$$

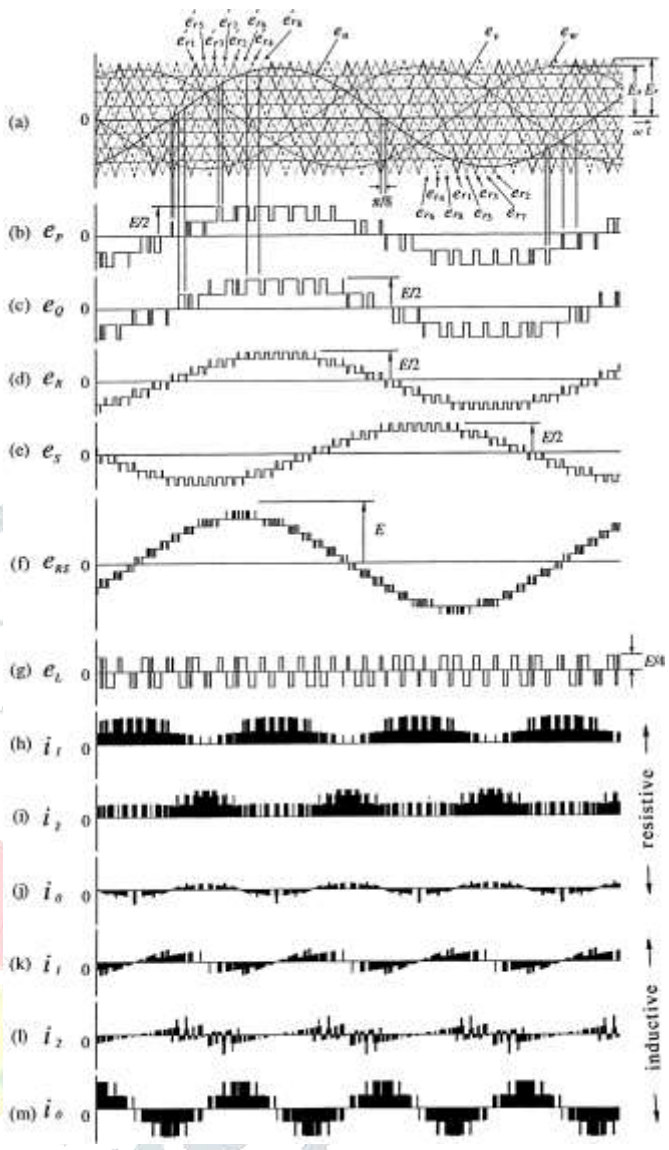


Fig. 3. Waveforms for multilevel modulation, (h) to (j) with resistive load, and (k) to (m), with inductive load.

III. Application of Multi-Level Carriers

For the above symmetrical modulation, some harmonic components are left as described later. Recently, the multilevel carrier method has been presented for multilevel inverters [4]–[6]. To improve the harmonic characteristics, a five-level inverter could be modulated by a multilevel carrier technique such as four-level carrier modulation. For our parallel connection, on the other hand, a specific technique has been devised and designed, so that the apparent carrier can be increased to eight levels. In this section, some techniques for devising and designing the carriers will be presented.

Fig. 3 shows various waveforms with the multilevel carrier discussed in this paper. In order to make each arm current balanced, sets of e_{r1} to e_{r4} and e_{r5} to e_{r8} should be displaced by $\pi/4$ radian to keep the symmetry of the carrier as described above. In addition, in order to effectively reduce the harmonics, multilevel carrier strategies need to be introduced, where the carriers are displaced by $\pi/8$ between two sets of carriers as

shown in Fig. 3(a). The fundamental principle of the multilevel carrier is the same as in the literature [4]–[6]. Consequently, for $3E_r/4 \geq e_m \geq E_r/2$, $E_r/4 \geq e_m \geq 0$, $-E_r/4 \geq e_m \geq -E_r/2$ and $-3E_r/4 \geq e_m \geq -E_r$, e_{cr1} to e_{cr4} are used for the arm of terminal P, while to e_{cr8} are for ter- minal Q. For the other levels, e_{cr1}' to are used, which are

displaced by $\pi/8$ radian relative to e_{cr1} through to e_{cr8}, respectively, where e_{cr1}' to e_{cr4}' are used for arm P and e_{cr5}' to e_{cr8}' are used for arm Q. In this case, the frequency ratio is given by $f_c/f_s = 5.625$, that is, a fractional ratio. In order that the output waveforms have quarter-wave and half-wave symmetries, this fractional ratio should be used for the multilevel carrier. The reason for this will be further explained in the next section. In Fig. 3(b) and 3(c), the waveforms obtained are not symmetrical, but the resultant waveforms in Fig. 3(d) and 3(e) become symmetrical waveforms. The actual waveform across the lines in Fig. 3(f) becomes an ideal waveform that varies by two voltage levels in a limited period.

IV. Harmonic Characteristics

The output PWM waveforms discussed in this paper are composed of many voltage levels and are thus complicated. Consequently, for harmonic analysis, there is some uncertainty in the analysis of such waveforms. Particularly in the case of multilevel modulation, as the waveform becomes more complicated, the physical meaning becomes difficult to interpret. Therefore, in this chapter, we will analyze analytically only the symmetrical modulation. For over-modulation or multilevel modulation, harmonic components will be presented only from the simulation results. As the detailed analytical methods have already been reported [3], [7], we will present only the procedure and results of the analysis.

First, the output voltage of a three-level inverter is analytically resolved [3]. In the next step, by means of displacing the phase of the carriers by π radians, another analytical result can be obtained. Hence, the mean value of the two analytical results is calculated. This voltage waveform becomes the same as that of the five-level inverter. Similarly, another output voltage waveform with another carrier can be analytically obtained. These waveforms have previously been presented in detail [3], [7]. In this way, the nine-level output waveform in a parallel connection can also be analyzed. Consequently, the magnitudes of the harmonic components are given in Table I. The magnitude of the ω_s component is identical for each inverter. As shown in Table I, an increase in the number of output voltage levels can be realized by paralleling the previous stage inverters with a different phase of the carriers. When connected in parallel as just described, if the conventional three-level inverter is taken as a unit inverter, the magnitude of the $2mn\omega_c \pm (2k+1)\omega_s$ component can be expressed in general as shown in the lowest line in the Table. The modulation index is defined by $a = E_s/E_c$, where E_s is the amplitude of the sinusoidal reference wave and E_c is the amplitude of the triangular carrier wave as shown in Fig. 2(a).

Fig. 4 shows the relationship between the amplitudes of the harmonics and the voltage modulation index a calculated from the corresponding equation in Table I in the region of $a \leq 1.0$.

TABLE I
Dominant Harmonic Components

		Harmonic order	magnitudes
	fundamental frequency	ω_s	$\sqrt{3}aE/2$
inverter types	three level	$2n\omega_c \pm (2k+1)\omega_s$	$(\sqrt{3}E/n\pi)J_{2k+1}(n\pi a)$
	five level	$4n\omega_c \pm (2k+1)\omega_s$	$(\sqrt{3}E/2n\pi)J_{2k+1}(2n\pi a)$
	nine level	$8n\omega_c \pm (2k+1)\omega_s$	$(\sqrt{3}E/4n\pi)J_{2k+1}(4n\pi a)$
	$2m+1$ level	$2mn\omega_c \pm (2k+1)\omega_s$	$(\sqrt{3}E/mn\pi)J_{2k+1}(mn\pi a)$

where $n = 1,2,3,\ldots$ $k = 2k'$, $2k'+2,\ldots$ $k' = 0,1,2,\ldots$
ω_s is the angular frequency of the fundamental wave,
ω_c is the angular frequency of the carrier, $a = E_s/E_c$,
m is the number of inverter is parallel and J_n represents the Bessel function.

It is shown that the lower order harmonic components are eliminated by increasing the level, but the higher order components are left as they are. In Fig.4 (a) for the conventional two-level inverter, the theoretical results are shown in [3]. The reduced components, below a few percent, are not shown in the figure. As can be seen, a multilevel inverter can be obtained by paralleling the previous stage inverters. Namely, a nine-level inverter can be obtained by paralleling the five-level ones, which are derived from the three-level ones, and so forth.

Fig. 5 shows the relationship between the amplitudes of the harmonics and the voltage modulation index for multilevel modulation. The experimental parameters such as carrier frequency, modulation index etc. are identical with those in Fig. 3. The harmonic components are well suppressed over the whole region. The frequency ratio is given by $f_c/f_s = 5.625$. The reason for this can be explained as follows. The triangular carrier waves are shifted by $\pi/8$ radians to the lower or upper stage carriers as shown in Fig. 3(a) Consequently, the sum of the phases of triangular waves over one cycle of the fundamental wave becomes $n\pi + \pi/8 + \pi/8 = 2\pi \times (n/2 + 0.125) = 2\pi(f_c/f_s)$, where n is the natural number. As mentioned above, to obtain waveforms with symmetry between the positive and the negative, the frequency ratio of the carrier wave to the sinusoidal wave should be selected in such a way to be fractional. In addition, in order to make a symmetrical waveform in three phases, the ratio, $n/2 + 0.125$ should be exactly divided by three. For instance, with $n = 11$, $f_c/f_s = 5.625$, and the theory is established. The effective carrier frequency f_c' in each stage can be represented by eight times the reference carrier frequency. Consequently, the frequency ratio becomes an integer number as follows: $f_c'/f_s = 8f_c/f_s = 8 \times 5.625 = 45$. For symmetrical modulation, the effective carrier ratio is $f_c'/f_s = 48$, the procedure for which can be explained in the same way.

At the sidebands at around eight times the carrier frequency, one can see that if the frequency ratio f_c/f_s is given by an integer, the harmonic order becomes an even number. However, if the ratio of f_c/f_s is given by a fraction as shown, the harmonic order becomes an odd number resulting in a symmetrical wave, where the experimental results are plotted using circles, etc. Fig. 6 shows the relationship between the distortion

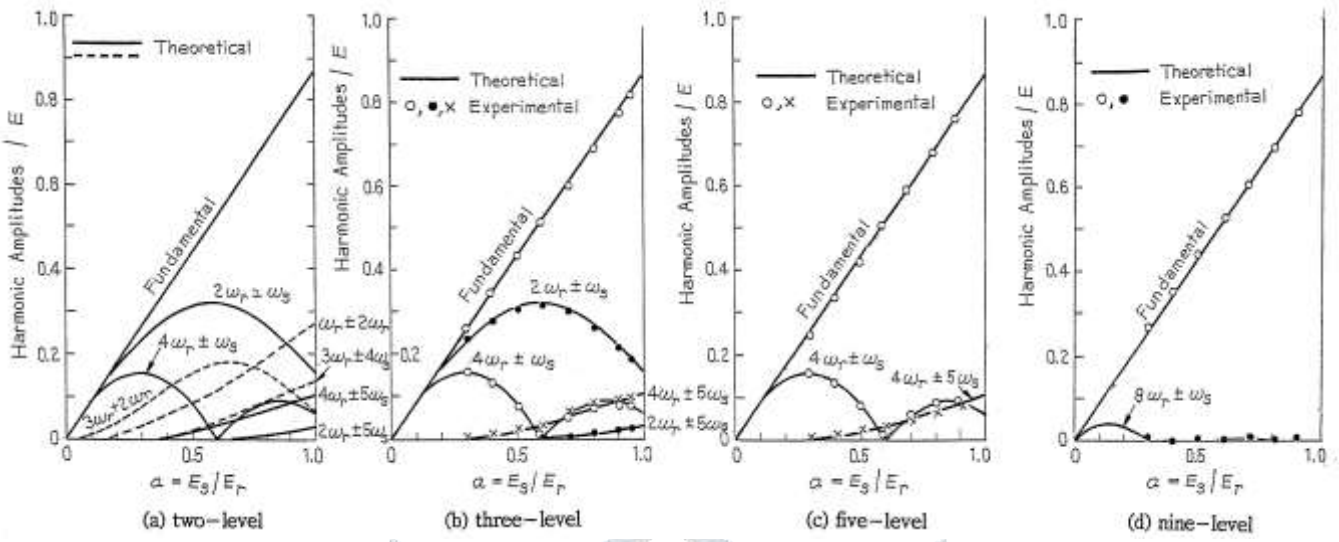


Fig. 4. Harmonic components for various level inverters.

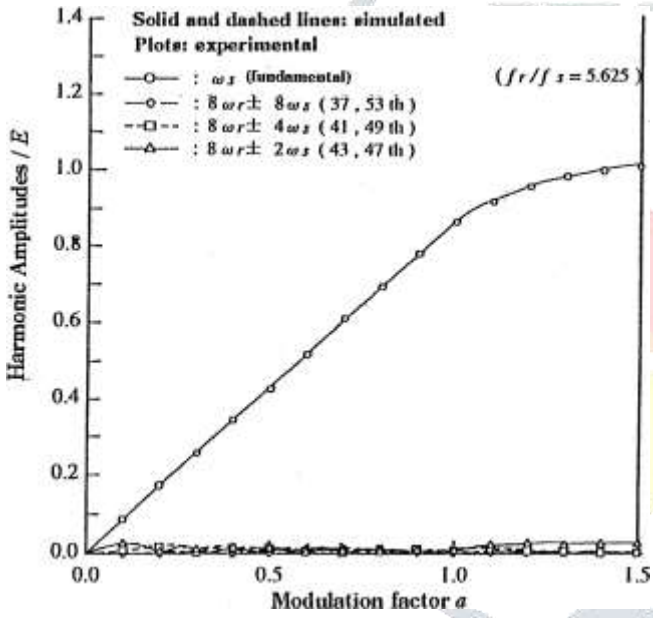


Fig. 5. Harmonic components of output voltage.

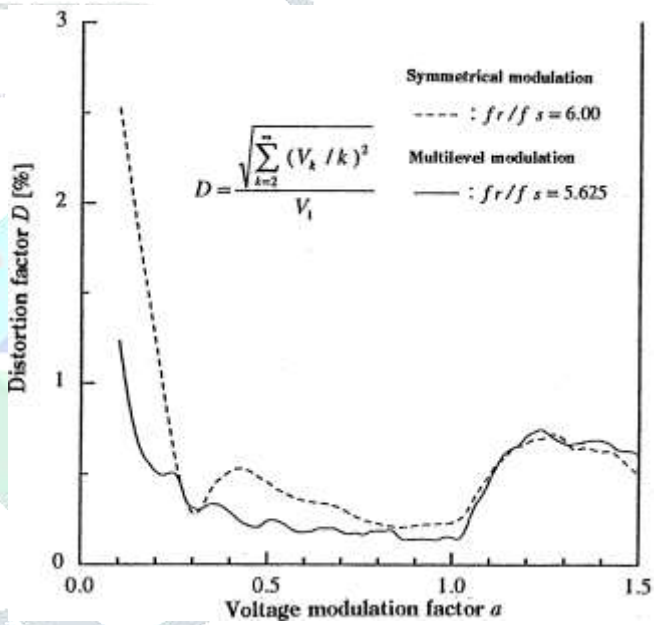


Fig. 6. Modulation factor versus distortion factor.

factors calculated from the simulation results. The definition of this is indicated in the figure [13]. Except for the regions near $m = 0.3$, and $m \geq 1.0$, where the results are almost equal, the distortion factors for multilevel modulation are improved compared with symmetrical modulation. In the over modulation region of $m \geq 1.0$, the lower order harmonic components that do not exist in the normal modulation region of $m \leq 1.0$, cause the distortion factor to deteriorate.

V. Discussions on Capacitor Voltage Control

The purpose of this chapter is to discuss the possibility of capacitor voltage control if the input power supplies are replaced by capacitors such as SVCs. In this case, it is well known that for a three-level inverter, the input power supply can be divided by two capacitors because the voltages keep their balance against the disturbances. Consequently, it is unnecessary to control the capacitor voltage if a quick response is not required. In conventional five-level inverters, however, as mentioned above, since four input power supplies deliver the active power, the input power supply can not be divided just by capacitors like the three-level inverter. For a SVC supplying the reactive power only, however, division of the power supply by capacitors is quite within the bounds of possibility. For the case in which a five-level inverter is applied to a SVC, the input power supply could be divided into four capacitors. In such a case, however, it would be necessary to control the voltages. It is evident that the voltages can be regulated by the dc current flowing through each capacitor. In order to examine the possibility of capacitor voltage control for the SVC circuit, the third order harmonic injection method is presented below.

Fig. 7 shows the average direct current of each input power supply due to third order harmonic injection, which is injected

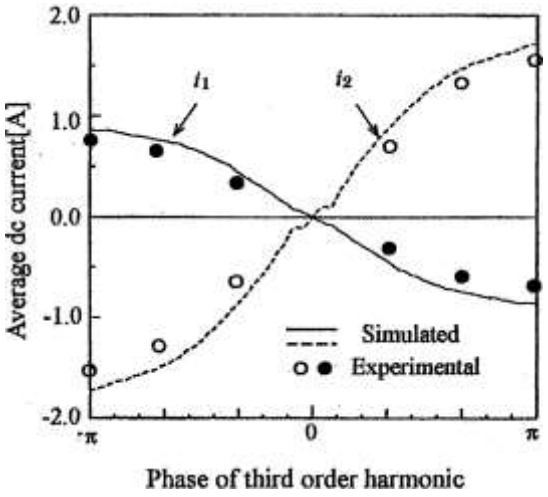
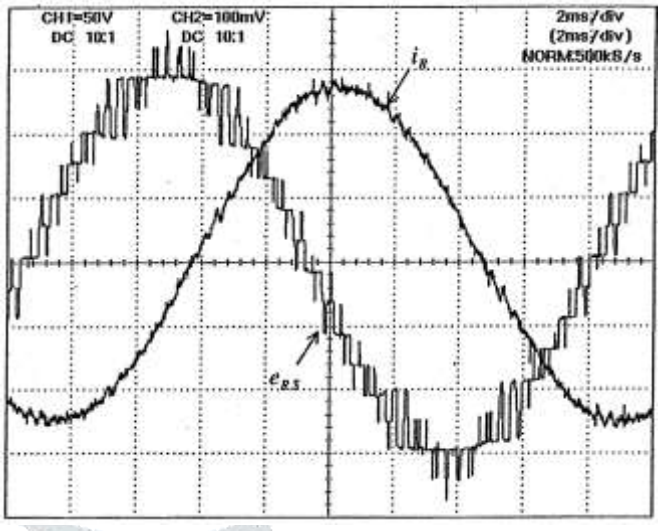
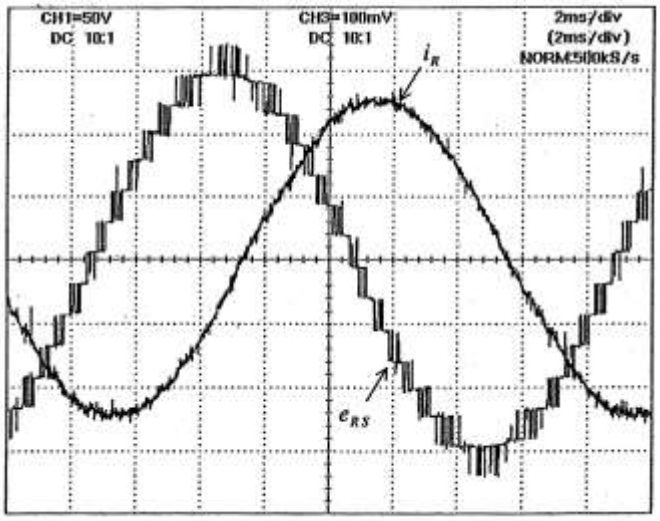


Fig. 7. Capacitor current variation due to third order harmonic injection.



(a)



(b)

Fig. 8. Output line voltage waveforms e_{RS} and phase current waveform i_R (50V/div, 2A/div, 2ms/div). (a) Symmetrical modulation (fr=fs = 6.00). (b) Multilevel modulation (fr=fs = 5.625).

to the reference sinusoidal wave. The principle of operation is the same as in references [8], [9]. This injection ratio is given as 15.47%, which is that presented for conventional inverters [9]. In the case of a SVC, the power supply and the load change places with each other compared to a conventional inverter. In general, the capacitor voltages can be controlled by the active power flow through them. In order to calculate the active power flow, the inverter load is substituted by a purely inductive load, and the capacitors of the SVC are substituted by a dc power supply. In this way, the possibility of controlling the capac- itor voltage will be discussed. By means of the phase shift of the third-order harmonic, the power delivered from the supplies varies as shown by curves i_1 and i_2 in Fig. 7 [10]. In the lower two supplies, current flows are identical but of opposite polarity, because of the symmetrical waveform. Thus, for the SVC where the supplies of the inverter are replaced by capacitors, control of the capacitor voltage would be possible. The total capac- itor voltage could also be controlled by varying the modulation index as for the three-level one [11]. In the figure, the circles and dots show the experimental results with the same experimental constants as just described later.

VI. Experimental Results and Discussions

A. Operating Waveforms

Fig. 8(a) shows the inverter output line voltage and phase current waveforms for the induction motor drive with no load using symmetrical modulation. It can be seen that the waveform e_{RS} is similar to the one shown in Fig. (2f). The experimental parameters are as follows. The reference sinusoidal frequency $f_s = 60$ Hz, the carrier triangular frequency $f_c = 360$Hz, that is, $f_r/f_s = 6.00$, the voltage modulation index $a = 0.9$ and the supply voltage $E = 200$ V. On the other hand, Fig. 8(b)shows the experimental waveforms for multilevel modulation, so the output voltage varies between two levels in a limited period, and the current waveform is reasonably improved [12].

Fig. 9 shows various current waveforms for multilevel modulation with an inductive load. Each current waveform is similar to the case in Fig. 3(k) to (m). These results show that the simulation results are valid. The experimental waveforms i_1 and i_2 seem to have a little dc components, because some active power flows due to the circuit and load losses. Compared to the simulated ones in Fig. 3(m), i_a, there is some sag near the peak value in the experiment, which is also due to the circuit and load losses.

Fig. 10 shows the voltage waveform across the interphase reactor for the experimental parameters shown above. The applied voltage is at the low level of $E/4$ and the repetitive frequency is high. The value of the interphase reactor is $L_R = 74$ mH and the unbalancing factor $k = 0.03$, where $k = (I_1 - I_2)/I_R$, I_1 and I_2 are currents in the reactor and I_R is the total current.

B. Harmonic Components

The experimental harmonic components of the output waveform are plotted in Figs. 4(b)–(d) and 5 using circles and other symbols. The experimental values coincide with the theoretical ones calculated from Table I and the simulated ones. These results show that the theoretical expressions and the simulated results are valid [14], [15].

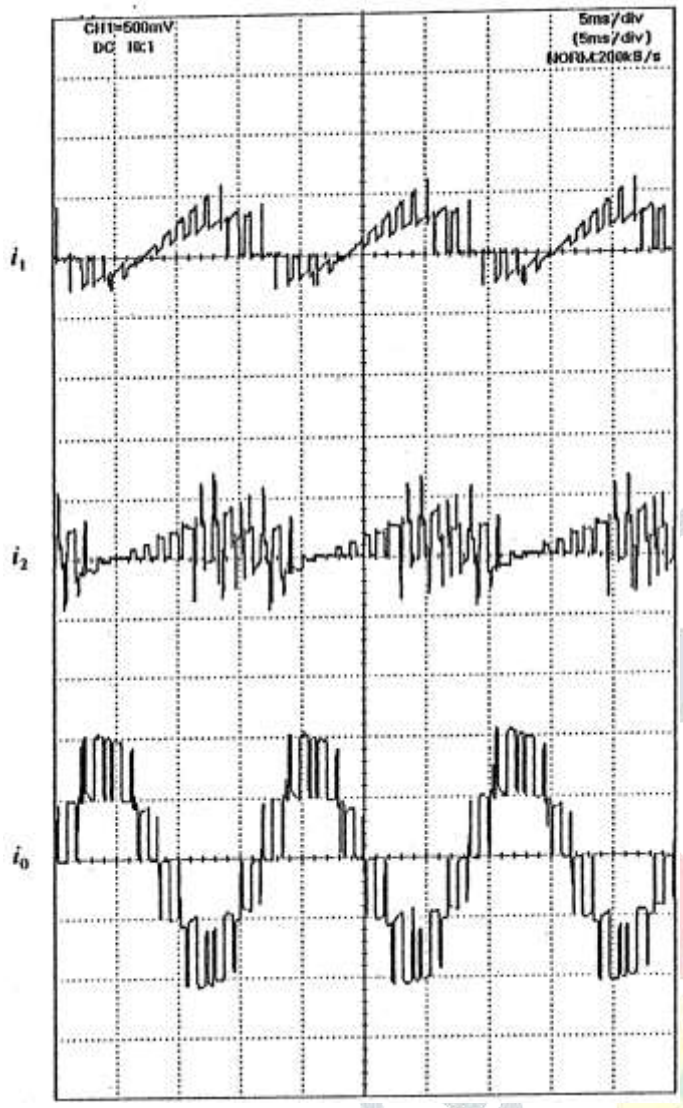


Fig. 9. Current waveforms with inductive load (5A/div, 5ms/div).

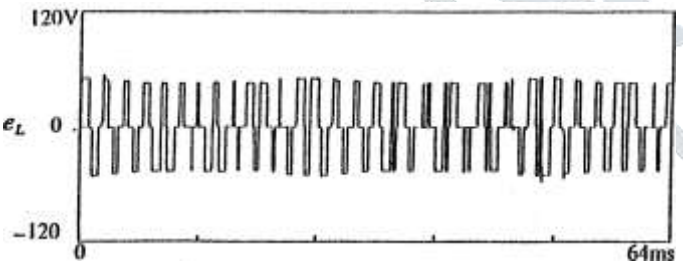


Fig. 10. Voltage waveform across the current sharing reactor.

VII. Conclusion

Multilevel inverters, including a five-level one, are effective for large capacity ac motor drives or the large capacity converters in power systems like the SVC. For still larger capacity, paralleling the inverters is a promising method at present. In this paper, some effective techniques are devised and designed for paralleling the inverters and controlling the waveforms. By means of various carriers with appropriate phase differences, such as multilevel carriers, undesirable harmonics are eliminated and the waveforms of the output currents become acceptably sinusoidal.

It is found that the dc current flow of dc power supplies can be controlled by means of phase shifting of the injected third order harmonics. In the near future, various strategies of capacitor voltage control including the mentioned technique will be presented and developed in the SVC.

In order to realize larger capacity converters, the fundamental characteristics of the converter are discussed and presented.

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