A REVIEW OF MODULATION SCHEMES FOR SINGLE PHASE FIVE- LEVEL CASCADED MULTILEVEL INVERTER

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Abstract*—For medium voltage and high power applications, multilevel inverter has been accepted as a better alternative as it has good waveform quality, better performance and is comprised of switching devices subjected to low stresses. Among the various topologies of multilevel inverters, Cascaded H-bridge inverter has been found as more reliable, easy to design and has satisfactory performance. This paper analyses the performance of single phase 5- level Cascaded H-bridge inverter. The performance of the inverter is analyzed through simulation using Phase Shifted Pulse Width Modulation (PSCPWM) and Level Shifted Pulse Width Modulation technique (LSPWM). LSPWM can be classified into three subgroups i.e. Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD). PSCPWM technique and various methods of Level Shifted PWM techniques are implemented for Single Phase Five Level Cascaded H-Bridge inverter. Simulation results are obtained using MATLAB/ SIMULINK and %THD comparisons are tabulated.

Index Terms*—Cascaded H-bridge Multilevel Inverter, Level Shifted Pulse Width Modulation, Phase Shifted Pulse Width Modulation, Phase Disposition, Phase Opposition Disposition, Alternate Phase Opposition Disposition, Total Harmonic Distortion.

I. INTRODUCTION

Multilevel inverter is a power electronic converter that is capable of generating a desired alternating waveform of several steps depending on the choice of number of levels and modulation technique. Multilevel inverters are popularly known due to their applications in medium voltage drives with power and voltage ratings ranging between 1MW to 4MW and 3.3KV to 6.6KV. Multilevel inverters are known for their ability to attain a stair case waveform that nearly reflects a pure sinusoid comprising negligible amount of harmonic content [1]. Multilevel inverters are classified into two types- Single DC source inverters and Multiple DC source inverters depending on the requirement of number of sources as shown in Fig.1. Diode Clamped Multilevel inverters and Flying Capacitor multilevel inverters require only one DC source. Cascaded H-Bridge inverter falls under the category of Multiple DC source inverters [4].

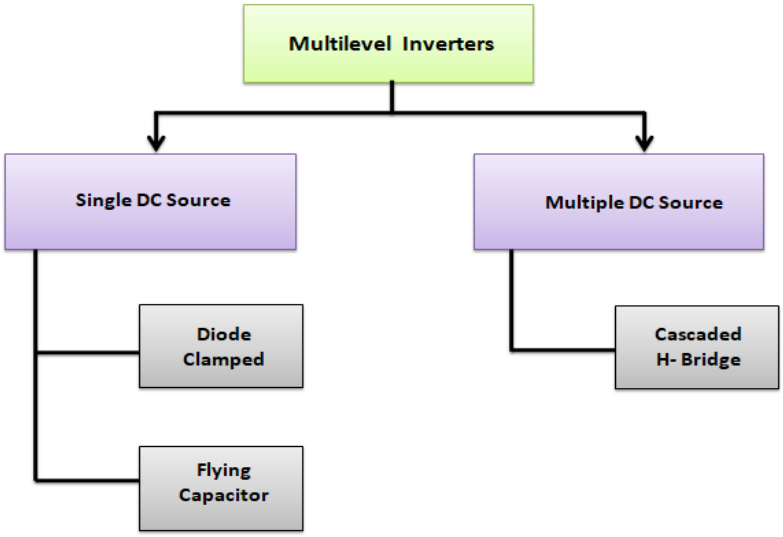

Fig.1. Classifications of Multilevel Inverters

The number of components required to build a Cascaded Multi Level inverter for any level of output voltage is less as compared to that of Diode Clamped and Flying Capacitor inverter structures [4]. The circuit configuration is simple and does not require heavy and lossy snubber circuit. Thus it is less expensive than other multilevel inverter configurations. Cascaded multilevel inverters are widely used in electric vehicle applications, active power filters, motor drives, power factor correction devices, var compensators, interfacing the grid with renewable energy sources etc [6].

For achieving better performance and proper efficiency, multilevel inverters require a pertinent modulation technique. Modulation method may be a simple method, approach or an algorithm that compares a modulating waveform and carrier signal such that gating pulses are generated that decide sequential switching pattern of power electronic devices in a multilevel converter.

Several modulation techniques have been available in the literature. Considering switching frequency as a factor, modulation techniques are classified into fundamental switching frequency techniques and high switching frequency techniques [3]. Sinusoidal Pulse Width

Modulation techniques and Space Vector Modulation technique are the types of high frequency techniques. Space Vector Control and Selective Harmonic Elimination are the types of Fundamental Switching Frequency modulation techniques [2].

Among all the modulation techniques available Sinusoidal PWM technique is simple and can be implemented for any type of multilevel inverters without any complexity [3]. In this paper, a brief note on Single phase three level Cascaded Multilevel inverter is presented. Later on, design and simulation of a Single phase Five level Cascaded Multilevel inverter is discussed for all types of SPWM techniques. This paper also presents a brief note on all the modulation techniques. Simulation results of output voltage waveforms obtained for Single phase Five level Cascaded multilevel inverter are presented using modulation techniques and corresponding harmonic spectrum are depicted.

II. CASCADED H-BRIDGE CONVERTER

Cascaded H-Bridge inverters are used for medium voltage and high power applications. The number of levels of inverter output voltage can be increased by increasing the number of series connected H-bridge cells. Each call requires a separate DC source. The modular structure inverter made it more flexible to be used for high power FACTS applications. The necessity for separate dc sources for each H-bridge cell made the inverter suitable for renewable energy applications.

A. Basic Three level Cascaded H-Bridge Inverter

Fig.2 shows a single H-bridge cell which results in three levels of output voltage (Vdc, 0, -Vdc) and Table.1gives the Switching combination for a Three Level Cascaded Multilevel Inverter.

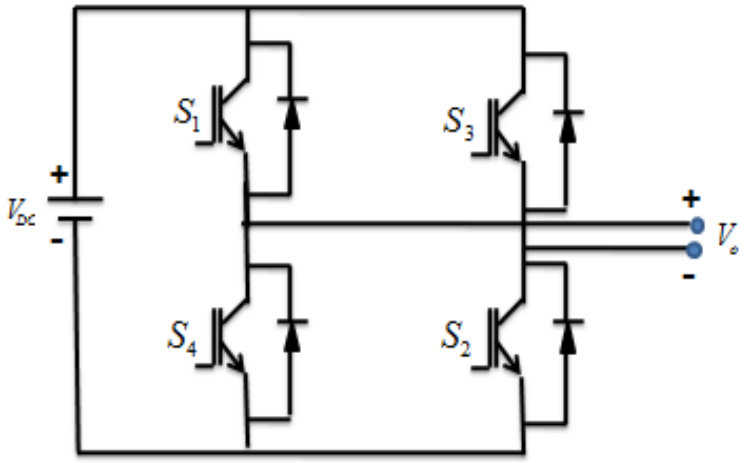

Fig.2. A basic Three Level configuration of Cascaded- H Bridge Inverter

Table.1 switching combination for a Three Level Cascaded Multilevel Inverter

Switches ON	Switches OFF	Output Voltage level
S1,S2	S3,S4	Vdc
S3,S4	S1,S2	-Vdc
S1,S3	S2,S4	0
S2,S4	S1,S3	0

B. Five level Cascaded H-Bridge Inverter

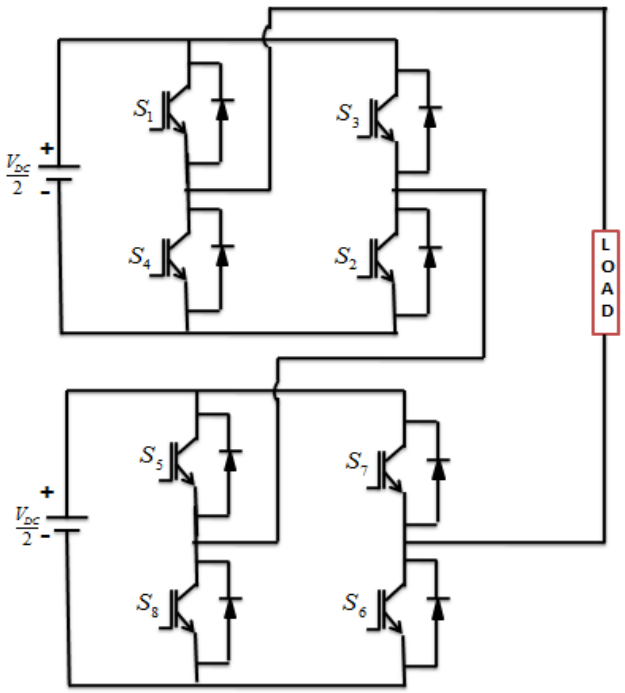

Fig.3. Single phase Five Level configuration of Cascaded H- Bridge Inverter

Fig.3 shows single phase configuration of a Five level Cascaded H-Bridge inverter. The circuit is obtained be connecting another H-Bridge cell in series to a single cell. A three level Cascaded H-bridge inverter will result in three levels of output voltage Vdc, 0, -Vdc. By adding a H-Bridge cell in series, the resultant configuration will result in five levels of output voltage $\left(V_{dc}, \frac{V_{dc}}{2}, 0, -\frac{V_{dc}}{2}, -V_{dc}\right)$. Table.2 shows the switching states of Five level Cascaded H-Bridge inverter. The number of output voltage levels 'N' in a Cascaded inverter is given by the equation (1).

$$N = 2S + 1 \quad (1)$$

Where 'S' denotes the number of DC voltage sources. Thus in order to obtain output voltage, of five levels, two separate DC sources is necessary.

Cascaded H-Bridge Multilevel Inverters have modularized structure. Clamping diodes are not necessary and necessity of voltage balancing is avoided due to absence of capacitors. However, this type of topology requires separate DC sources.

Table.2. Switching States of Five Level Cascaded H- Bridge Inverter

Output Voltage (V_O)	Switch state							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_0 = V_{dc}$	1	1	0	0	1	1	0	0
$V_0 = \frac{V_{dc}}{2}$	1	1	0	0	0	0	0	0
$V_0 = 0$	0	0	0	0	0	0	0	0
$V_0 = -\frac{V_{dc}}{2}$	0	0	1	1	0	0	0	0
$V_0 = -V_{dc}$	0	0	1	1	0	0	1	1

III. MODULATION TECHNIQUES

The procedure of turning on/off of power electronic switches of an inverter in a proper sequence so as to attain a nearly sinusoidal waveform is known as modulation. Based on the switching frequency, modulation techniques are classified as shown in Fig.4. Fundamental switching frequency techniques involve only one of two commutations of power semi conductor switches per cycle of output voltage .Space Vector Control (SVC) is best known example of Fundamental switching frequency technique.

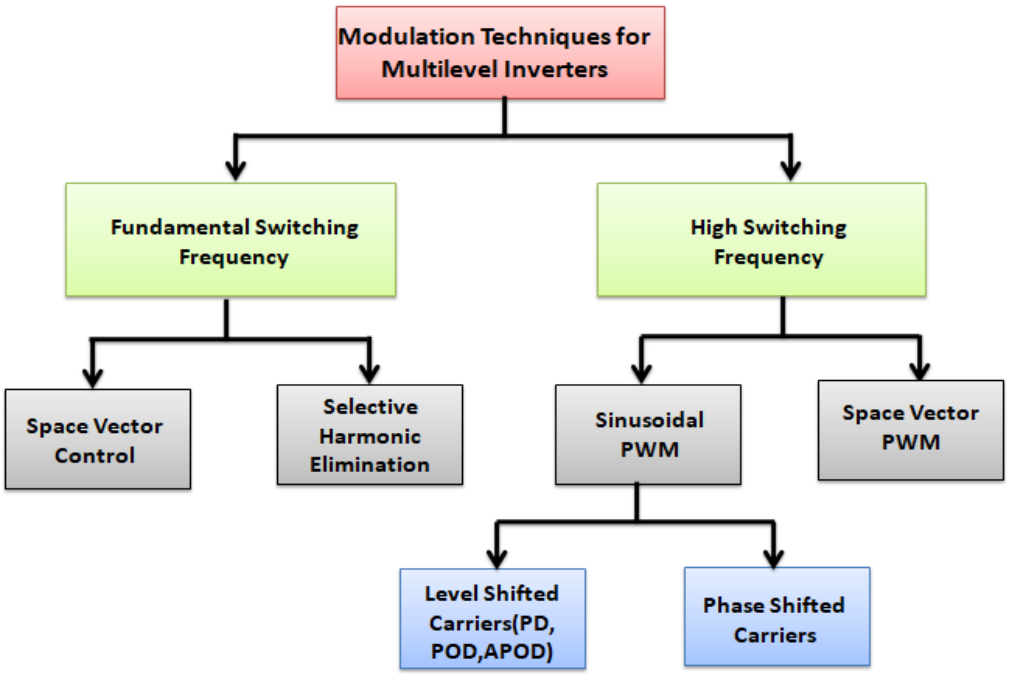

Fig.4.Broad classification of Modulation Techniques for Multilevel Inverters

The number of triggering and commutations of power electronic switches within a cycle of fundamental voltage is very high in High Switching frequency techniques. Sinusoidal Pulse Width Modulation (SPWM) is a popular example of high switching frequency technique.

The concept of Space Vector PWM was proposed by Hotlz et al in 1987 and modified by Van der Broeak et al in 1988. The principle of SVPWM technique is to approximate the voltage space vector trajectory by sequential switching of power electronic devices. During this period, the continuously rotating reference vector is sampled at a sampling frequency. During this period, reference vector is assumed to remain constant. This technique also includes calculation of switching times for each switching state [2].SVPWM principle can be extended to higher levels of output voltage and to different types of multi level inverters. The voltage utilization ratio of SVPWM is 15% higher than that of SPWM technique [2] [9]. This feature makes the converters feasible for high voltage and high power applications.

The principle of Selective Harmonic Elimination was proposed by Richard and Husmukh in 1973. In this method, the square wave output is chopped multiple times. Chopping time defines switching angles of the inverter. The output waveform of the inverter is controlled by proper distribution of switching angles that in turn decides the turn on/ off of inverter switches. This method is effective in eliminating lower order harmonics and thus is capable of generating output waveform of better quality.

Sinusoidal Pulse Width Modulation (SPWM) is a simple technique that is used to a sequence of voltage pulses by consequent turning on/ off of power electronic switches in a converter [5]. This technique results in generating pulses of constant amplitude but with varying width. The technique involves comparing a reference sine wave with a high frequency triangular carrier wave. Fig.5 shows the output pulses generated. Vr is reference wave and Vc is the peak value of high frequency carrier wave. The instants of switching and commutation of the switches is determined by the points of intersection of reference and carrier waves.

SPWM techniques when implemented for multilevel inverters require more number of carrier waves. Thus for a N-level inverter, N-1 carrier waves are required. For multilevel inverters, SPWM technique is further classified as follows depending on the requirement of multiple carrier signals [10].

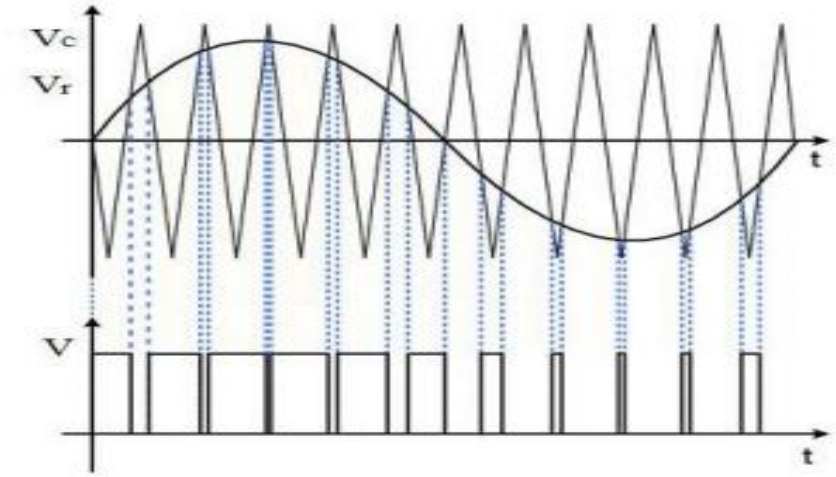

Fig.5. Concept of Sinusoidal Pulse Width Modulation

- Phase Shifted Pulse Width Modulation (PSPWM)
- Level Shifted Pulse Width

Modulation (LSPWM)

- ✓ Phase Disposition (PD)
- ✓ Phase Opposition Disposition (POD)
- ✓ Alternate Phase Opposition Disposition (APOD)

A. Phase Shifted Pulse Width Modulation (PSPWM)

PSPWM technique is common is Cascaded H- Bridge inverter as it simple and can be effectively implemented to any levels of an inverter structure. This technique is also known for even distribution of power for individual H-bridge cells in an inverter. For Phase shifted modulation, all the carrier signals should have equal amplitude and frequency [7] [8]. However, for an N-level inverter, the number of carrier waves required is N-1, that should be displaced by $\frac{360^0}{N-1}$ with respect to each other. Triangular carrier signals are chosen commonly that are compared with a sinusoidal reference wave for generating gate pulses required for the inverter circuit. Fig.6 shows the carrier signals required for a 5-level Cascaded H-Bridge inverter. As seen in Fig.6 carrier triangular signals are required that are phase displaced by 90 degrees. These carrier signals are compared with sinusoidal reference wave to generate the gating pulses.

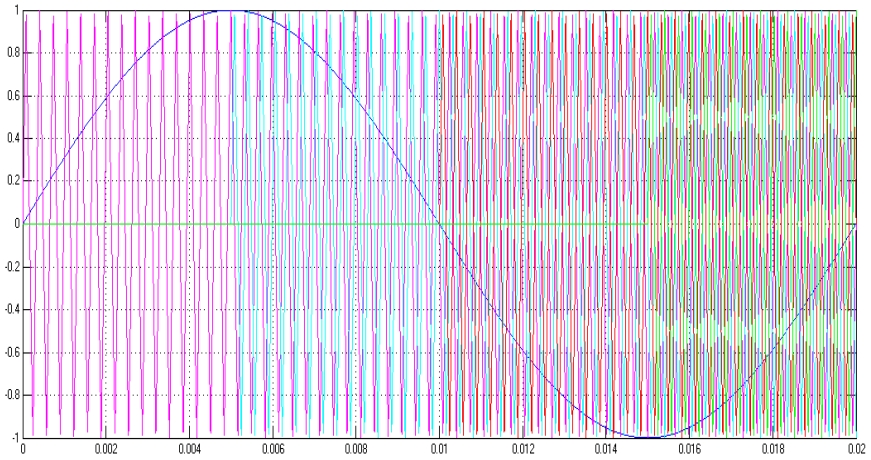

Fig.6. Carrier waves in PSPWM

B. Level Shifted Pulse Width Modulation (LSPWM)

In LSPWM, the number of carrier signals needed for N-level inverter is N-1. The signals should have equal frequency and equal amplitude. All carrier signals are phase shifted with respect to each other taking zero reference into consideration. Carrier signals are compared with the modulating signal and a pulse is generated at the instants when the amplitude of modulating signal is greater than carrier signal [7][8]. Following are different types of LSPWM technique.

(i) Phase Disposition (PD)

In PD technique, all the four carriers are in phase as shown in Fig.7.

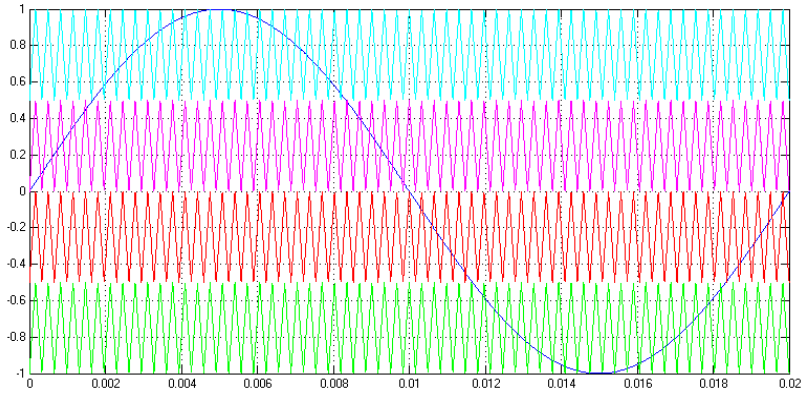

Fig.7. Reference and carrier signals in PD Modulation method

(ii) Phase Opposition Disposition (POD)

In POD technique, the carriers above zero reference are 180 degrees out of phase with respect to the carriers below the zero reference as shown in Fig.8.

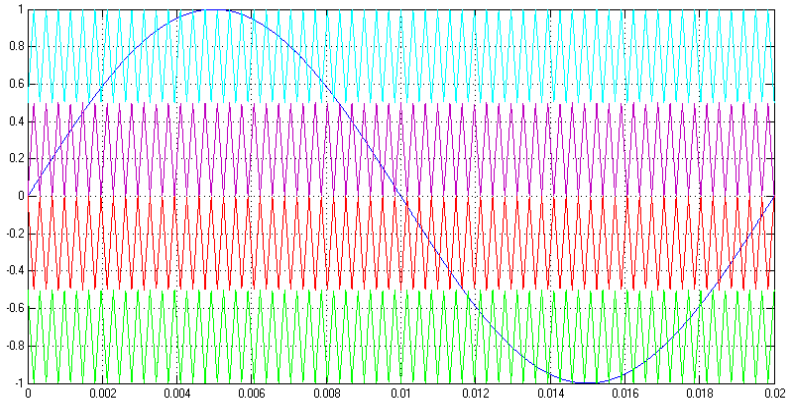

Fig.8. Reference and carrier signals in POD Modulation method

(iii) Alternate Phase Opposition Disposition(APOD)

In APOD technique, each carrier is phase shifted by 180 degrees with respect to its adjacent carrier as shown in Fig.9.

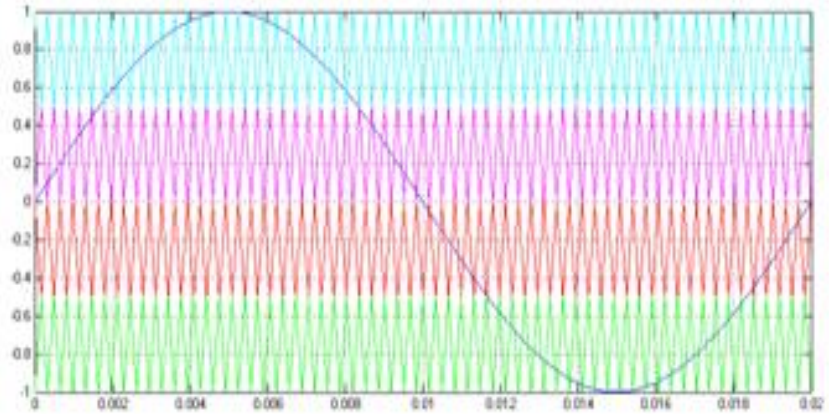

Fig.9. Reference and carrier signals in APOD Modulation method

However, for all types of LSPWM techniques it is necessary that all carriers should have equal frequency and amplitudes. Table.3 shows the simulation parameters of the system.

Table.3 Simulation Parameters

DC Voltage	**200V**
Switching frequency (fs)	3050HZ
Load resistance	10ohm
Modulation index	1

IV. SIMULATION RESULTS

All the above mentioned methods are simulated in MATLAB/SIMULINK at modulating carrier frequency of 3050 Hz, modulation index= 1, resistive load R=10 Ω.

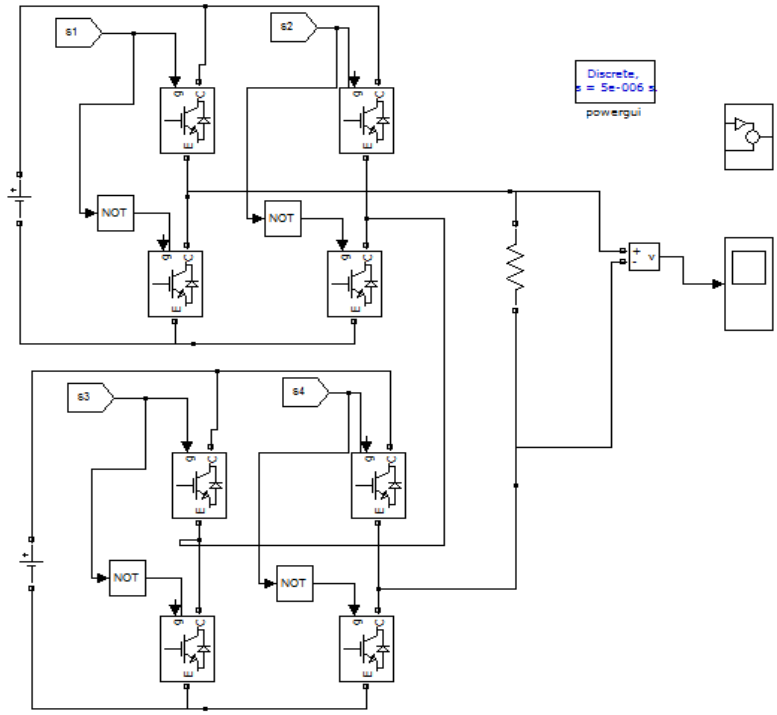

Fig.10. Simulation model of Five Level- Cascaded H-Bridge Inverter

Fig.10 shows MATLAB/ Simulink model of a Five Level- Cascaded H-Bridge Inverter. It requires two H-bridges, thus satisfying Eq.1. Each H-bridge in turn is composed of four IGBT switches.

Fig.11 depicts the five level output voltage of Cascaded H-Bridge Inverter with voltages -200V, -100V, 0, 100V, 200V (using PSPWM). Fig.12 shows harmonic spectrum of output voltage of Five Level Cascaded H-Bridge inverter using PSPWM technique. % THD in output voltage is 26.84%.

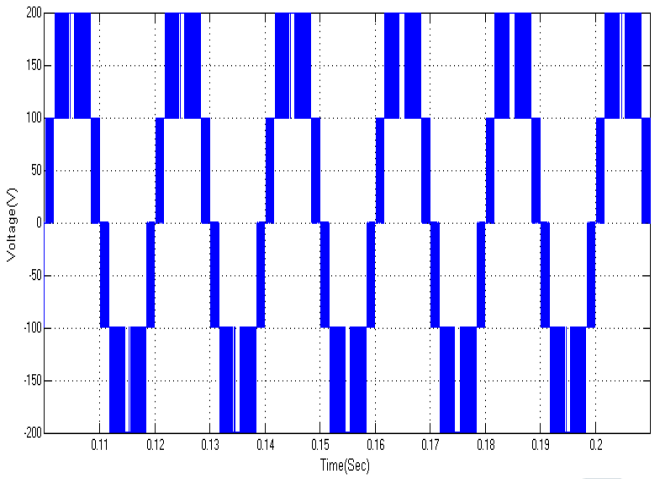

Fig.11.Five level output voltage of Phase Shifted PWM

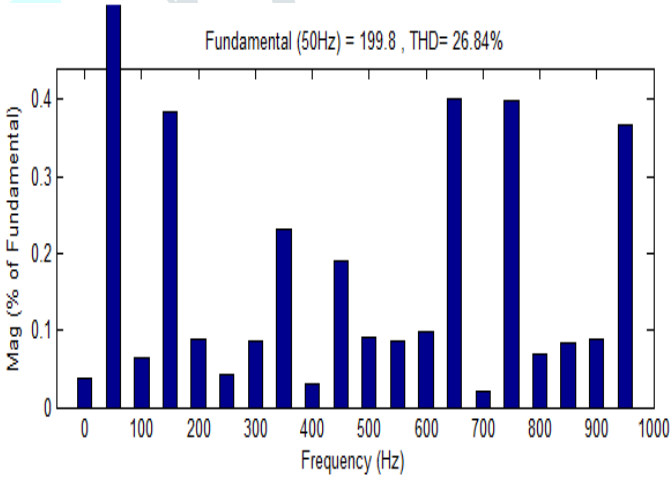

Fig.12. FFT analysis of Five Level- Cascaded H- Bridge Inverter using Phase Shifted PWM.

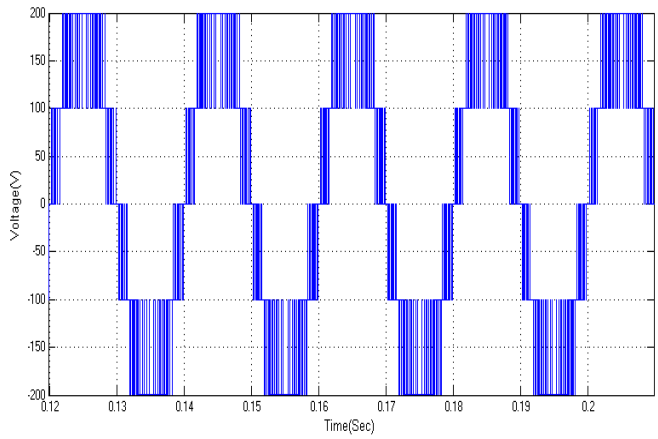

Fig.13. Five Level Output Voltage of Level Shifted PWM with PD.

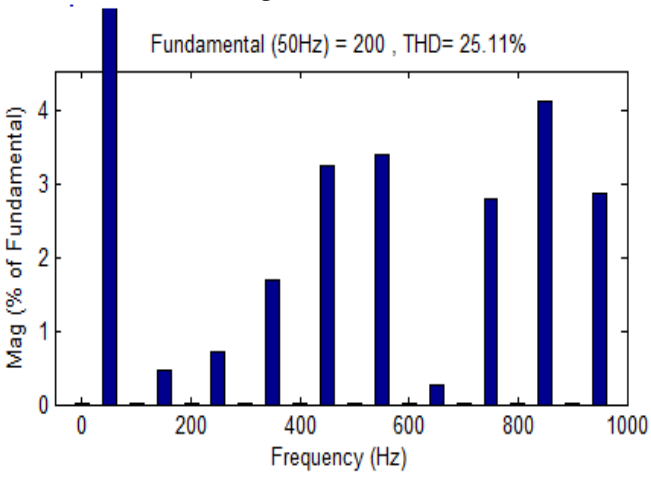

Fig.14. FFT analysis Of Five Level Inverter using PD

Fig.13 represents the five level output voltage waveform obtained from Five level Cascaded H- Bridge inverter using PD type PSPWM technique. Fig.14 represents harmonic spectrum of corresponding output voltage waveform. % THD is around 25.11%.

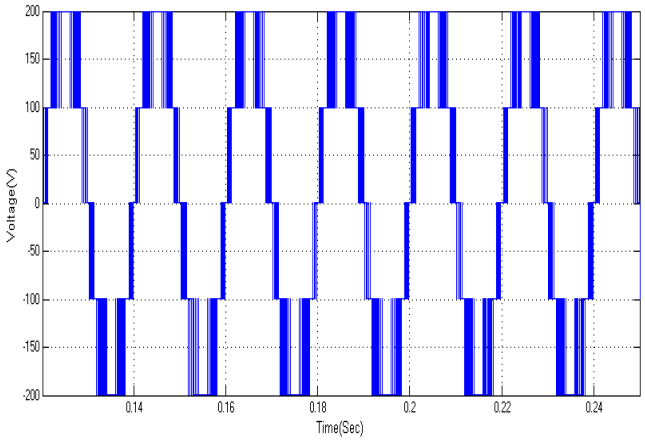

Fig.15. Five Level Output Voltage of Level Shifted PWM with POD.

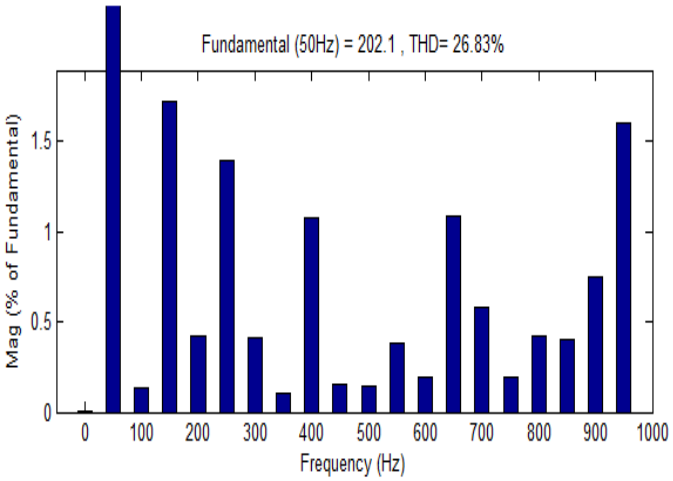

Fig.16. FFT analysis of Five Level Inverter using POD.

Fig.15 represents the five level output voltage waveform obtained from Five level Cascaded H- Bridge inverter using POD type PSPWM technique. Fig.16 represents the harmonic spectrum of the corresponding output voltage waveform. % THD is nearly 26.83%.

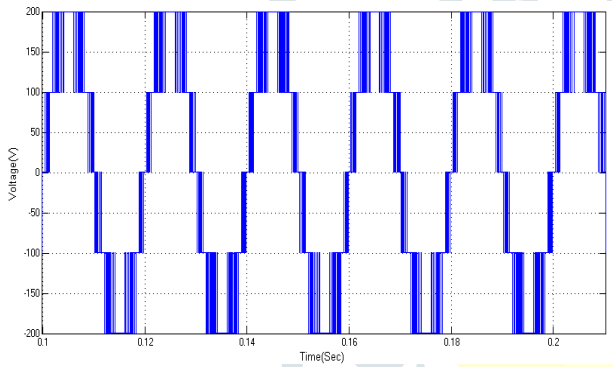

Fig.17. Five Level Output Voltage of Level Shifted PWM with APOD

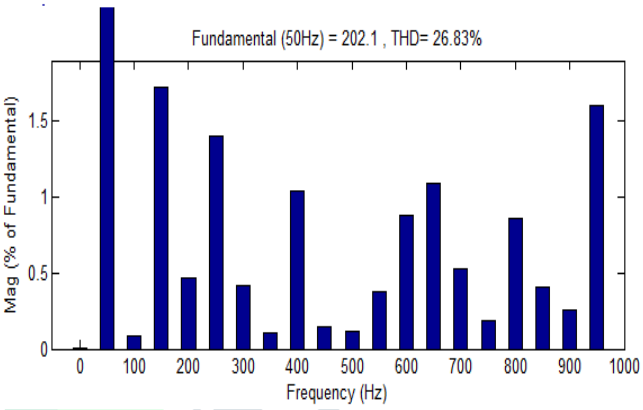

Fig.18.FFT analysis of Five Level Inverter using APOD.

Fig.17 represents the five level output voltage waveform obtained from Five level Cascaded H- Bridge inverter using APOD type PSPWM technique. Fig.18 represents the harmonic spectrum of the corresponding output voltage waveform. % THD is nearly 26.83%.

Table.4 Comparison of %THD in output voltage waveform.

Five Level CHB inverter	**PSC PWM**	**LSC PWM**		
		PD	**POD**	**APOD**
	26.84%	25.11%	26.83.%	26.83%

V. CONCLUSION

IN THIS PAPER DIFFERENT TYPES OF MODULATION TECHNIQUES THAT CAN BE EMPLOYED FOR MULTILEVEL INVERTERS ARE BRIEFLY EXPLAINED. THIS PAPER ALSO SUMMARIZES THE EFFECT OF PSPWM AND LSPWM TECHNIQUES ON A SINGLE PHASE FIVE- LEVEL CASCADED H-BRIDGE INVERTER CIRCUIT. THIS PAPER CANNOT COVER ALL THE RELATED WORK, BUT THE FUNDAMENTAL PRINCIPLES OF DIFFERENT MULTILEVEL INVERTERS HAS BEEN INTRODUCED SYSTEMATICALLY. IN THIS PAPER, SINGLE PHASE FIVE -LEVEL CASCADED INVERTER WITH PSCPWM AND LSCPWM IS SIMULATED. THE FIVE LEVEL OUTPUT VOLTAGE AND CORRESPONDING HARMONIC SPECTRUM ARE PRESENTED FOR EACH METHOD. THE %THD OF OUTPUT VOLTAGE FOR LSPWM TECHNIQUE IS COMPARED FOR THE TYPES PD, POD, APOD. THE SUMMARY TABLE GIVES %THD DETAILS OF THE OUTPUT VOLTAGE FOR PSPWM AND FOR ALL TYPES OF LSPWM- POD, PD, AND APOD METHODS. PD HAS LESS HARMONIC DISTORTION CONTENT AS COMPARED TO POD AND APOD AND PSPWM METHODS. THE INTENTION WAS SIMPLY TO PROVIDE A BRIEF IDEA TO THE READERS INTERESTED IN LOOKING BACK ON THE EVOLUTION OF MULTILEVEL INVERTER TECHNOLOGIES AND MODULATION TECHNIQUES EMPLOYED.

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