ANALYSIS OF LOW POWER IN THE EMBEDDED SYSTEM USING OPTIMIZATION TECHNIUES

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ABSTRACT: VLSI (Very Large Scale Integration) procedure has gigantic improvement in the course of the most recent ten years with highlights sizes being downscaled from micrometer to nanometer administration. This paper is more useful to analyze the design factors of the low power VLSI systems. The element sizes have moved from couple of small scale meters to couple of nanometers. Due to the increasing high complexity of modern VLSI chip design, Electronic Design Automation (EDA) tools play an important role in delivering high system performance. This work proposes the minimized interconnect power dissipation are also discussed in the detailed manner.

Key words: Low power, Optimization, VLSI Circuits, Power Consumption

I. INTRODUCTION
VLSI System

Moore's law expresses that the aggregate number of transistors on a solitary coordinated circuit pairs at regular intervals. The movement is from couple of several transistors on a solitary chip to the couple of a huge number of transistors on a solitary chip now-a-days. This noteworthy relocation is conceivable just by diminishing the component sizes of the transistor incorporated circuit. The element sizes have moved from couple of miniaturized scale meters to couple of nanometers. Because of the expanding high multifaceted nature of present day VLSI chip design, Electronic Design Automation (EDA) instruments assume an imperative part in conveying high framework execution. VLSI physical design process incorporates apportioning, floorplanning, arrangement, directing and compaction (Chang et al 2000 and Chen et al 1999). In future, the gigantic development of VLSI circuits will depend on the advancement of physical design robotization instruments.

In the physical design process, Routing has been a critical issue in VLSI back-end design since the nature of directing outcomes has awesome effect on different design measurements, for example, circuit delay, power utilization, chip dependability and manufacturability and so on. With the propelled creation innovation entering nanometer scale, particularly VLSI steering has been confronting more difficulties. With gadgets work at a higher speed, the interconnect delay and interconnect power dispersal turn out to be more huge. The issue of limiting these interconnect delay and interconnect power scattering has been tended to at steering stage. Directing is the way toward masterminding circuit wires on a design. In VLSI design, directing comprises of deciding most limited way between source to sink places of all pieces on the format, to such an extent that the wirelengths are limited and imperatives are fulfilled.

II. OVERVIEW OF VLSI DESIGN PROCESS

In VLSI technology, a single chip contains more than billions of transistors. The overall design process is divided into a sequence of steps: system specification, architectural design, logic design, circuit design, physical design or circuit layout, fabrication, packaging and testing (Hu et al 1985). These design steps are demonstrated by the flow chart given in Figure 1.1. The design cycle flinches with the system description. It is used to determine the specifications of the system, primarily functionality, performance, and physical dimensions. It also includes the design techniques and fabrication technology. The stipulationsfor the size, speed, power, and functionality of the VLSI system are determined by technology, market demand, and economical perspective (Sherwani 1999).

In the architectural design step, the design purpose and system constraints are defined. The system is divided into more than a few sub components that interrelate with each other. Next, functional design involves identifying the main functional components of the system as well as the interconnection requirements between the components. Generally, a timing pattern or other relationships between components are the end result of the functional design.

III. DESIGN CHALLENGES IN EMBEDDED SYSTEMS

Some of the design challenges and scope for design of embedded systems to meet the designconstraints are as listed below:
- Design analysis for statistical performance characteristics
- Packaging and Integration of digital, analog and power circuits to reduce size.
- Low cost, reliability with minimal redundancy
- Accurate thermal modeling
- De-rating components differently for each design depending on operating environment.
- Variable "design margin" to permit tradeoff between product robustness and aggressive cost optimization.
- Software and I/O driven hardware synthesis, Reliable software.
- Ultra low power design for long term battery operation.
- Life cycle, cross design component cost models.
- Partitioning / synthesis to minimize recertification costs.
- Ensuring complete interface, timing and functionality compatibility when upgrading designs.

> ➢ Cost effectively updates old designs to incorporate new components
> ➢ Rapid redesign to accommodate changing form factors, control algorithms and functionality requirements.
> ➢ Customize designs while minimizing component variant proliferation.
> ➢ Create design tools and methodologies that provide unique advantages for embedded design.

There are several optimization techniques available for design of embedded system which concentrates on the design for optimization of power, cost, and area. There is always tradeoff which exists between different design metrics which has to be handled carefully by the designer to improve the overall performance of the system.

Design Challenge – Optimizing Design Metrics

The embedded system designer has to meet the design challenge of constructing an implementation which optimizes numerous design metrics. Improving one metric will affect the other. This is compared to a wheel as shown in fig 1, with numerous pins such that if one is pushed the other comes out. Hence the designer needs to migrate from one technology to another to meet the constraints and also have the knowledge of both hardware and software.The power continues to be an important metric and a challenge for embedded designers isthat as the size of the systems are becoming less, the increase in integration level has resultedin more and more heat being generated and hence increase in power dissipation of thesystem. This needs to be addressed properly to meet the performance requirement of thesystem.
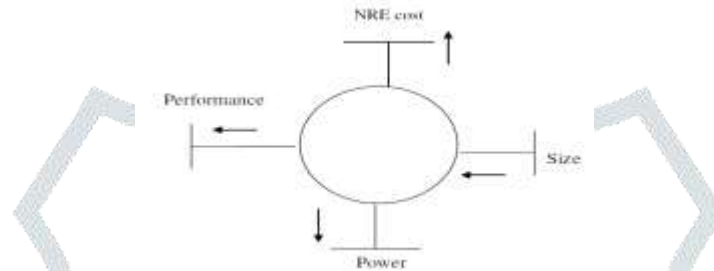

Fig 1: Design Metrics pinball

Performance Design Metrics:

Performance of an embedded system is very important as it defines how long the system takes to respond to execute the desired tasks. There are many metrics which are associated with the performance like clock frequency or instructions per second. The performance is measured in terms of latency or response time and also throughput. It is a key challenge for the designer to optimize all the design metrics simultaneously. The designer has to suitably select the advantages and disadvantages of various processor technologies, IC Technologies and for better optimization the designer should focus on mobility of functions between hardware and software. Hardware /software co-design is a field which emphasizes on the development of synthesizers and simulators that enable the development of systems using both hardware and software. Finally the optimization of metrics like speed, size, cost and power depends on the selection of customized technologies or programmable technologies. The application areas of embedded systems are very vast. Very significant and important applications can be found in portable devices like Digital Camera, Mobiles, Smart phones,Tablets etc where several techniques have been implemented to make them energy efficient by increasing battery life.

IV. LOW POWER DESIGN

Power is an important design metric to be considered in embedded system design since the requirements for portable devices with advanced features are becoming popular. As the size of these devices is becoming smaller, the power dissipation in these devices and also in non portabledevices has to be reduced. More complex processors are being used in these systems which have increased the power dissipation level to a greater extent and hence suitable measures to be taken at the designing stage itself to reduce power.
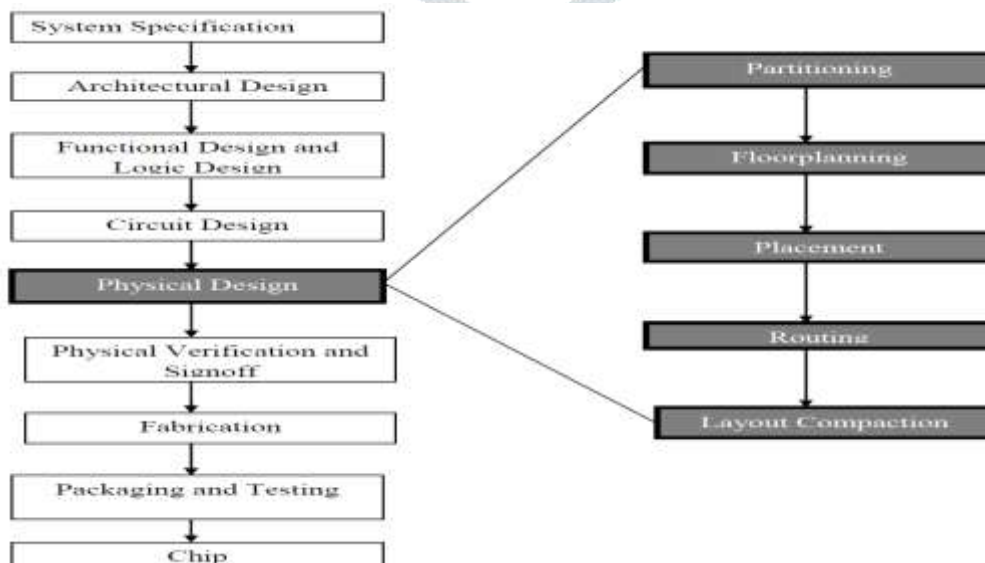

Fig 2: VLSI design process

V. DESIGN TECHNIQUES FOR POWER REDUCTION

There are various techniques described in the literature such as
- Using the devices operating at different voltages
- Using devices operating at different frequencies
- Using devices having different modes of operation (i) Running (ii) waiting and (iii) idle
- Using devices capable of operating at different clock speeds
- Using scheduling techniques in the software program for reducing power consumption in embedded systems.

It is clear from the above discussions that the choice of suitable processors for embedded applications is important. Most of the available processors have implemented one or more power optimization techniques. However there exists a major requirement for the design of suitable architecture with external and internal power optimization. This work focuses on the study of various power optimization techniques for embedded system followed by the design of an embedded system and implementation of power optimization techniques, which is more useful to reduce the power consumption of the VLSI circuits.

CONCLUSION

The analysis depicted in this exploration, adds to framework level power optimization with the low power VLSI circuits. In this work, the execution debasement is forestalled through suitable some models of the framework are discussed. It is reasoned that for successful power optimization, mix of different optimization methods must be actualized in the VLSI System.This paper is more useful to analyze the design factors of the low power VLSI systems. The feature sizes have moved from few micro meters to few nanometers.

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