

# COMPARATIVE ANALYSIS OF HYBRID CORDIC PROCESSOR ON FPGA

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**Abstract**— The CORDIC or CO-ordinate Rotation Digital Computer is a fast, simple, efficient and powerful algorithm for the implementation of various elementary, especially trigonometric functions using minimal hardware such as shifters, adders/subtractors and comparators. CORDIC works by rotating the coordinate system through constant angles until the angle reduces to zero. The angle offsets are selected such that the operations on X and Y are only shifts and adds. This Paper contains the survey about some Speed parameter for Cordic algorithm on FPGA.

**Index Terms**—Instruction Set, CISC, Cordic, Hybrid, FPGA

**I. INTRODUCTION (COMPARISON OF CORDIC PROCESSOR OVER NORMAL PROCESSOR)** - Normal processor have slow processing where Cordic processor have parallel computing that's why speed his very high compare to normal processor.

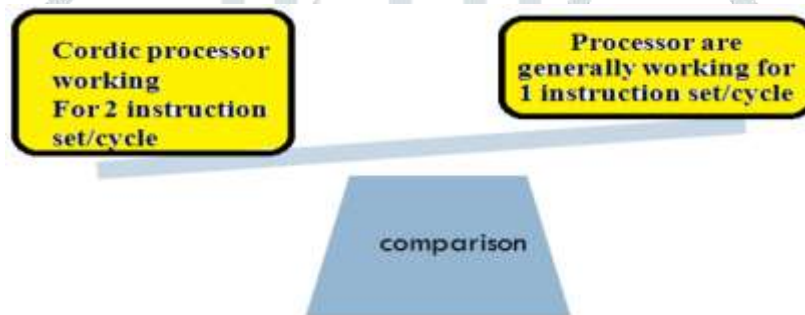


Figure 1. Cordic Processor vs. Normal Processor

All CORDIC is an acronym for Co-ordinate Rotation Digital Computer and was derived by Jack E Volder in 1959 for the purpose of calculating trigonometric functions. Its popularity came about nearly twenty years later when VLSI solutions became a reality.

Instead of using Calculus based methods such as polynomial or rational functional approximation, it uses simple shift, add, subtract and table look-up operations to achieve this objective. It is usually implemented in either rotation mode or vectoring mode. In either mode the algorithm is rotation of an angle vector by a definite angle but in variable directions. This fixed rotation in variable direction is implemented through an iterative sequence of addition/subtraction followed by bit-shift operation. The final result is obtained by appropriately scaling the result obtained after successive iterations. Owing to its simplicity the CORDIC algorithm can be easily implemented on a VLSI system.

Havilland and Tuszynski designed and built a CORDIC processor in 1980 which used a iterative process to calculate circular, linear and hyperbolic functions. A more recent implementation (1993) by Duprat and Muller discusses the possibility of using redundant number system for the representation of signed digit.

## II. OVERVIEW OF CORDIC PROCESSOR ALGORITHMS:-

**1. Application-Specific Instruction-set Processor** - ASIP can act as an alternative to ASIC and GPP design if it does satisfy the critical points of power consumption, total delay, manufacturing cost and productivity of those designs the ASIP devices that consists of simple programming characteristics have higher productivity. Productivity causes ASIP to be more applicable and to have lower cost in comparison to GPP and ASIC design. The last reason that speed in these application specific processors is higher than the general purpose processors. ASIP design will be considered as an alternative to ASIC and GPP design if it satisfy these four important parameters: power, delay, cost, and productivity. Merits of ASIP is Reduce power consumption, Reduce delay, Reduce productivity cost, but design is more complex [1].

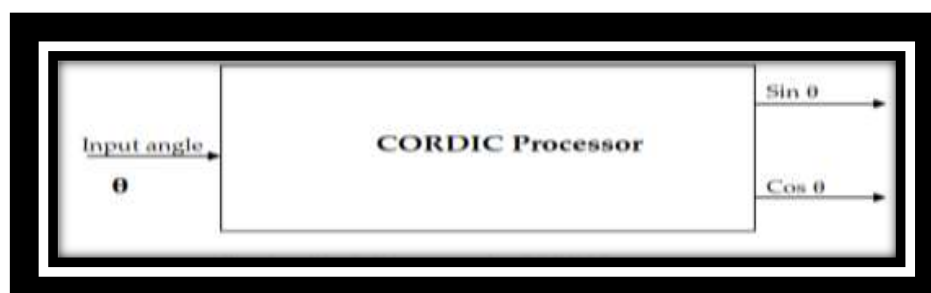


Figure 2. Basic block diagram of Cordic [1]

**2. O2D-DWT Architecture** - O2D-DWT architecture is designed using only adders and shifters for high speed operation and is applied on fingerprint image to generate four sub-bands. The optimized Fast Fourier Transform (OFFT) architecture is designed by computing different twiddle factor angles using modified CORDIC processor and is applied on LL sub-band coefficients to generate final fingerprint features. Performance of proposed real time architecture is better compared to existing architectures. no high speed spatial domain architecture [2]. The Performance of proposed architecture is better compared to existing architecture for the following reasons as (i) the O2D-DWT is implemented using only shifters and adders and (ii) the OFFT is realized by computing twiddle Factor using modified CORDIC processor [2].

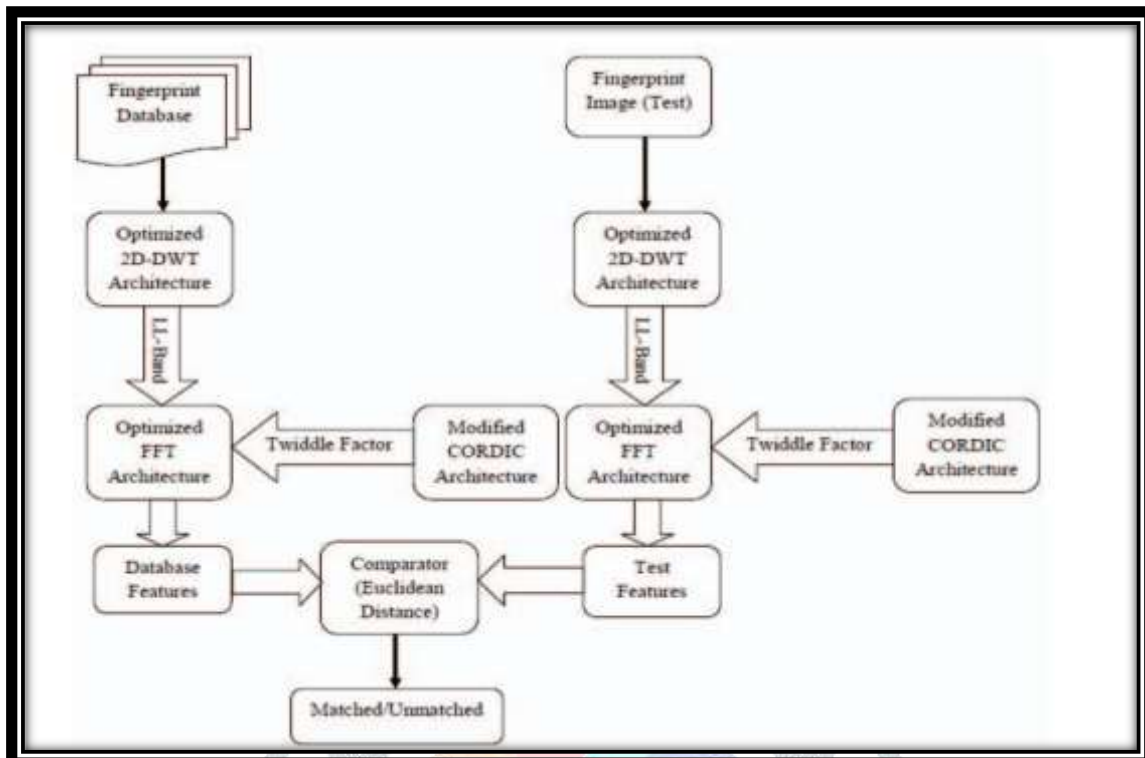


Figure 3. O2D-DWT architecture [2]

**3. FFT Using CORDIC** - The idea is to reduce the computational complexity of FFT using CORDIC processor. The CORDIC processor is hardware efficient which minimizes the computational complexity for twiddle factor computations. The FFT extract features of fingerprint and is implemented using CORDIC processor which consumes 390 LUTs on VIRTEX 4 FPGA [3].

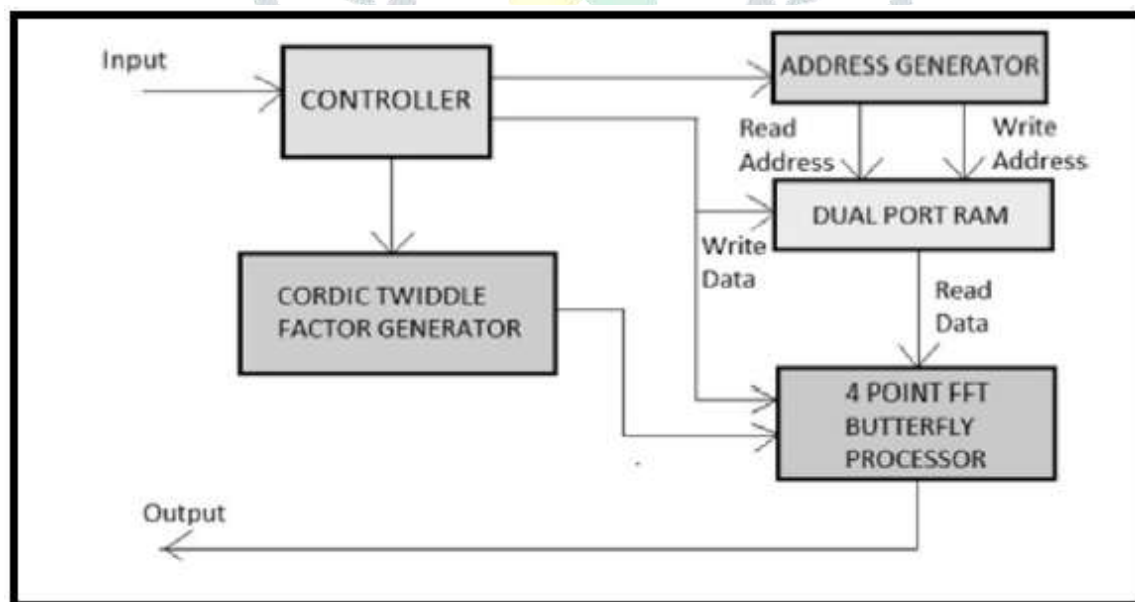


Figure 4. CORDIC based FFT Architecture [3]

**4. Dual Fixed Point CORDIC** - Dual Fixed Point CORDIC, that provides a compromise between Fixed Point and Floating Point CORDIC hardware implementations. A fully parameterized hardware is presented that allows for extensive exploration of the resources-accuracy design space, from which we generate optimal (in the multi-objective sense) realizations. Using DFX they are try to improve the accuracy. The Comparison of floating points, fixed points and dual fixed points are show in figure 5 [4].

# ACCURACY IMPROVEMENT

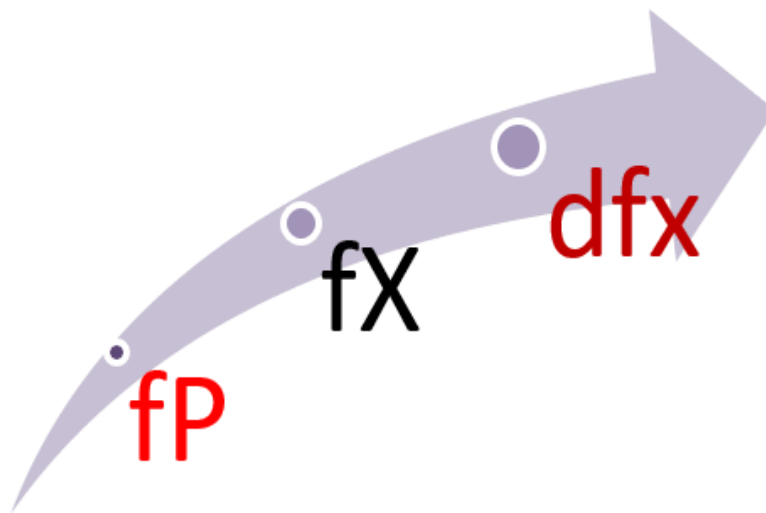


Figure 5. Comparison of floating points, fixed points and dual fixed points [4]

**III. CONCLUSION** – From above techniques, we have observe that number of algorithm and technique available for calculating triangular calculation in space and seas but still it's quite degrading performs in terms of time delay and speed. We have to find a solution of CORDIC design effective mechanism/algorithm to overcome this issue.

## REFERENCES

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