A VHDL based Analog Capture Circuit and DAC for Spartan-3E FPGA

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Abstract - In this paper a VHDL based design of Analog Capture Circuit and DAC, present on a Spartan-3E FPGA board. It has been carried out and tested using oscilloscope and function generator. A VHDL (VHSIC Hardware Description Language) code has been designed based on finite state machine for amplifier, ADC and DAC, implemented on Spatan-3E FPGA Starter Kit board and tested.

Index Terms - Sparta-3E FPGA; Analog Capture Circuit; ADC; DAC; VHDL; Lock-In amplifier

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I. INTRODUCTION - Several experiments in the advanced laboratory require an accurate measurement of a slowly varying, extremely small voltage. Lock-in detection is a powerful technique to recover such a signal, even in the presence of broadband noise whose magnitude is several times greater than the signal itself. Lock-In amplifier (LIA) use Phase Sensitive Detection (PSD) technique to reject undesired signals.

The PSD can be done using either analog or digital methods. The analog form uses an analog multiplier to make a convolution process that is one of the most expensive elements. The better the precision and quality of the multiplication operation required, the more hardware requirements there are and the higher the cost becomes. On the other hand, the digital process uses a discrete multiplier to perform the convolution operation, which is cheaper when compared to the analog multiplier [7]. FPGA has strong flexibility, can be programmed, and debugged, can be fully developed and verified. So, lock-in amplifier can implement on the FPGA platform.

A signal which is given to the Lock-In amplifier input is an analog signal. We can use to convert it into digital form and get back as analog using Analog Capture Circuit and DAC of Spartan-3E FPGA board. The Spartan-3E FPGA Starter Kit board have analog capture circuit consists of a Linear Technology LTC6912-1 programmable preamplifier for scaling of the incoming analog signal, Linear Technology LTC1407A-1 14-bit ADC and Linear Technology LTC2624 quad DAC with 12-bit unsigned resolution. The amplifier, ADC and DAC are serially programmed or controlled by the FPGA [3]. Programmable preamplifier has two inputs VINA and VINB and the output of the preamplifier is connected to ADC. They are very useful to apply and test the DSP algorithms which are executed inside the Spartan-3E FPGA [3].

W.I. Zidan, A. Radi , and H.I. Khedr, A.G. Mostafa control of Analog Capture Circuit and DAC of Spatan-3E FPGA Starter Kit board using finite state machine for each component [3]. Husnain Al Bustam, Mohammad Shahzamal represents a VHDL based design of DAC, present on a Spartan-3E starter kit [4]. Istiyanto, J.E carried out and tested a VHDL design of a controller for the amplifier and ADC present on a Spartan-3E Starter Kit board [5].

II. DESIGN AND IMPLEMENTATION - Figure given below shows the block diagram of programmable pre-amplifier, ADC, DAC and their signal with Spartan 3E FPGA.

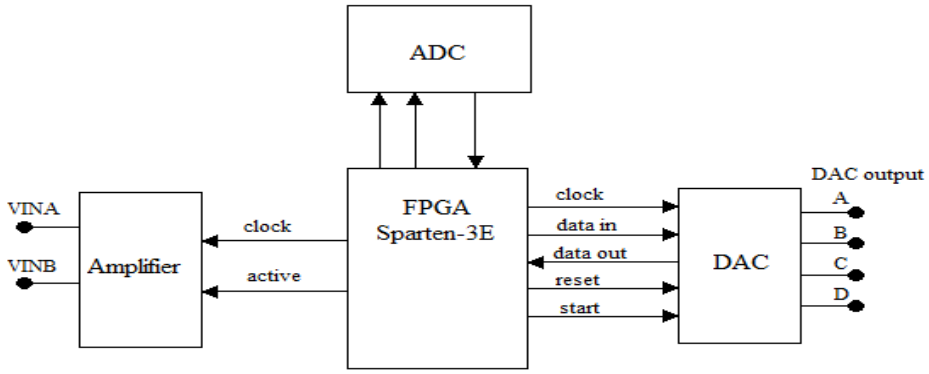

Figure 1. Block diagram of amplifier, ADC, DAC [3]

Analog signals presented on the VINA or VINB inputs are amplified relative to 1.65V. The 1.65V reference is generated using a voltage divider of the 3.3V voltage supply. The gain of each amplifier is programmable from -1 to -100 the maximum range of the ADC is ±1.25V which is centered on 1.65 V (reference). The gain of each amplifier is programmable according the input voltage range [1]. Table 1 shows Programmable gain setting for pre-amplifier.

Gain	A3	A2	A1	A0	Input voltage range	
	B3	B2	B1	B0	minimum	Maximum
0	0	0	0	0		
-1	0	0	0	1	0.4	2.9
-2	0	0	1	0	1.025	2.275

-5	0	0	1	1	1.4	1.9
-10	0	1	0	0	1.525	1.775
-20	0	1	0	1	1.5875	1.7125
-50	0	1	1	0	1.625	1.675
-100	0	1	1	1	1.6375	1.6625

Table 1 Programmable gain setting for pre-amplifier

To control amplifier, ADC and DAC a VHDL code is designed with states and different process. VHDL is used to program FPGA. Table 2 lists the interface signals between the amplifier, ADC, DAC and FPGA. Figure shows State condition for coding. Figure 3 shows the Schematic diagram of amplifier, ADC, DAC their interface with Spartan 3E FPGA.

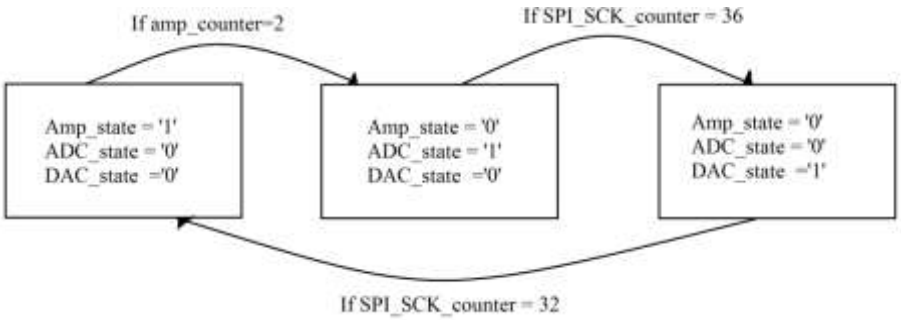

Figure 2. State condition for coding

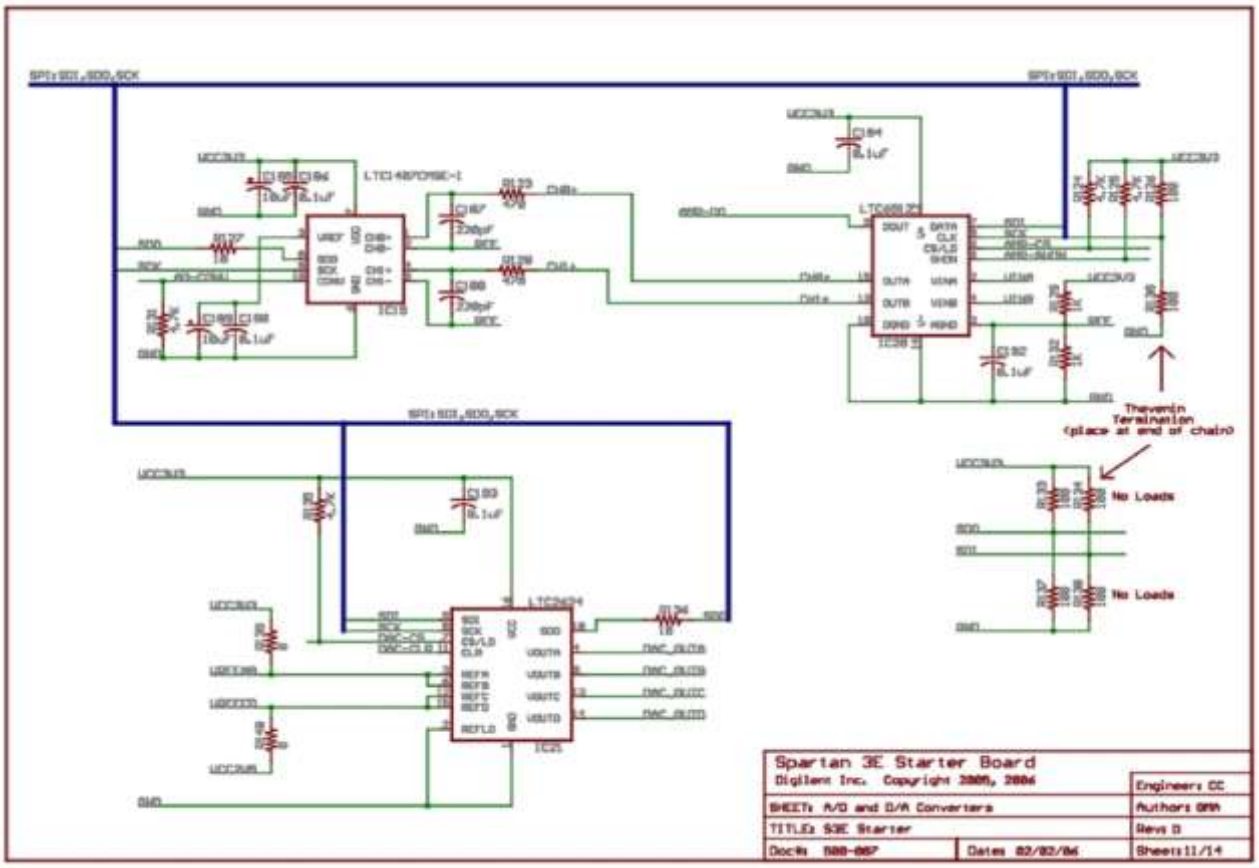

Figure 3. Schematic of amplifier, ADC and DAC [1]

Signal	FPGA Pin	Direction	Description
SPI_MOSI	T4	FPGA→AD FPGA→DAC	Serial data: Master Output, Slave Input
AMP_CS	N7	FPGA→AMP	Active-Low chip-select. The amplifier gain is set when signal returns High
SPI_SCK	U16	FPGA→AMP FPGA→ADC FPGA→DAC	Clock
AMP_SHDN	P7	FPGA→AMP	Active-High shutdown, reset
AD_CONV	P11	FPGA→ADC	Active-High shutdown and reset

SPI_MISO	N10	FPGA←ADC	Serial data: Master Input, Serial Output. Presents the digital representation of the sample analog values as two 14-bit two's complement binary values
		FPGA←DAC	Serial data: Master Input, Slave Output
DAC_CS	N8	FPGA→DAC	Active-Low chip-select. Digital-to-analog conversion starts when signal returns High.
DAC_CLR	P8	FPGA→DAC	Asynchronous, active-Low reset input

Table 2. Amplifier, ADC and DAC interface signals with FPGA

III. VERIFICATION AND RESULTS - VHDL code of Analog Capture Circuit and DAC code has been implemented directly into the Spartan-3E starter kit board using USB cable. Xilinx ISE 14.5 software has been used for synthesizing and implementation on the FPGA. After configuration FPGA was checked by applying well characterized signals to the input of the amplifier from function generator and recognizing their corresponding output signals of the DAC in oscilloscope. Here, inputs were connected to the VINA and VINB of the board. Figure 4 shows the Experimental Setup.

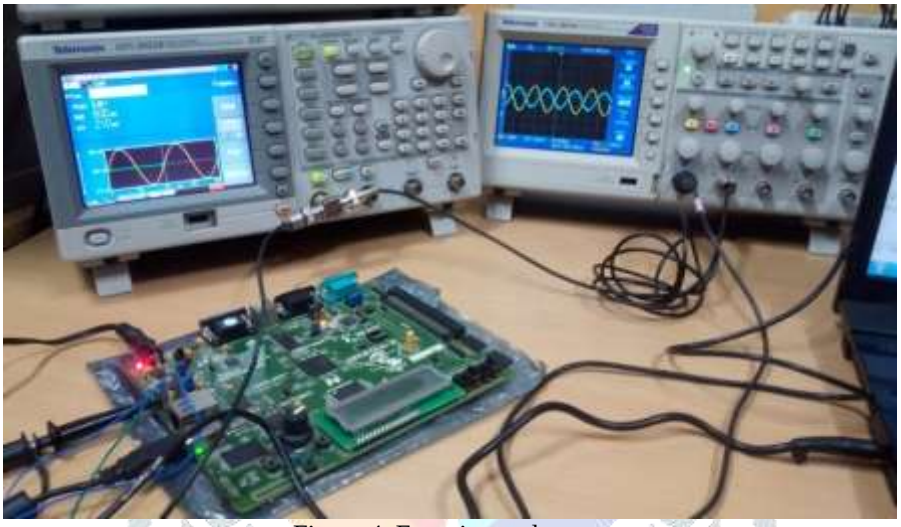

Figure 4. Experimental setup

To get maximum voltage range that can be sampled, gain of the amplifier is set to -1(by transferred "00010001"this value to the programmable preamplifier) which gives 0.4 - 2.9 V voltage range; the offset of the signals needed to adjust to 1.65V. Figure 5 shows the obtained results of the amplifier input against DAC output for recommended value.

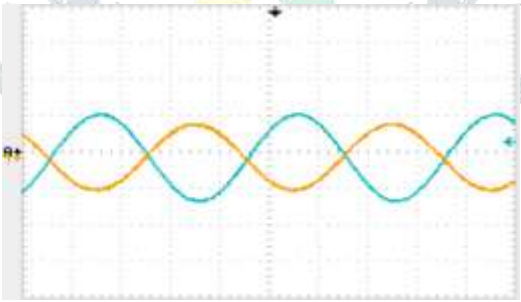

Figure 5. Result of the amplifier input against DAC output

As per expectation, the output signal of DAC was matched with the input signal of the amplifier. In waveforms we can see the 180 degree phase shift with some delay and difference in amplitude. Phase come because the output of the ADC is in 2's compliment form. The difference in amplitude is caused due to the differences in both the gain of amplifier and the number of bits of 14-bit ADC and 12-bit DAC as well as the capturing time of the input and output signal i.e. the output signal should be delayed than the input signal because it takes few micro seconds to be generated by DAC [3].

Change in offset and amplitude values in order to be beyond the recommended values (offset=1.65V, amplitude = ±1.25V) gives change (distortion) in output. Below figure shows the obtained results of t DAC output after increasing the offset to be (2.8V) and decreasing the offset value to be (0.5V), respectively.

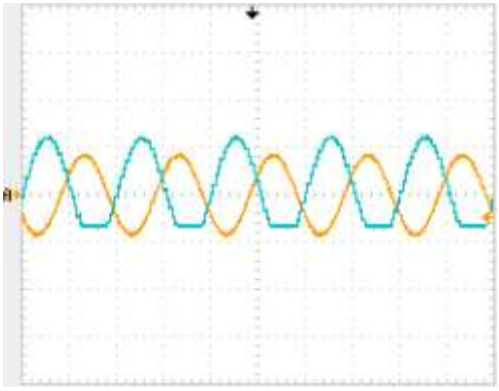

Figure 6. Results of the amplifier input against DAC output when decreasing offset value

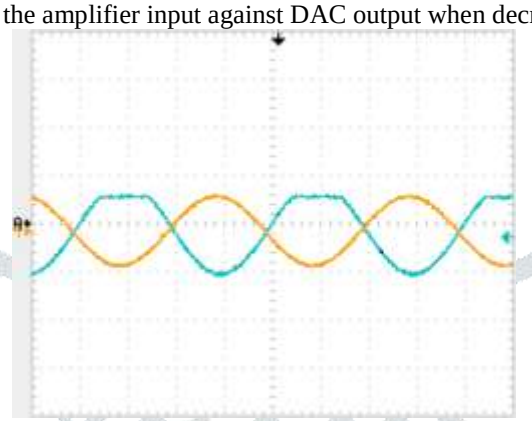

Figure 7. Results of the amplifier input against DAC output when increasing offset value

Below figure shows the bus components AD_CONV, SPI_MISO and SPI_SCK from DAC respectively.

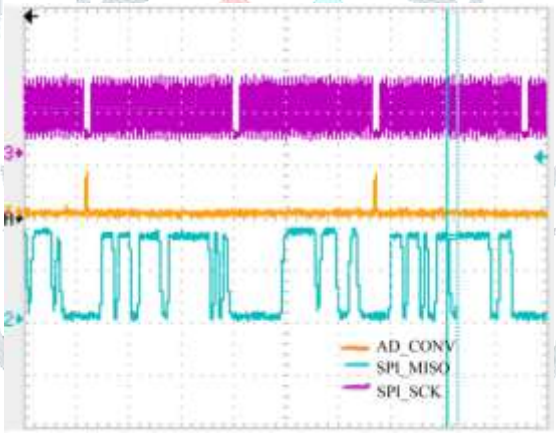

Figure 8. AD_CONV, SPI_MISO and SPI_SCK from DAC

IV. CONCLUSION - This paper represents the controlling of on board amplifier, ADC and DAC of Spartan-3E FPGA Starter Kit. The results of the implemented VHDL code on Spartan-3E FPGA Starter Kit properly interfaced with real world signal which are in between 0.4 to 2.9V.

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