DESIGN AMBA BASED AHB TO APB BRIDGE USING VERILOG HDL

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Abstract—The purpose of this project is to design and verify of AMBA based AHB to AHP bridge. AHB2APB Bridge is a complex interface between Advance high performance bus (AHB) and Advance peripheral bus (APB) .AHB2APB Bridge will be communicate between low bandwidth peripheral on APB with high bandwidth ARM processors and high speed device on (AHB). So, there will be no data loss between AHB to APB or APB to AHB data transfers.

Index Terms— AMBA bus, AHB bus, APB bus, SOC

I. INTRODUCTION

The Advance microcontroller bus Architecture(AMBA) are standard for on chip bus architecture .On chip bus architecture plat a very important role in SOC system. The AMBA is used to interconnect the component of module .It will maintain the intercommunication of functional blocks on system on chip[1]. The AMBA will provide a efficient way to interconnect the components and increase the performance of the system. AMBA have an advantage that it is open specification.

The Advanced Microcontroller Bus Architecture protocol describes number of buses and interfaces. In its first version which Introduced in 1996 by ARM were advance system bus and in its second version 2 in 1999, it defines AMBA 2.0, which is a high performance bus. Advance high performance bus is a signal clock edge protocol. In 2003, ARM introduced its third generation version AMBA 3.0 which includes AXI[6]. The first version of AMBA contains only one peripheral bus with two system bus.

Three bus specifications are there in AMBA as follow-

1. Advanced High- Performance Bus (AHB).
2. Advanced System Bus (ASB).
3. Advanced Peripheral Bus (APB).

1.1 Advance high Performance bus (AHB)

In 1999 ARM introduced second version AMBA 2.0, which is a high performance bus and synthesizable design .AHB has high bandwidth, which makes a best choice among a APB and ASB. AHB is high performance and high clock frequency system module[8]. This bus provide high bandwidth interface between the Elements of transfer. AHB support multiple masters and provide high bandwidth performance. The AHB bus acts as a high performance systembackbone[1].

The AHB bus support interconnection between high performance ARM processor, high bandwidth on chip RAM, high bandwidth external memory interface and DMA bus. There is a bridge between high performance bus (AHB) and low bandwidth peripheral bus (APB) for efferent data transfer.

1.2. The Advance System Bus (ASB)

The First Version of AMBA introduced Advance System Bus in 1996. The AMBA based ASB is for high frequency system modules.ASB is system bus which is suitable for use where the high-performance features of AHB are not required. ASB also supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheralfunctions[6].

1.3 The Advance Peripheral Bus (APB)

ARM introduced second version in 1999, it defines AMBA 2.0, which is a high performance bus. The APB is low power consumption and low frequency system module[7]. The APB reduces complexity for interfacing with peripheral. APB can be used for small area and less power with either version of the system. The APB protocol is the bus protocol employed for the peripherals like UART, Keypad, PIO, Timer, LCD Display or LED display etc.

2 AHB to APB Bridge

AHB2APB Bridge is a interface between Advance high performance bus (AHB) and Advance peripheral bus (APB) .Bridge provide communication between low frequency peripheral on APB with high frequency and high speed device on (AHB).Bridge provide efficient data a transfer from AHB to APB[6]. So, there is no data loss between AHB to or from APB during data transmission. Here, Handshaking Signaling method will use to transfer data between AHB and APB[1].

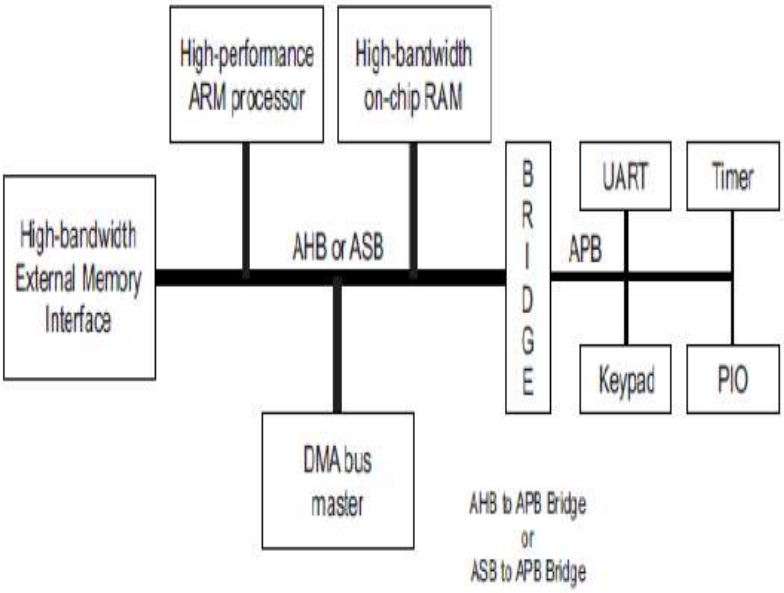

Figure 2.1: AMBA Architecture[3]

Bridge FSM is used to transmit data from AHB to APB.AHB will send valid address and write data to APB .The address, control and data from AHB will control the peripheral of APB. If valid is high write signal is low of AHB then read transfer is perform. Write transfer is perform from AHB to APB and read transfer is perform from APB to AHB[2]. When valid and write both signal is high then write transfer is perform. Read and Write transfer is complete in two cycles and enable signal will assert at second cycle and drive low at thirdcycle[6]. Pipeling structure is to transmit data because APB is slow to transmit data, So AHB has to wait for APB to complete the transfer. For burst transfer wait state is used in write transfer[6].

3. Architecture of AHB to APB Bridge

The Architecture of AHB to APB is given on the Figure 3.1. As shown in figure 3.1 architecture has three modules. In this Architecture data will transfer from APB master to AHB slave Bridge. FSM is used for interface between low bandwidth APB and high bandwidth AHB. Pipelining structure is use in FSM to transfer data from APB to AHB.A wait state is use transfer data to or from APB ,because APB has low bandwidth so its transfer speed is slow, so AHB need to wait until APB complete the read or write transfer[6].

In AMBA based AHB master will initialize the operation by sending address and control signal to AHB Slave. After that AHB Slave will send read and write data to AHB master as per the address and control given by AHB slave. Then AHB master will send Hready signal to AHB slave, which indicate that transfer has done[2].

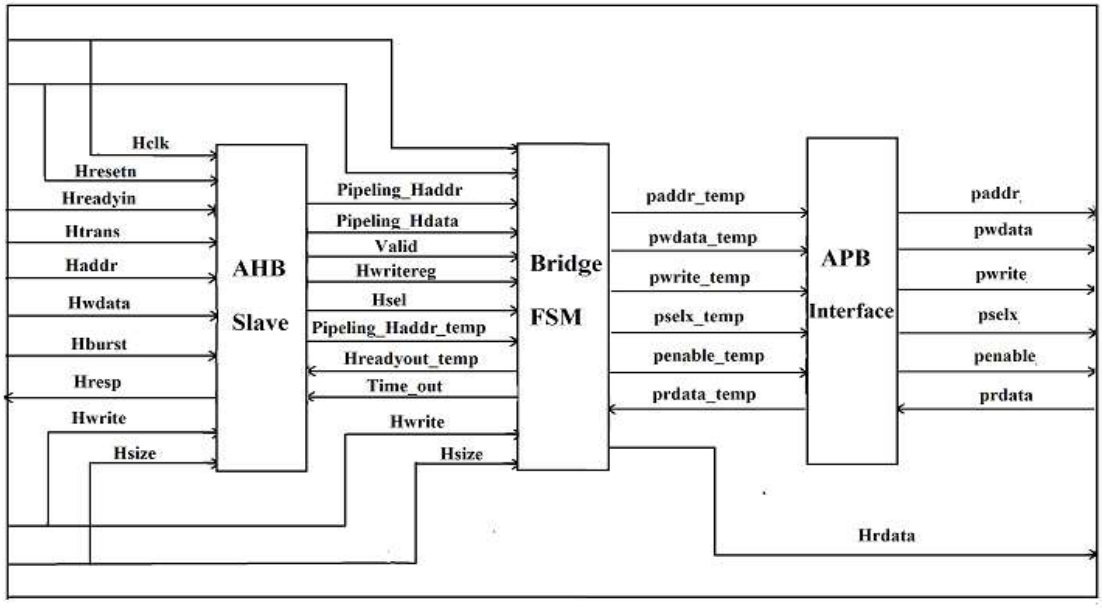

Figure 3.1:. Architecture of AHB to APB Bridge

To solve the existing problem a time counter is used in APB interface. When AHB master is failed to send Hready signal , after some time timer counter signal will drive high and APB interface can start another transfer or resend the read data to AHB slave, this will increase the performance of the system.

4. State Machine of AHB to APB

AHB to APB Bridge FSM is use for communication between AHB protocol and APB Protocol. The State machine of AHB to APB Bridge FSM is shown in Fig 4.1.AHB to APB bridge State machine has 8 states. Description of all the stage is given below.

FSM is used for interface between low bandwidth APB and high bandwidth AHB. Pipelining structure is use in FSM to transfer data from APB to AHB.A wait state is use transfer data to or from APB ,because APB has low bandwidth so its transfer speed is slow, so AHB need to wait until APB complete the read or write transfer[6].

ST_IDLE:

IN this state APB buses and Pwrite will hold the last value they had and Pselx and PENABLE will be low.

The ST_IDLE state is entered from:

- This state is entered when Hresetn is zero.
- When there is no peripheral to perform ST_IDLE state is entered from ST_RENABLE,ST_WENABLE,ST_IDLE.

The next state:

- ST_READ: for a read transfer, when AHB contains valid APB read transfer
- ST_WWAIT: for write transfer, when AHB contains valid APB write transfer.

ST_READ:

In this state address is decoded and Haddr is driven in Paddr and Pselx line is driven high and Pwrite is driven low. In this state data is read from APB to AHB.A wait state is use ensure AHB read data transfer do not complete until APB drives read data on Hrdata
The ST_READ state entered from ST_IDLE, ST_RENABLE, ST_WENABLE, when read transfer has to perform.

The next state is always ST_RENABLE

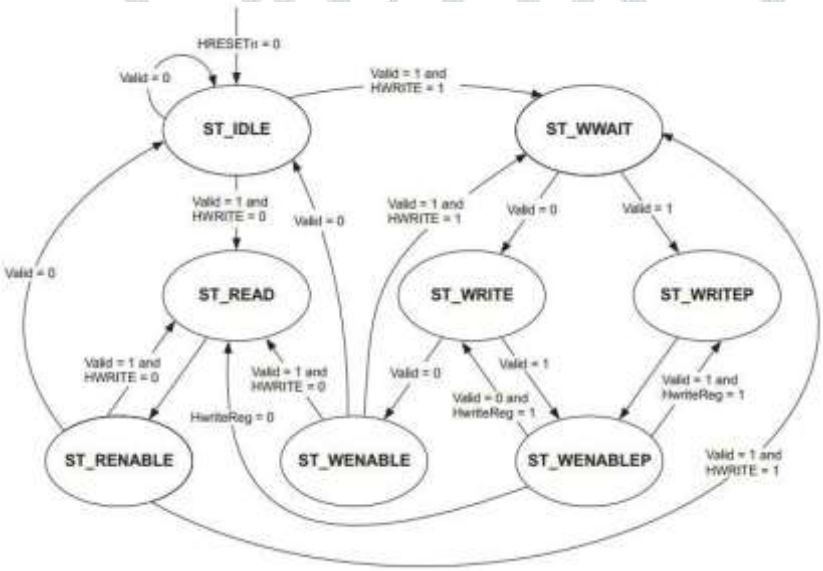

Figure 4.1: State machine of AHB to APB[6]

ST_WWAIT:

The wait state is use for Pipeling structure of AHB transfer, to allow to complete AHB write data transfer so that write data is driven on a Hwdata. The APB write transfer is start in next cycle after write data is driven in Hwdata.

The ST_WWAIT state is entered from ST_IDLE, ST_RENABLE, ST_WENABLE, when write transfer is need to perform.

The next state is always ST_WRITE.

ST_WRITE:

In this state address is decoded and Haddr is driven in Paddr and Pselx line and Pwrite line driven high. Single transfer is done in ST_WRITE

The ST_WRITE state is entered from:

- ST_IDLE: when there are no more peripheral to perform the transfer.
- ST_WENABLEP: when there are no more peripheral to perform the transfer and current pending transfer is write.

The next state:

- ST_WENABLE: When there are no more peripheral to perform the transfer.
- ST_WENABLEP: When there are one more peripheral to perform the transfer.

ST_WRITEP:
In this state address is decoded and Haddr is driven in Paddr and Pselx line and Pwrite is driven high. More than one transfer is done in ST_WRITEP state. A wait state is use because AHB bandwidth is high and APB bandwidth is low so there will be always one pending transfer between current AHB peripheral transfer and current APB peripheral transfer.

ST_RENABLE:
In this state Penable is driven high and it will enable the read transfer of APB

5 .Implementation and Result

- Waveform of top module of AHB to APB bridge is shown in figure 5.1

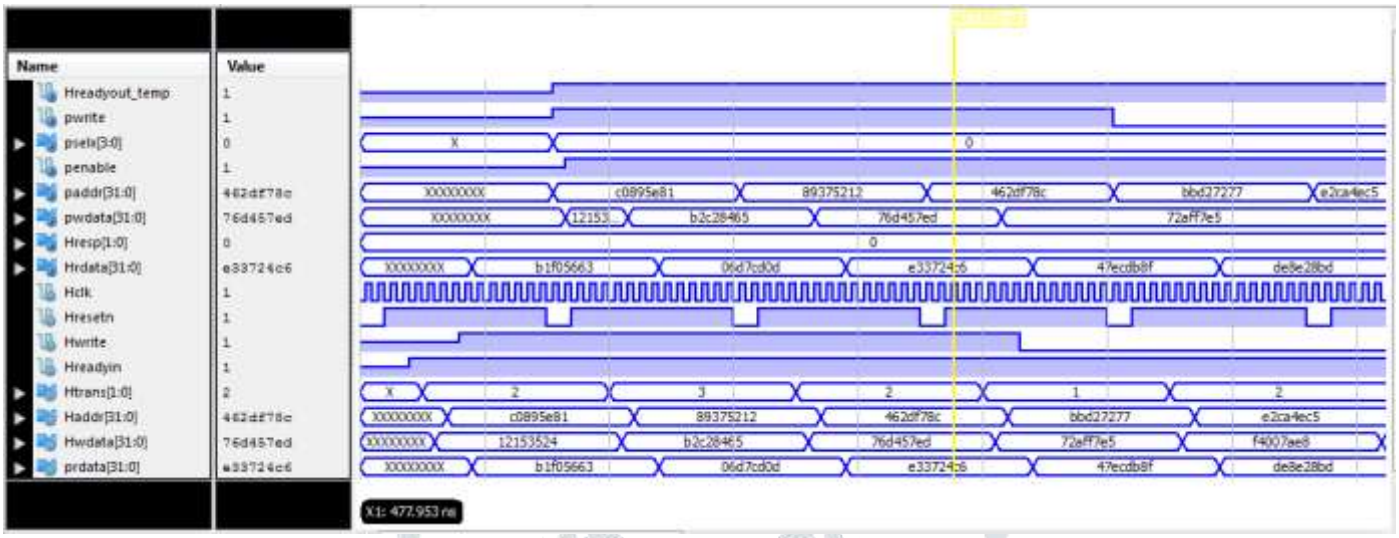

Figure 5.1 Simulation result of AHB to APB top module

- Waveform of AHB slave is shown in figure 5.2

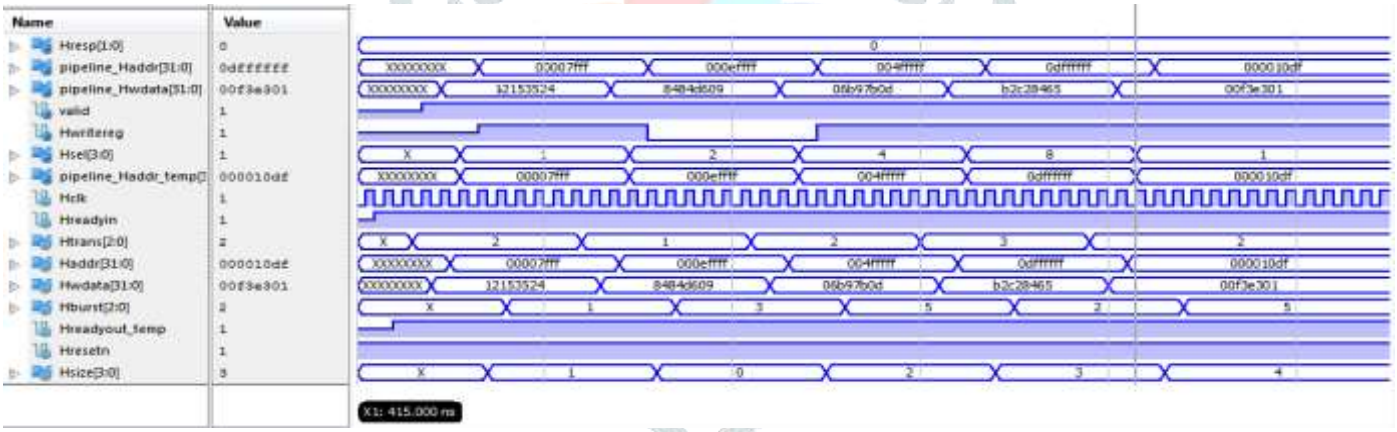

Figure 5.3 Simulation result of AHB_slave

- Waveform of AHB to APB bridge fsm is shown in figure 5.3

Figure 5.3 Simulation result of AHB to APB bridge fsm

- Waveform APB interface is shown in figure 5.4

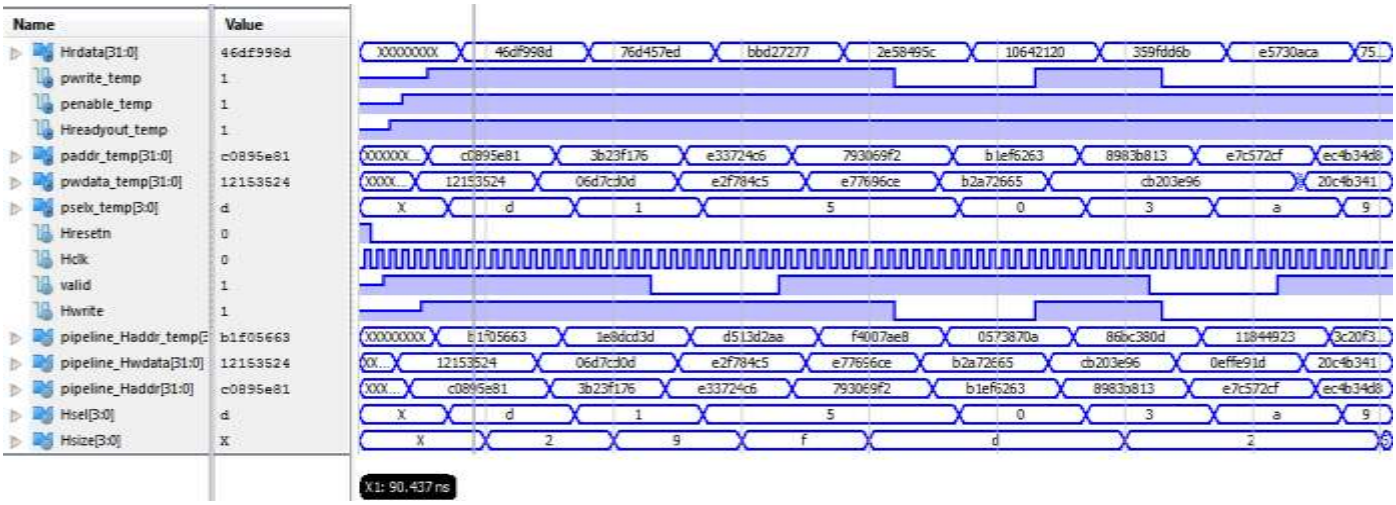

Figure 5.4 Simulation result of AHB to APB bridge fsm

6. Acknowledgement

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7. Conclusion.

The implemented communication bridge between AHB and APB was designed and implemented in Xilinx ISE 14.1, spectrum 6, using Verilog HDL .The design topmodule of AHB2APB bridge is completed successfully. The design AHB slave, AHB2APB bridge FSM and APB interface is completed successfully.

8. References

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