DETECT THE PERMANENT FAULTS IN FIFO OF NOC ROUTERS USING SINGLE ADDRESS

1. P. PUSHPALATHA, 2. SK.JABIDA
1. ASSISTANT PROFESSOR, Dept. of ECE, JNTUK UCEK, KAKINADA, A.P
2. M. Tech Student, Dept. of ECE, JNTUK UCEK, KAKINADA, A.P

ABSTRACT:
The on line transparent test technique for detection of latent hard faults which develop in first input first output buffers of routers during field operation of NOC and also propose fault tolerant solution by introducing shared buffer in router. It provides alternative way in case of detection of faults otherwise used to improve efficiency. The technique involves repeating tests periodically to prevent accumulation of faults. NOC approach has emerged as a promising solution for on chip communications. This proposes an on line transparent test technique for detection of latent hard faults which develop in first input first output buffers of routers during field operation of NOC. The technique involves repeating tests periodically to prevent accumulation of faults. Further this project can be enhanced by using clock skewing technique. Time optimization is main criteria in this enhancement. Modified ring counter decrease total combinational path delay for improved memory organization.

KEYWORDS: Network On Chip (NOC), First in First Out (FIFO), Built in Self Test (BIST), Dynamic Random Access Memory (DRAM), Clock skewing, Modified ring counter.

INTRODUCTION:
Over the last decade, network-on-chip (NoC) has emerged as a better communication infrastructure compared with bus-based communication network for complex chip designs overcoming the difficulties related to bandwidth, signal integrity, and power dissipation [1]. However, like all other systems-on-a-chip
(SoCs), NoC-based SoCs must also be tested for defects. Testing the elements of the NoC infrastructure involves testing routers and interrouter links. Significant amount of area of the NoC data transport medium is occupied by routers, which is predominantly occupied by FIFO buffers and routing logic. Accordingly, the probabilities of run-time faults or defects occurring in buffers and logic are significantly higher compared with the other components of the NoC. Thus, test process for the NoC infrastructure must begin with test of buffers and routing logic of the routers. In addition, the test must be performed periodically to ensure that no fault gets accumulated. The occasional run-time functional faults have been one of the major concerns during testing of deeply scaled CMOS-based memories.

These faults are a result of physical effects, such as environmental susceptibility, aging, and low supply voltage and hence are intermittent (nonpermanent indicating
device damage or malfunction) in nature [2]. However, these intermittent faults usually exhibit a relatively high occurrence rate and eventually tend to become permanent [2]. Moreover, wear-out of memories also cause intermittent faults to become frequent enough to be classified as permanent. Thus, there is a need for online test technique that can detect the run-time faults, which are intermittent in nature but gradually become permanent over time. Chip integration has reached a stage where a complete system can be placed in a single chip. When we say complete system, we mean all the required ingredients that make up a specialized kind of application on a single silico n substrate. This integration has been made possible because of the rapid developments in the field of VLSI designs. This is primarily used in embedded systems. Thus, in simple terms a SoCcan be defined as “an IC, designed by stitching together multiple s Tand -alone

VLSI designs to provide full functionality for an application.” A NoC is perceived as a collection of computational, storage and I/O resources on -

chip that are connected with each other via a network of routers or switches instead of being con nected with point to point wires. These resources communicate with each other using data packets that are routed through the networkin the same manner as is done in traditional networks. It is clear from the definition that we need toemployhighly sophis ticated and researched methodologies from traditional computer networks and implement themon chip.we have to explore the motivating factors that are compelling the researchers and designers to move toward the adoption of NoC architectures for future SoCs. The area of NoC is still in its infancy, which is one of the reasons why there are various names for the same thing; some call it on chip networks, some networks on silicon, but the majority agrees upon "Networks on Chips" (NoCs). However, we will be using these terminologies interchangeably throughout our tutorial.NOC is Integrating various processors and on chip memories into a single chip .Faults occur in NOC

- Permanent faults
- Transient fault

NETWORK-ON-CHIP BASED MEMORY BIST:

The problem of optimized test power and test time at reduced area overhead during test of embedded memories in SoCs have been tackled separately by previous approaches found in literature. However, there are no system-level solutions for the same in case of memories interconnected using NOC. In this respect, this thesis focuses on providing a system level solution for test of NOC based memory cores utilizing NoC as TAM and targeting optimization of test power, test time and reduced DFT area overhead.

DISTRIBUTED AND HYBRID TEST ARCHITECTURE :

A distributed MBIST architecture has been proposed for testing heterogeneous memory cores interconnected using NoC. In the proposed architecture, the memory cores formdifferent groups based on distance and timing constraints. Each group has a dedicated BIST controller which performs parallel March test on all the cores in a group. The groupsare tested in a pipeline fashion. The NoC is re-used to act as TAM for delivering test instructions to the BIST controllers. The hybrid test technique and the distributed BIST architecture allows the test of memory cores to be performed at much lesser time than required in [59]. The proposed architecture is an improvement on similar architectures found in literature as it allows test of memory cores of any size while others had allowed only test of homogeneous memory cores. Utilizing a distributed BIST architecture leads to less area overhead than dedicated BIST for each core.

SRAM OPERATION:

The basic architecture of a static RAM is shown in Figure 2.1. A location of a SRAM can be randomly accessed for read/write by inputing the address of the corresponding location. Each address is linked to a particular data input/output pin. The architecture of the SRAM includes a rectangular array of memory cells in rows (word-lines) and columns (bit-lines) and additional circuits for arranged decoding addresses and implementing read and write operations. A memory cell is a bistable flip-flop made up of four to six transistors. The flip-flop may be in either of two states that can be interpreted by the support circuitry to be a 1 or a 0. Each memory cell has a unique location or address defined by the intersection of a row and column.

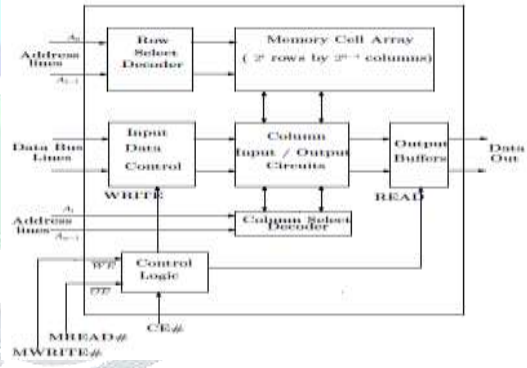
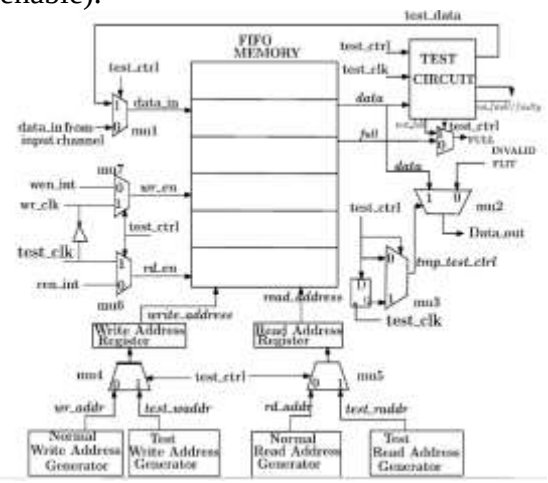


Figure : Basic Architecture of SRAM

The address of a memory location comprises of two parts. The first part is the row address (A0 to Ai□1 lines shown in Figure, which selects one row/word-line. The second part,(Ai to An□1 lines shown in Figure) is the column address which selects one bit out of all the bits of the word activated during the word-line selection. Since row and column addresses are not required at the same time, they can be multiplexed on the same address lines. Theread/write operations are controlled by the Control logic as shown in Figure. The chip select enable(CE#) is an additional input signal required to activate the chip. Two more control input pins exist on the

chip, the WE#(write enable) and the OE#(output enable).



FIFO BASED SYSTEM:

TRANSPARENT TEST GENERATION: The faults considered in this brief, if applied for SRAMs or DRAMs, can be detected using standard March tests. However, if the same set of faults are considered for SRAM type FIFOs, March test cannot be used directly due to the address rest riction in SRAM type FIFOs mentioned in and thus we were motivated to choose single order address MATS ++ test (SOA MATS ++) for the detection of faults considered in this brief. The word oriented SOA MATS ++ test is represented as {_ (wa) ; ↑ (ra,wb) ; ↓ (rb, wa) }; _ (ra) } where, a is the data background and b is the complement of the data background. ↑ and ↓ are increasing and decreasing addressing order of memory, respectively. _ means memory addressing can be increasing or decreasing. Application of SOA MATS ++ test to the FIFO involves writing patterns into the FIFO memory and reading them back. As a result, the memory contents are destroyed. However, online memory test techniques require the restoration of the memory contents after test. Thus, researchers ha ve modified the March tests to transparent March test so that tests can be performed without the requirement of external data background and the memorycontents can be restored after test. We have thus transformed the SOA MATS ++ test to transparent SOA MAT S ++ (TSOA MATS ++) test that can be applied for online test of FIFO buffers. The transparent SOA MATS ++ test generated is represented as {↑ (rx,w $\bar{}$ x, r $\bar{}$ x,wx, rx) } . The transparent SOA MATS ++ algorithm is intended for test of stuck at fault, transient faul t, and read stuck at fault, transition fault, and read disturb fault tests developed during field operation of FIFO memories. The fault coverage of the algorithm is shown in Fig. 2 . In both the figures, the word size of FIFO memory is assumed to be of 4 b its. As shown in Fig. 2 ,assume the data word present in LUT be 1010.The test cycles begin with the invert phase (memory address pointer j with 0 value) during which the content of location addressed is read into temp and then backed up in the original . Th e data written back to SOA MATS ++ test. LUT is the complement of content of temp . Thus, at the end of the cycle, the data present in temp and original is 1010, while lut contains 0101.Assume a stuck - At 1 fault at the most significant bit (MSB) position of t he word stored in LUT . Thus, instead of storing 0101, it actually stores 1101 and as a result, the stuck At fault at the MSB gets excited. During the second iteration of j , when lut is readdressed, the data read into temp is 1101. At this point, the data p resent in temp and \ original are compared (bitwise XOR ed). An all 1's pattern is expected as result. Any 0 within the pattern would mean a stuck at fault at that bit position.

MEMORY ORGANIZATION:

The buffer is adaptive, that is it continuously learns the optimal delay to be applied to the audio flow at run-time. Once the optimal delay has been learned, the delay buffer will apply this delay to the audio flow, expanding or shrinking the audio samples as necessary when the actual audio samples in the buffer are too low or too high.

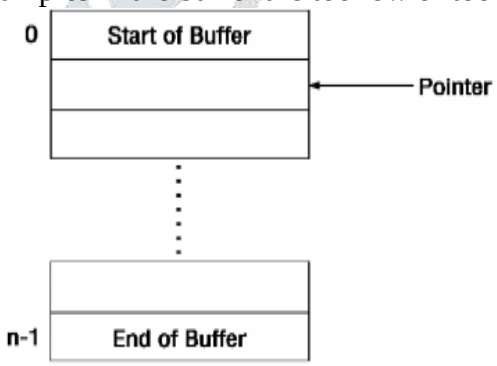


Fig : Buffer

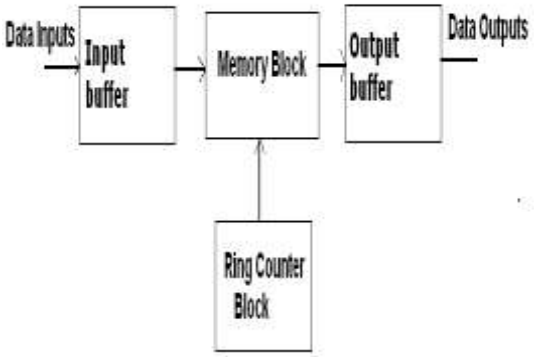
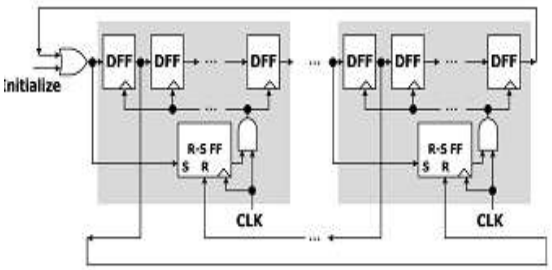


Fig: Basic RAM Design

RING COUNTER:

A **ring counter** is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register.

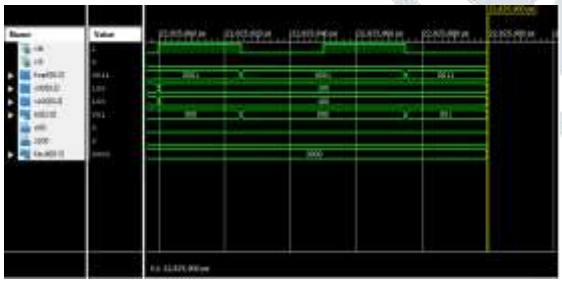


: Ring Counter With SR Flip-Flops

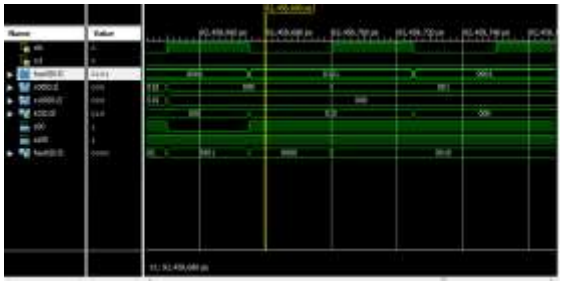
The above block diagram shows the power controlled Ring counter.First, total block is devided into two blocks. Each block is having one SR FLIPFLOP controller

RESULT:

WAVE FORM WITHOUT FAULT

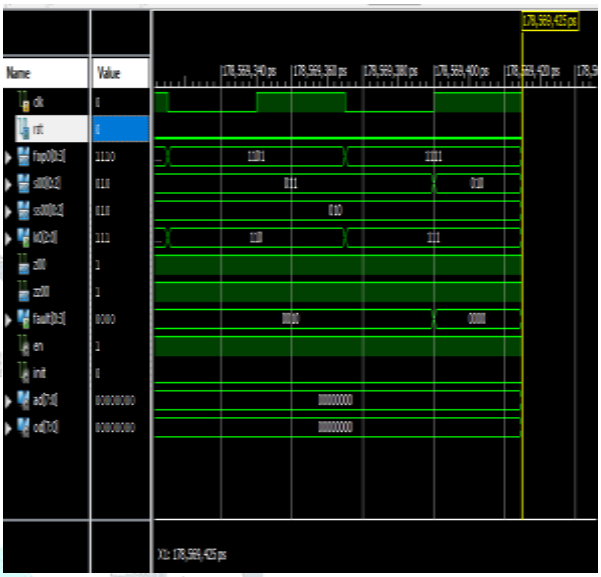


WAVE FORM WITH FAULT



USINR RING COUNTER WITHOUT FAULT

USING RING COUNTER WITH FAULT



PARAMETERS

S.No	Comparsion	Time	delay	power
1	Existing	5.5ns	8.6ns	82.1uw
2	proposed	2.5ns	2.7ns	96.4uw

CONCLUSION:

The focus of the thesis has been to devise improved test techniques for NoC based memory systems which include SRAM or DRAM cores interconnected using NoC and FIFO buffers which are present within the routers of the NoC infrastructure. The objective of the presented work has been to find the research gap in the existing works related to the topic and bring about improvements in them by reducing the test cost. The test cost estimation has been done in terms of area overhead, test time and power dissipation during test.

REFERENCES:

[1] On-Chip Networks Bibliography. http://www.cl.cam.ac.uk/_rdm34/onChipNetBib/ browser.htm#Jantsch:2003:NOC. Accessed: 2014-05-30.

[2] Various Methods of DRAM Refresh. In Technical Note TN-04-30. Micron Technology, Inc., 1999.
[3] R. D. Adams. High Performance Memory Testing: Design Principles, Fault Modeling and Self Test. New York, USA, 2002.
[4] R. Aitken. A Modular Wrapper Enabling High Speed BIST and Repair for Small Wide Memories. In Proceedings of International Test Conference, pages 997 – 1005, October 2004.
[5] A. M. Amory, C. Lazzari, M. Lubaszewski, and F. G. Moraes. A New Test Scheduling Algorithm Based on Networks-on-Chip as Test Access Mechanisms. Journal of Parallel Distributed Computing, 71(5):675–686, 2011.
[6] S. Bahl and V. Srivastava. Self-Programmable Shared BIST for Testing Multiple Memories. In 13th European Test Symposium (ETS), pages 91 –96, May 2008.
[7] S. Barbagallo, M. L. Bodoni, D. Medina, G. de Blasio, M. Ferloni, F. Fummi, and D. Sciuto. A Parametric Design of a Built-in Self-Test FIFO Embedded Memory. In Proceedings of the Workshop on Defect and Fault-Tolerance in VLSI Systems (DFT '96), pages 221–229, 1996.
[8] L. Benini and G. D. Micheli. Chapter 1 - Networks on Chip. In Networks on Chips, pages 1 – 22. Morgan Kaufmann, San Francisco, 2006.
[9] A. Benso, S. Di Carlo, G. Di Natale, P. Prinetto, and M. Bodoni. Programmable Built-in Self-Testing of Embedded RAM Clusters in System-on-Chip Architectures. Communications Magazine, IEEE, 41(9):90 – 97, September 2003.
[10] P. Bernardi, M. Grosso, M. Reorda, and Y. Zhang. A Programmable BIST for DRAM Testing and Diagnosis. In Proceedings of International Test Conference, pages 1 –10, November 2010.
[11] A. Bondavalli, S. Chiaradonna, F. D. Giandomenico, and F. Grandoni. Threshold-Based Mechanisms to Discriminate Transient from Intermittent Faults. IEEE Transaction on Computers, 49(3):230–245, 1998.