DESIGN OF MULTIPLE THRESHOLD INVERTER QUANTIZATION BASED FLASH ADC USING CUSTOM LAYOUT TOOLS

Joshua Daniel Raj.J[1] & S.Ramakrishnan[2]
Sr. Asst. Professor[1] & Asst. Professor[2]
EEE Dept., New Horizon College of Engg. Banglore, India[1 & 2]

Abstract

The comparator is the most important component in the ADC architecture. Its role is to convert an input voltage Vin into a logic 1 or 0 by comparing a reference voltage Vref with Vin. If the Vin is greater than Vref the output of the comparator is 1 otherwise 0. Commonly used comparator structure in CMOS ADC design is fully defined latch comparators. The TIQ comparator uses two cascaded CMOS inverters as a comparator for high speed conversion and low power dissipation. The aim of the project is to implement MTIQ comparator in Flash ADC by replacing ordinary comparators. It is possible to achieve higher speed, linearity, accuracy, and high resolution . The project aims to make a TIQ implemented ADCs for less area and power using different compaction algorithms in layout tools like MAGIC/CADENCE.All the power Calculations are done using SPICE/CADENCE Spectre tools.

Key words: Threshold Inverter, ADC, TIQ Comparator

1.INTRODUCTION

The minimum channel length of the transistor will be scaled down to 0.065 um in 2007, according to the roadmap of semiconductors. In addition to this downscaling, today's system-on-chip (SoC) trend forces analog and digital integrated circuits (ICs) to be integrated on a single chip called the complete SoC. At present, there are many demands on the complete SoC in wireless and broadband communications wireless networking (WLAN, voice/data communication, and Bluetooth), wired communication (WAN and LAN), and consumer electronics (DVD, MP3, digital cameras, video games, and so on). Therefore, as one of the mixed- signal ICs, analog-to-digital converters (ADCs) must follow this complete SoC trend. Many challenges exist to make ADCs adaptable for SoC implementation with current mixed-signal technology. The major considerations in designing

ADCs for the complete SoC are high-speed conversion, low-power dissipation, and low-voltage operation.In terms of high-speed conversion, 0.13 um CMOS technology presently allows processor speeds in excess of 2.4 GHz. However, the sampling speed of ADCs fabricated with an advanced BiCMOS process has been around 200 mega samples per second (MSPS) [2]. Recently, Maxim Integrated Products has produced a high-speed ADC with a bipolar process operating up to 1.5 giga samples per second (GSPS) for digital oscilloscopes, digital RF/IF signal processing, direct RF down-conversion, and radar/ECM systems.

This ADC has enough speed for SoC implementation, but the price is too high because it uses bipolar solid-state technology. Both cost and high-speed conversion are limitations of the complete SoC. Accordingly, to remove the speed gap between a processor and an ADC in the complete SoC implementation, an ADC architecture must not only be fast but also cheap. The next challenge is low-power dissipation. ADCs should be integrated with digital circuits on a single chip for portable devices. The down-scaling of the minimum channel length to 0.065 um results in the reduction of the power supply voltage to 0.7 V. However, the minimum supply voltage for the analog circuits predicted in the SIA Roadmap [4] does not follow the digital supply voltage reduction. As a result, an ADC should be operated in a small voltage range. The main motivation for this project is to design an ADC that will allow on-chip direct digitization of a wide band RF signal. Yet one of the major challenges in developing the complete SoC product for the wireless digital network market is the integration of radio frequency (RF) analog circuit devices, which are mostly passive discrete devices.

1.1 SOLID-STATE TECHNOLOGY

The type of solid-state technology used to implement the converter also acts the speed of an ADC. Three different types of solid-state technologies are currently used for high-speed ADC implementations: CMOS technology, bipolar technology, and Gallium Arsenide (GaAs) technology. GaAs technology is the fastest of the three, and CMOS technology is the slowest. The fastest ADCs are implemented with flash type architecture using the GaAs technology. The BiCMOS technology requires more processing steps and higher cost compared to standard CMOS technology. Therefore, mixed-signal circuit implementation using only the standard CMOS technology is the

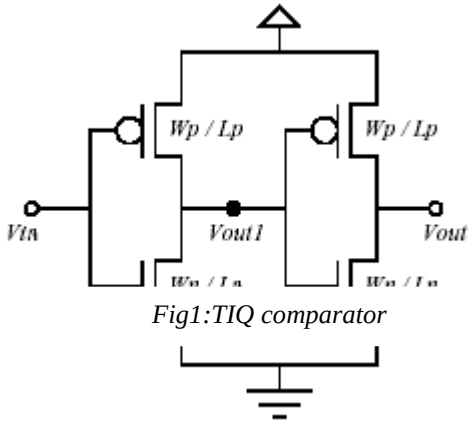


Fig1:TIQ comparator

preferred choice for SoC products.

2.THRESHOLD INVERTER QUANTIZATION (TIQ)

We propose a high-speed CMOS Flash Analog to Digital Converter architecture with low power dissipation, which features the Threshold Inverter Quantization (TIQ) technique. The TIQ technique allows greater ADC speed

$$V_m = \frac{r\left(V_{DD} - \left|V_{Tp}\right|\right) + V_{Tn}}{1+r} \quad \text{with} \quad r = \sqrt{\frac{k_p}{k_n}}$$

using the standard CMOS logic circuitry preferred for SoC implementation. The main advantage of the TIQ based CMOS Flash Analog to Digital Converter (TIQ Flash Analog to Digital Converter) design is a simpler comparator design. The idea is to use digital inverters as analog voltage comparators. This eliminates the need for high-gain differential input voltage comparators that are inherently more complex and slower than the digital inverters. The TIQ Flash Analog to Digital Converter also eliminates the need for reference voltages, which require a resistor ladder circuit. This simplicity in the comparator part provides both high-speed conversion and low-power dissipation at the same time. Moreover, it allows a complete ADC to be implemented using the standard CMOS logic technology, making the featured ADC ideal for a complete SoC implementation. On the other hand, the ADC input range varies due to process parameter changes from one fabrication to another, and the single-ended inverter comparator is more susceptible to noise. These two criteria must be carefully considered to obtain a successful TIQ Flash Analog to Digital Converter implementation

2.1 TIQ Comparator

The comparator is the most important component in the ADC architecture. Its role is to convert an input voltage Vin into a logic `1' or `0' by comparing a reference voltage Vref with the Vin. If the Vin is greater than Vref , the output of the comparator is `1', otherwise `0'. Commonly used comparator structures in CMOS ADC design are the fully differential latch comparator [3] and the dynamic comparator [5, 1]. The former is sometimes called a clocked comparator," and the latter is called an auto-zero comparator" or chopper comparator." To achieve high speed, such comparators are usually implemented with bipolar transistor technology. For SoC implementation in this case, BiCMOS technology would be necessary to integrate both a high-speed ADC and a digital signal process on the same substrate.

The TIQ comparator uses two cascaded CMOS inverters as a comparator for highspeed conversion and low-power dissipation. The proposed TIQ comparator that is described in this project has been developed not only for

higher speed but also for higher resolution. The inverter threshold voltage Vm is defined as the Vin = Vout point in the VTC of an inverter .Mathematically, where VTp and VTn represent the threshold voltages of the PMOS and NMOS devices, respectively. figure 1 shows the schematic of the TIQ comparator and ts VTC from the simulation. At the first inverter, the analog input signal quantization level is set by Vm, depending on the W/L ratios of PMOS and NMOS. The second inverter is used to increase voltage gain and to prevent an unbalanced propagation delay To

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\left(V_{DD} - \left|V_{Tp}\right|\right) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

derive Equation 2, we assume that both transistors are in the active region, the gate oxide thickness (Cox) for both transistors is the same, and the lengths of both transistors (Lp and Ln) are also the same. From Equation 2. we know that Vm is shifted, depending on the transistor width ratio (Wp/Wn). That is, increasing Wp makes Vm larger, and increasing Wn
makes Vm smaller on the VTC.This changing of the widths of the PMOS and NMOS devices with a fixed transistor length is the idea of the TIQ comparator. We can use the inverter threshold voltage as an internal reference voltage to compare the input voltage. However, to use the CMOS inverter as a voltage comparator, we should check the sensitivity of Vm to other parameters, which are ignored in Equation 2, for correct operation of the TIQ flash ADC. In a mixed-signal design, the ignored parameters threshold voltages of both transistors, electron and hole mobility, and power supply voltage are not fixed at a constant value.

3. TYPICAL FLASH ADC

The flash ADC is known for having the fastest speed compared to other ADC architectures. Therefore, it is used for high-speed and very large bandwidth applications such as radar processing, digital oscilloscopes, high-density disk drives, and so on. The flash ADC is also known as the parallel ADC because of its parallel voltage comparator architecture. Figure 2 illustrates a typical flash ADC block diagram. As shown in Figure 2 this architecture needs 2n - 1 comparators for an n-bit ADC. For example, a set of 63 comparators are used for a 6-bit flash ADC. Each comparator has a reference voltage that is provided by an external reference source. These reference voltages are equally spaced by VLSB from the largest reference voltage (V2n-1 in Figure 2) to the smallest reference

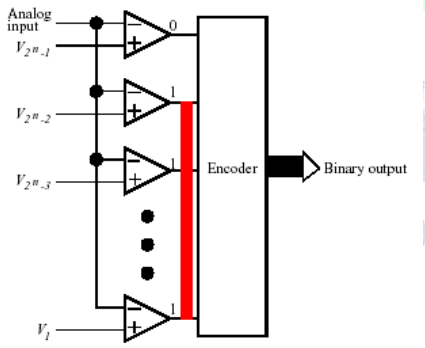
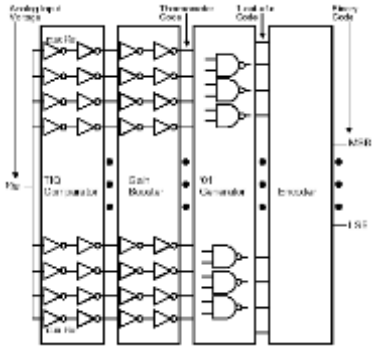


Fig2:typical Flash ADC

voltage V1. An analog input is connected to all comparators so that each comparator output is produced in one cycle. The digital output of the set of comparators called the thermometer code and is changed into a binary code through the encoder. The flash ADC architecture has high-speed conversion due to its parallel structure.

4.TIQ BASED FLASH ADC



This section provides detailed information about the proposed TIQ flash ADC, including its major components. The proposed flash ADC features the threshold inverter quantization (TIQ) technique for high speed and low power, using standard CMOS technology that is compatible with microprocessor fabrication. Figure 3 shows the block diagram of the TIQ flash ADC. The use of two cascaded inverters as a voltage comparator is the reason for the technique's name. The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters. Hence, we do not need the resistor ladder circuit used in a conventional flash ADC, as shown in Figure 2. The gain boosters make sharper thresholds for comparator outputs and provide a full digital output voltage swing. The comparator outputs - the thermometer code - are converted to a binary code in two steps through the `01' generator and the encoder, as shown in Figure 3.
the proposed structures layout with area and power optimization is done in MAGIC 7.0 with HSPICE simulator figure 4 shows the output waveform for a three bit ADC. During the layout different power optimization technique like double pass transistor logic(DPL) , static differential cascode voltage switch logic (SDCVSL) and Dual-Rail Domino Logic (DRDL) has been utilized according to the requirement.

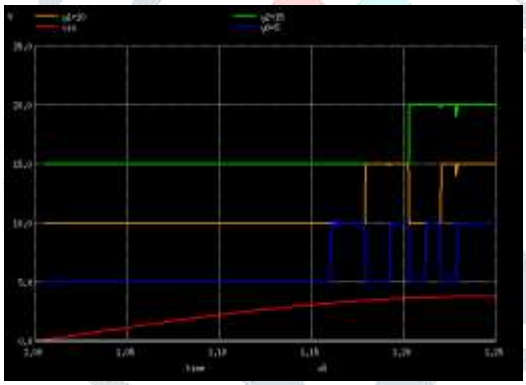
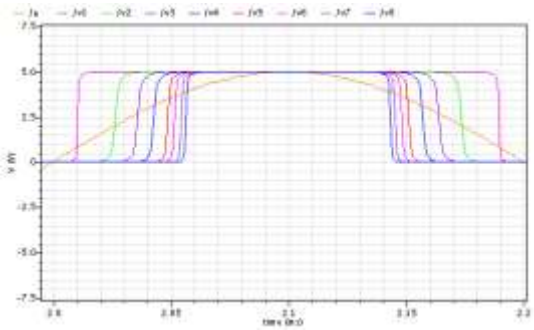


Fig4:output waveform for TIQ Flash ADC

Using cadence spectre tool the transistor level circuit diagram of the above said TIQ based Flash ADC is drawn and its found to occupy 103 transistors. The simulated waveform with nominal temperatures is shown in figure 5. All the power calculations are being done using a calculator associated with the Spectre. A comparative study of analog device ADC with the proposed one is made and an area reduction of 43% is obtained In order to obtain the reasonable conducting current to drive capacitive loads in ordinary available ADCs vary the width of the transistors which increases power dissipation and propagation delay This is completely avoided in the proposed prototype Power Dissipation can be calculated using

$$Pd = Vdd*Vswing *Cnode*Fc$$



Where Vswing=Vdd-Vth, problems of noise margin and speed degradation are improved at the cost of a slight increment in area.

The precharged circuit using dual rail domino logic increases the speed of the CMOS circuit required for the fat free encoder implemented in the TIQ based flash ADC. A domino gate consists of a pmos fet precharged transistor, nmos evaluation transistor with the clock signal applied to the gate nodes[3]. The complete output waveform of the TIQ based flash ADC for a three bit prototype in cadence is shown in figure 6.

5.ALGORITHMS

Since the project aims to score area optimization and power optimization the entire problem formulated is of NP- hard. Most optimization in physical design are NP-hard since project tries to make a prototype of the differed version of the inputs applied. Here inputs only ranging from 0Vto 7V. Since the size of the input is small then the algorithms with free exponential time complexity may be feasible. The solution of the problem is critical to the performance of the chip so i olve problem optimally. Integer programming is used to solve the physical d ave physical design problems and polynomial time complexity. One disadvantage is the performance may be degraded when sizing becomes large. Those instances special case algorithms can be used .The restrictions applied for such algorithms may be a limitation but it is solvable in a polynomial time. Layout problems allow the usage of special case algorithms .The clock routing problem which is rather hard for full custom design can be solved for symmetric structures using gate arrays. Rare possibilities of using approximations algorithms and heuristic algorithms are coming into the picture. Preference will be given to approximation algorithms since they provide a definite amount of guarantee in the solution provided.

Fig 5:cadence output fot TIQ comparator

Design Style	Adder Area ($\times 10^4 \mu m^2$)	No. of Transistors
CSL	5.42	144
CPL	4.46	88
DPL	6.52	136
SDCVSL	5.19	114
SDSL	6.39	130
DRDL	6.48	146
DDCVSL	7.22	154
ECDL	7.65	166

Table 1 shows the power and area optimization of different circuit styles implemented in the proposed design. The table shows that the DRDL is the best circuit styling to obtain the goal of the project.

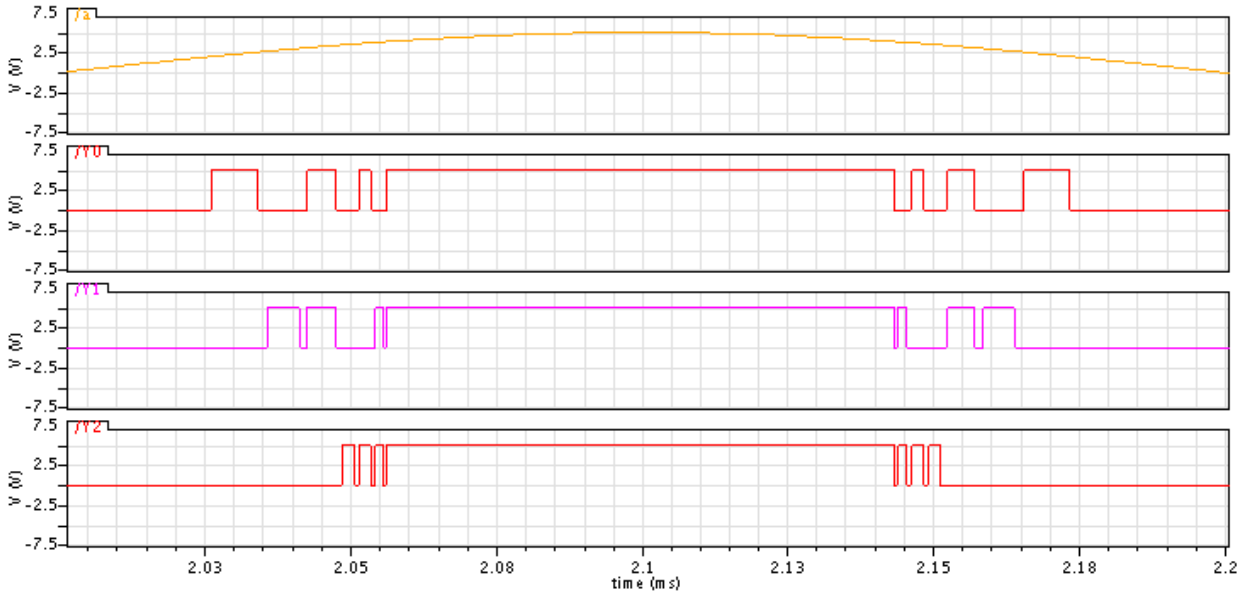


Figure 6 Output waveform for MTIQ based three bit flash ADC using Cadence

Table 2: Width Vs corresponding output

Width in um	Vref in Volts
0.5	0.8
3.6	2.01
8	2.7
14	3.1
23	3.5
30	3.6
40	3.8
50	3.9

6.CONCLUSION

The proposed design attains 43% of area optimization when compared with analog device ADC (6 bit) AD73148 which is the most commonly used ADC in embedded applications. The project guarantees no missing codes with the propagation delay of .1ns. Each bit increment of the ADC causes around 28 transistors further to the design. It is expected the proposed idea may drastically change the cost, area, speed and power optimization of conventional ADC in future years.

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