To Design 2-bit Magnitude Comparator using CMOS

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Abstract: This paper explains the design of a magnitude comparator with four digital input signals and three output signals. The outputs are Greater than, less than and Equals respectively for the four input signals. Low power comparator design is useful to reduce the complexity and increase the computation speed of many digital devices such as ADC, Memory chips etc.
The design is done using Full Adder circuit in Mentor Graphics Eldo net tool. The 180nm technology, file is used for the design of the magnitude comparator. Simulation is done on 0.6V, 0.8V, 1V and 1.2V respectively. It is found that power is least dissipates in 0.6 V that is 48.82pW.but it has the longest delay of 53.098ns.The proposed comparator design is compared with different logic styles such as PTL, Domino logic, and Transmission gates with voltage sweep

Index Terms **- Magnitude Comparator, nano meter technology, Full Adder, Eldo net Tool**

I. INTRODUCTION

Magnitude Comparator is a digital comparator which has three output terminals, one each for equality (A = B) greater than (A > B) and less than (A < B) result of two bit input DC signals. It is useful in design of ADC, DAC, Memory chips for power and speed efficiency. For IC Design various backend tools are available in the market such as Mentor graphics, Microwind, Tanner EDA tool etc. The two bit comparator is designed using Mentor Graphics EDA tool. Mentor Graphics provides various tools for Electronic Design Automation such as Integrated Circuit Design, IC Place and Route, IC verification, Schematic Editor, Layout and Design rules.

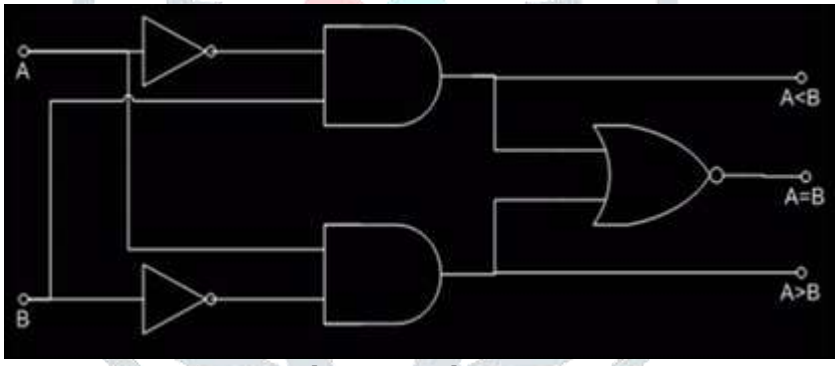

Figure 1: 2-bit magnitude comparator

Technology file contains the process related information such as sheet resistance and layer thickness. It also includes dimension of chip, conductive, non conductive layers, resistivity, permittivity, metal thickness, via. In Mentor Graphics we have ami05.mod, ami12.mod, tsmc018.mod, tsmc025.mod, tmsc03.mod technology files.

In paper [1] A Design of low power magnitude comparator, presented. Performance parameters such as Power, Delay and Power Delay Product are increased as compared to simple circuit. The 90nm technology file is used to get power dissipation parameter reduced to Pico Watts. The design of comparator is simulated for different voltage sweeps from 0.6V to 1V.In paper [2] the design of low power high speed comparator, the comparator is designed using 0.13um technology. Power dissipation is only 1.5nW. It works on supply voltage of 1.2V.

In paper [3] Design of a Low Power 0.25 µm CMOS application of comparator for ADC design is discussed. Dynamic latch method is used to design comparator. This design is used for high speed ADC. Overall result of the power dissipation is slightly off than the targeted value. In paper [4] Comparative Analysis of a 2-bit Magnitude Comparator using various High Performance Techniques, various logic styles for comparator design like Basic CMOS, Hybrid PTL, Domino etc. are implemented and compared. Hybrid PTL is derived as a Lowest Power consumption technique. In paper [5] Design of low power two bit magnitude comparator using adiabatic logic zero loss of heat is implemented in 0.18um technology. Power efficiency (PDP) as compared to conventional design is improved and equals to 80.54% as expected theoretically.

II. LOGIC STYLES AND CIRCUIT FAMILIES

We have various techniques to optimize combinational circuits for lower delay and/or energy. The vast majority of circuits use static CMOS because it is robust, fast, energy-efficient, and easy to design. However, certain circuits have particularly stringent speed, power, or density restrictions that force another solution. Such alternative CMOS logic configurations are called

circuit families. The most commonly used alternative circuit families are: Ratioed circuits, Dynamic circuits, and Pass Transistor circuits. The delay of a logic gate depends on its output current I, load capacitance C, and output voltage swing ΔV.

$$t \propto \frac{C}{I} \Delta V \text{..... Equation1}$$

Faster circuit families attempt to reduce one of these three terms. NMOS transistors provide more current than PMOS for the same size and capacitance, so NMOS networks are preferred.

Dynamic circuit operation is divided into two modes, as shown in Figure 5.During precharge, the clock ϕ is 0, so the clocked PMOS is ON and initializes the output Y high. During evaluation, the clock is 1 and the clocked PMOS turns OFF. The output may remain high or may be discharged low through the pulldown network. Dynamic circuits are the fastest commonly used circuit family because they have lower input capacitance and no contention during switching.

Figure 2: Precharge and Evaluation stage of Dynamic Circuit

But the Dynamic Circuit has the monotonicity problem. A fundamental difficulty with dynamic circuits is the monotonicity requirement. While a dynamic gate is in evaluation, the inputs must be monotonically rising. That is, the input can start LOW and remain LOW, start LOW and rise HIGH, start HIGH and remain HIGH, but not start HIGH and fall LOW. Unfortunately, the output of a dynamic gate begins HIGH and monotonically falls LOW during evaluation. This monotonically falling output X is not a suitable input to a second dynamic gate expecting monotonically rising signals.

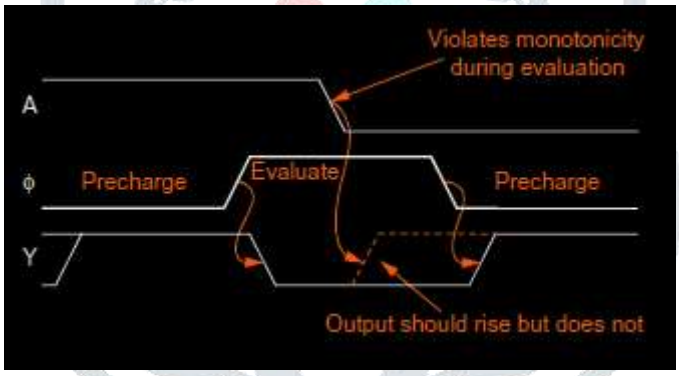

Figure 3: Monotonicity in Dynamic Circuit

The monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates. The dynamic-static pair together is called a domino gate because precharge resembles setting up a chain of dominos and evaluation causes the gates to fire like dominos tipping over, each triggering the next. A single clock can be used to precharge and evaluate all the logic gates within the chain. The dynamic output is monotonically falling during evaluation, so the static inverter output is monotonically rising. Therefore, the static inverter is usually a HI-skew gate to favor this rising output.

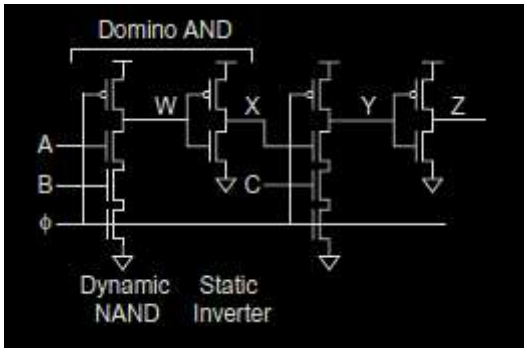

Figure 4: Domino Logic for Inverter Circuit

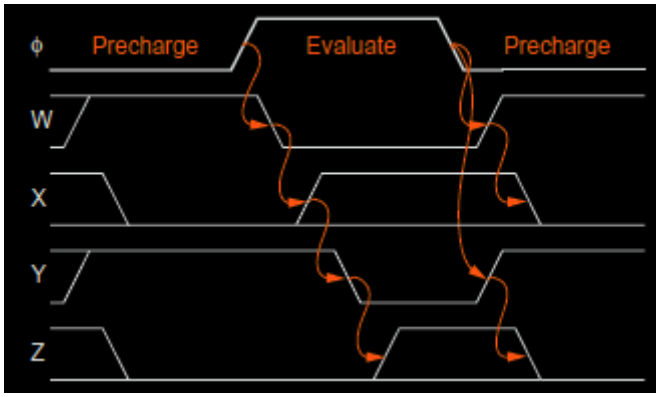

Figure 5: Monotonicity removed by Domino Logic

III. RESEARCH METHODOLOGY

The Magnitude Comparator is designed using domino logic. The Mentor Graphics tool is used for a circuit design. Figure 6 and Figure 7 Explains the Circuit design and the gate level design for the Greater than circuit Figure 8 and Figure 9 Explains the Circuit design and gate level design for the Equals to circuit. Figure 10 and Figure 11 Explains the Circuit design and gate level design for the Less than circuit.

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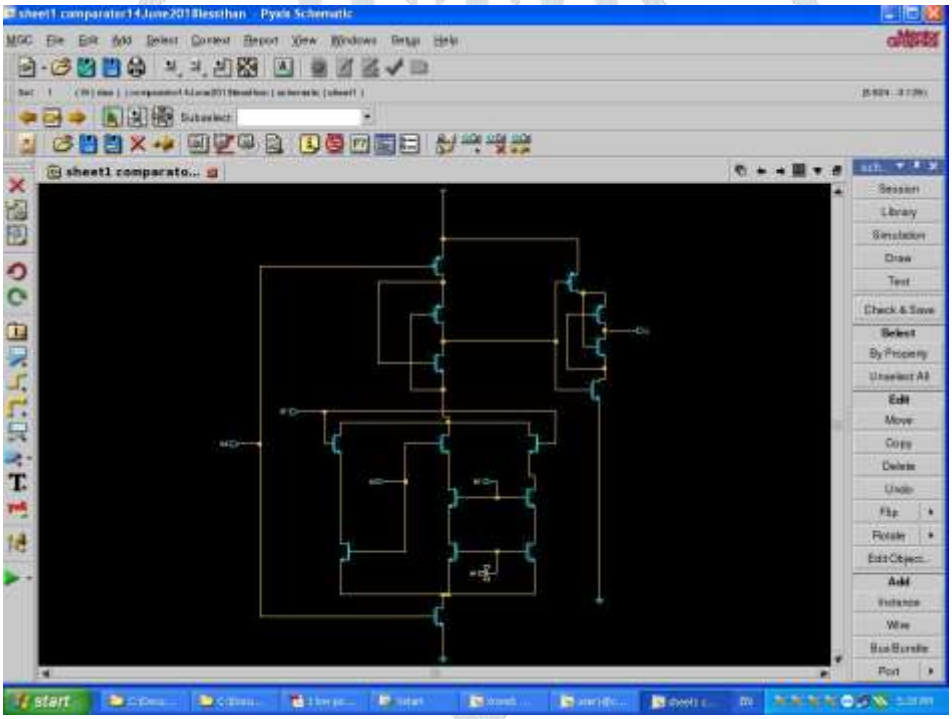

Figure 6: Circuit Diagram for Greater Than Circuit

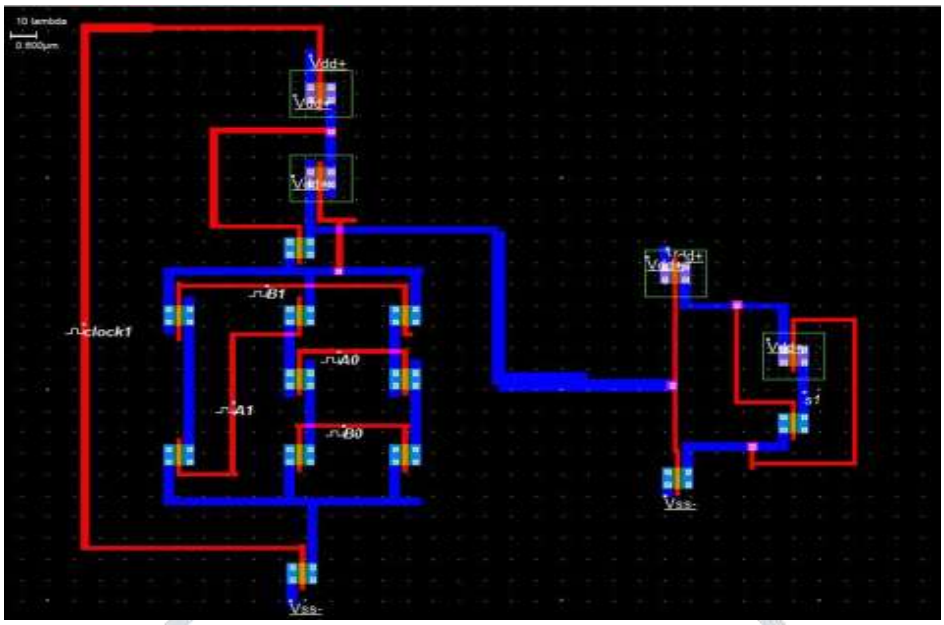

Figure 7: Gate level Diagram for Greater than Circuit

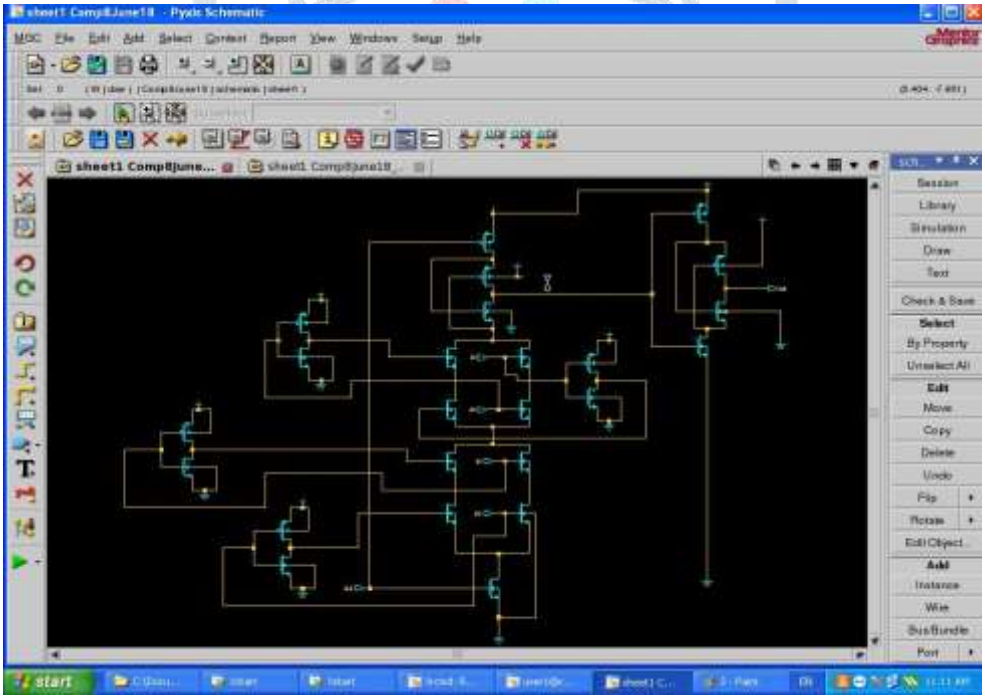

Figure 8: Circuit Diagram for Equals to Circuit

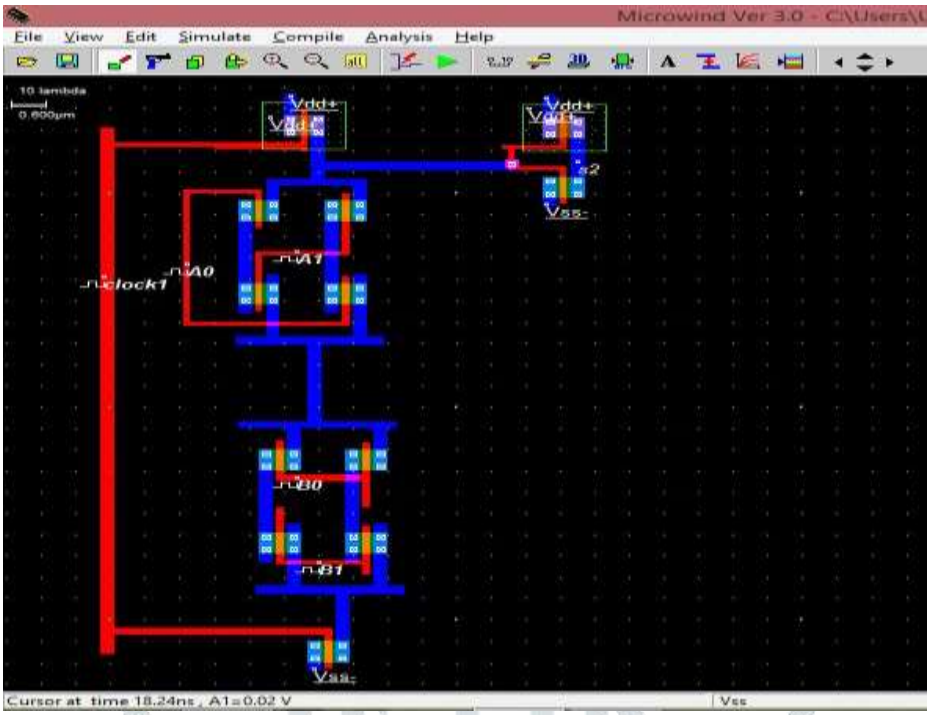

Figure 9: Gate level Diagram for Equals to Function

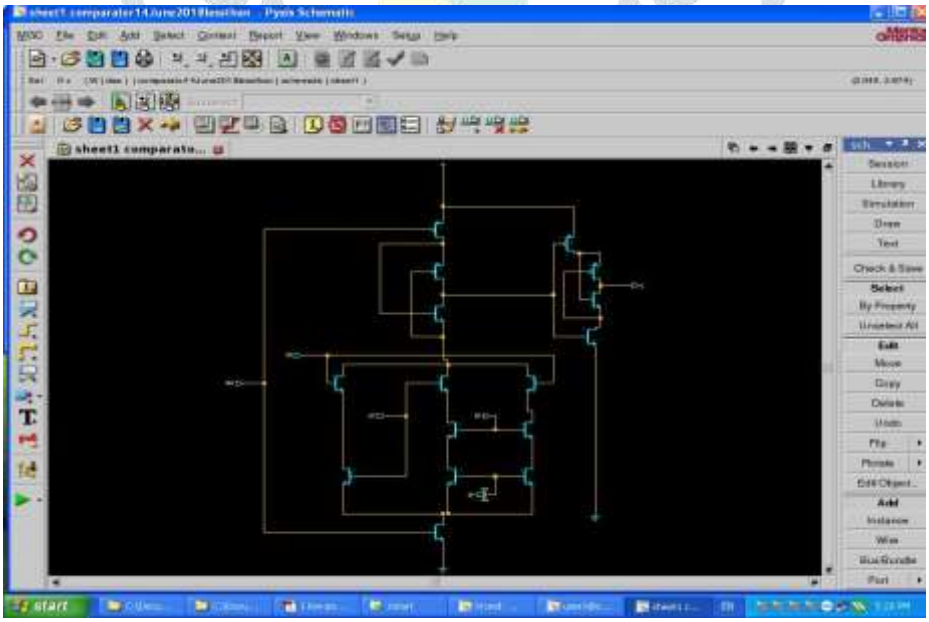

Figure 10: Circuit Diagram for Less than Circuit

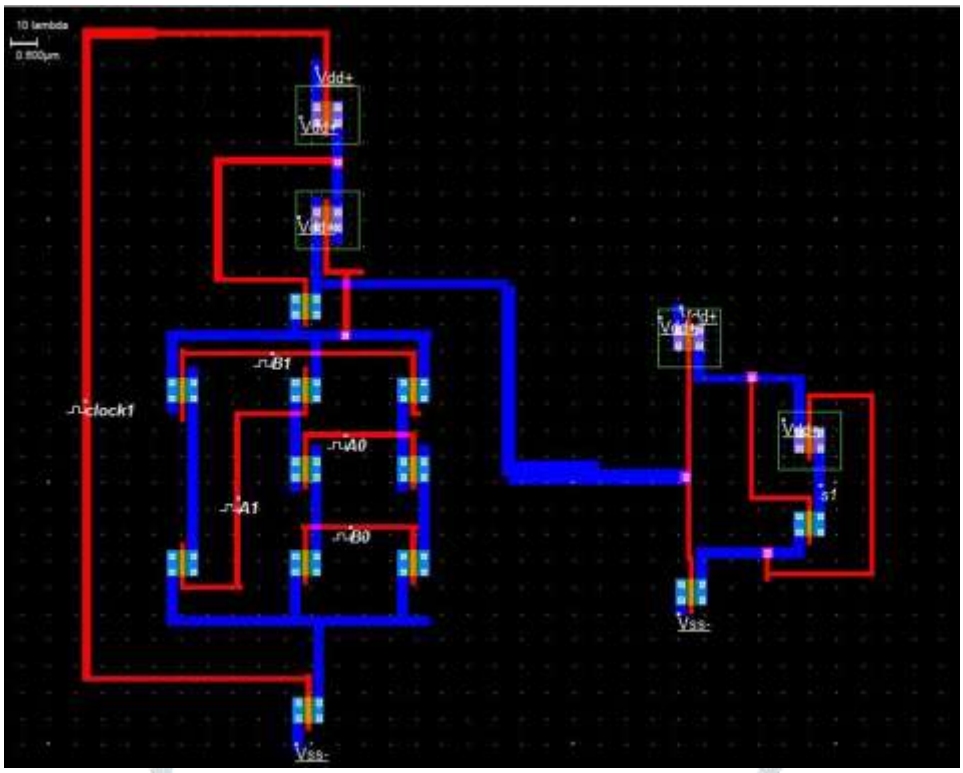

Figure 11: Gate level Design for the Less than Function

IV. RESULTS AND DISCUSSION

The output waveforms for the proposed circuit is shown in Figure 12, 13, 14 For the Greater than, Less than and Equals to Circuits.

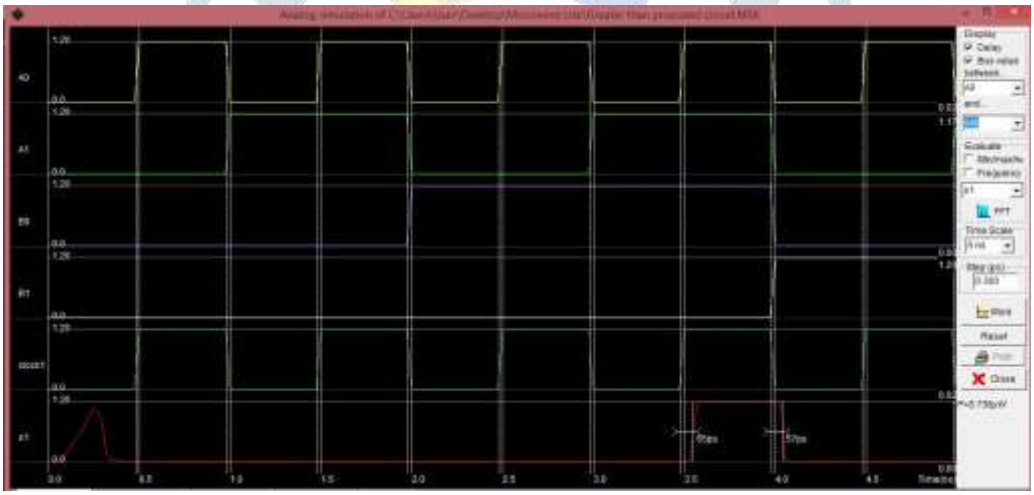

Figure 12: Greater than Circuit Output Waveforms

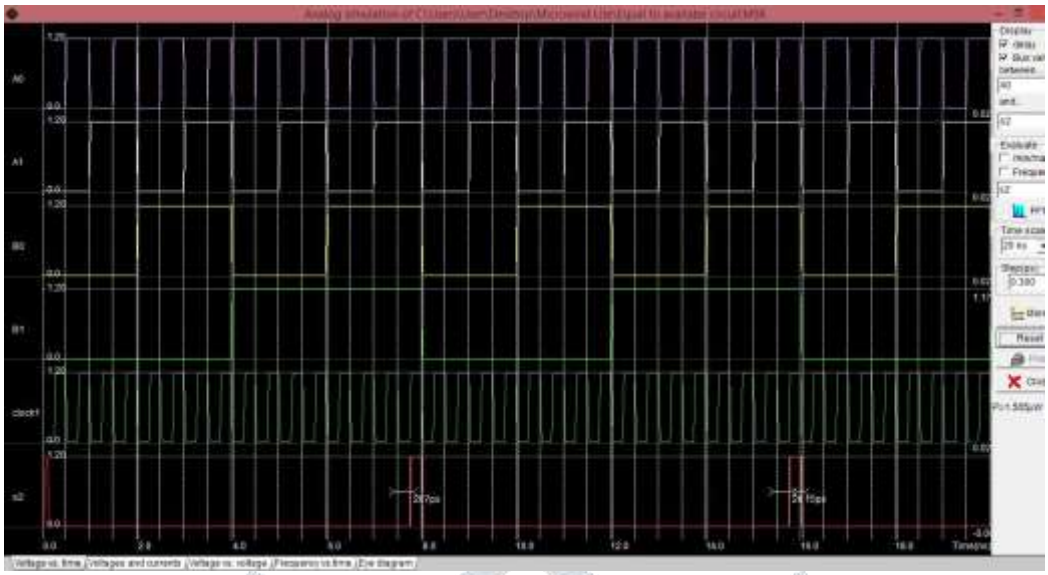

Figure 13: Equals to Circuit Output Waveforms

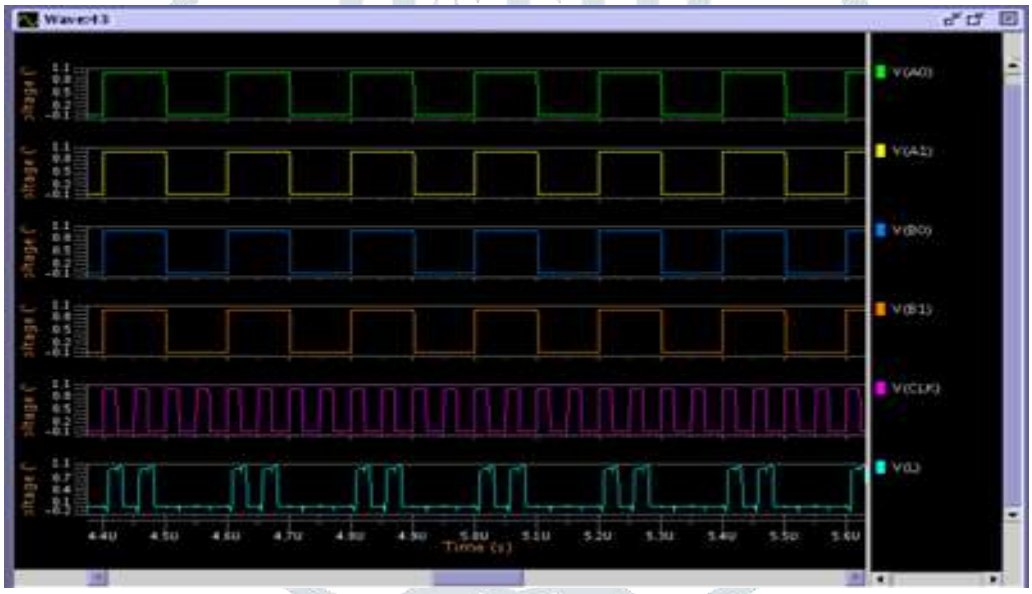

Figure 14: Less than Circuit Output Waveforms

The transient and DC Analysis are carried out for each circuit using EZ wave Tool. The proposed circuits are in good agreement in terms of power consumption as shown in Table 1.

Table 1 : Power Analysis for a Comparator

	Power Dissipation			
V dd	Full Adder	Transmission Gate	PTL logic	Domino logic
0.6	10.6	3.8	0.8	48.6218
0.8	33.5	10.7	3.7	73.5868
1	85.5	23.5	10.4	1110.2903
1.2	117.28	44.6	11.3	197.20

IV. ACKNOWLEDGMENT

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