

Design and Implementation of a Novel Multilevel DC–AC Inverter

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Abstract:

Multilevel inverters have been widely accepted for high-power high-voltage applications though the multilevel inverters hold attractive features, usage of more switches in the conventional configuration poses a limitation to its wide range application. Therefore, 7-level inverter topology is introduced using less number of switches and gate trigger circuitry, thereby ensuring the minimum switching losses, reducing size and installation cost. Multilevel inverter (MLI) plays a vital role in the field of power electronics and being widely used in many industrial and commercial applications. The multilevel inverter topology is the proper option from the point of view of modularity and simplicity of control.

Index Terms - Multilevel DC to AC inverter, PIC Microcontroller, SPWM.

I. INTRODUCTION

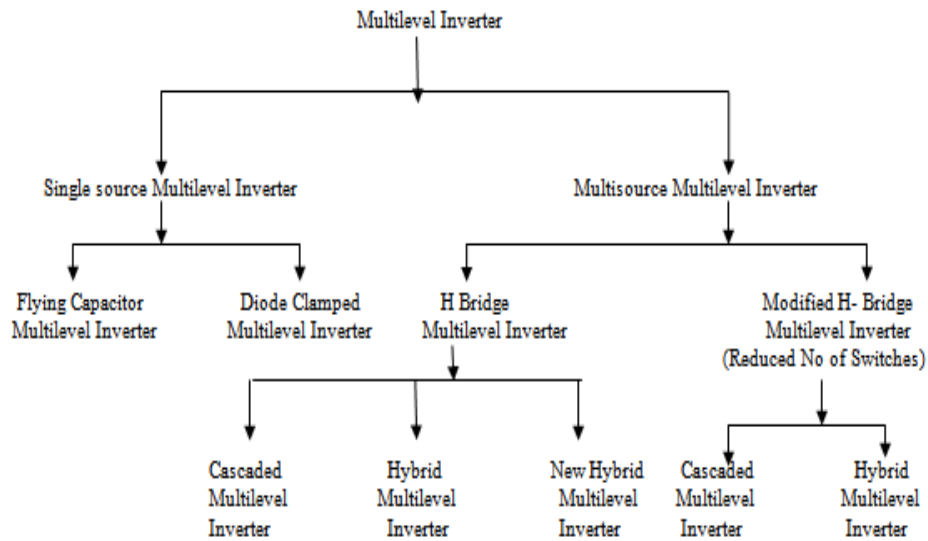
High power and high-voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power applications at both the transmission and distribution levels. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms.

One of the power converters which can transform dc–ac is called inverter. Inverter is the inter medium which transmits power to other electrical equipment such as uninterruptible power supply, servo motor, air-conditioning system, and smart grid composed of renewable energy shown in Fig. 1. To satisfy different demands and characteristic of loads, the output Frequency and voltage have to change with different loads. In recent years; the amount of power equipment is increasing. Therefore, the harmonic pollution of power system becomes more serious. Several standards and regulations have been formulated to limit quality of harmonics and power factor of electric equipment.

Furthermore, in order to meet the industry requirements for high power applications, the voltage stress of the power Device also increases. Although an insulated gate bipolar transistor (IGBT) has features of high power rating and high voltage stress, it cannot operate at high frequency. And the design of IGBT gate driver is complicated. AMOSFET is the appropriate Component to operate at high frequency, but power rating is not as good as IGBT. To solve the problem, many different topologies of multilevel use low rating component at high-power application.

The purpose of the multilevel topology is to reduce the voltage rating of the power switch. Therefore, it usually is used at High-power application. By combining output voltages in multilevel form, it has advantages of low dv/dt, low input current distortion, and lower switching frequency. As a result of advantages of multilevel topology, several topologies have emerged in recent years. A novel multilevel inverter is designed and implemented in this paper. The major feature of the proposed topology is the reduction of power components.

II. CLASSIFICATION OF MULTILEVEL INVERTER



III. POWER STAGE

A. Circuit Configuration

Fig. 2 shows the proposed novel topology used in the seven level inverter. An input voltage divider is composed of three series capacitors C_1 , C_2 , and C_3 . The divided voltage is transmitted to H-bridge by four MOSFETs, and four diodes. The voltage is sent to output terminal by H-bridge which is formed by four MOSFETs. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals design

B. Operating Principles

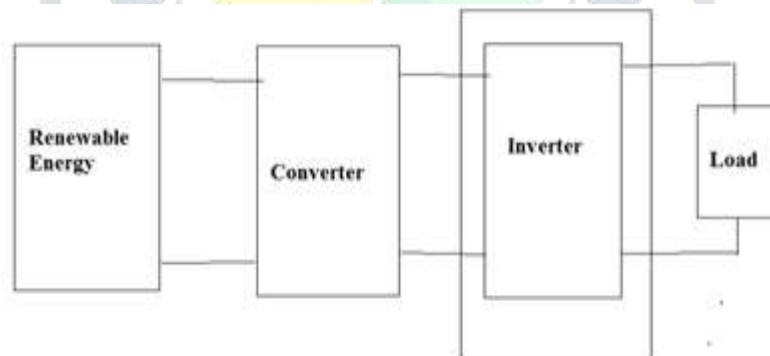


Fig 1. Block diagram of Renewable system

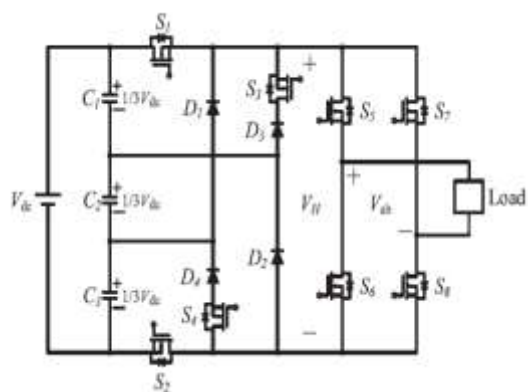


Fig.2. Proposed seven-level inverter topology

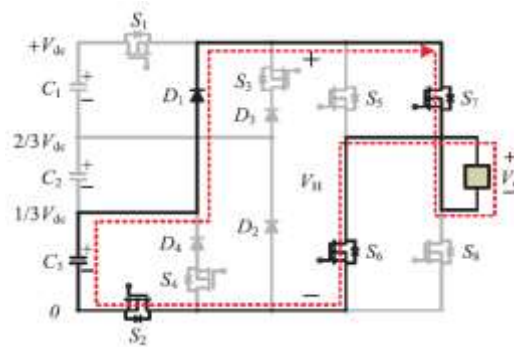


Fig. 6. Switching combination of output voltage level $-1/3V_{dc}$.

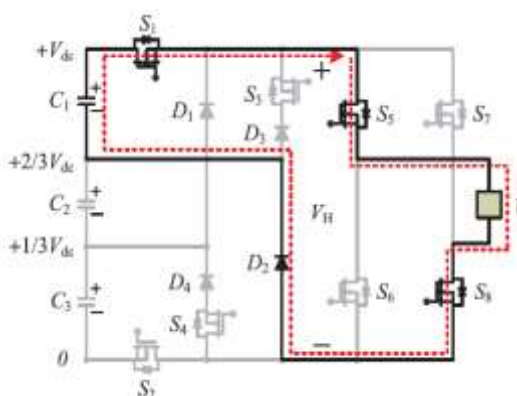


Fig. 3. Switching combination of output voltage level $1/3V_{dc}$

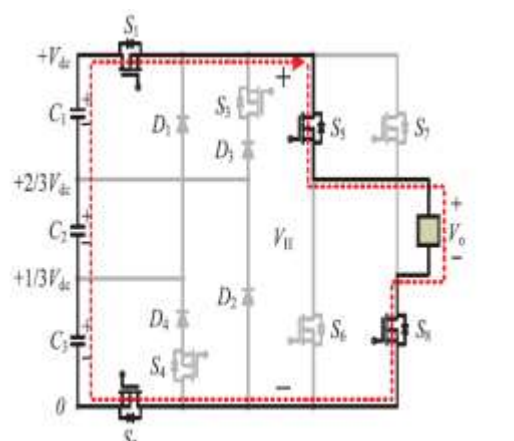


Fig 5. Switching combination of output voltage level V_{dc} .

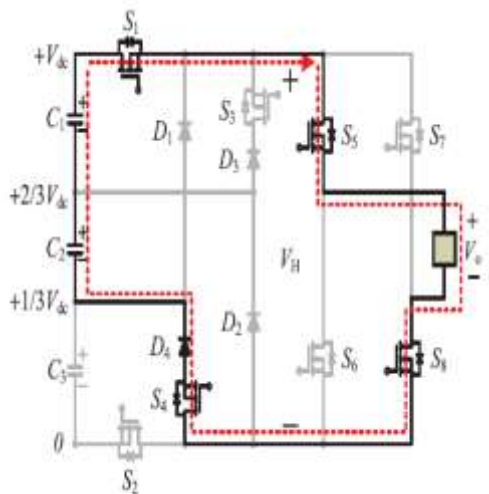


Fig 4. Switching combination of output voltage level $2/3V_{dc}$

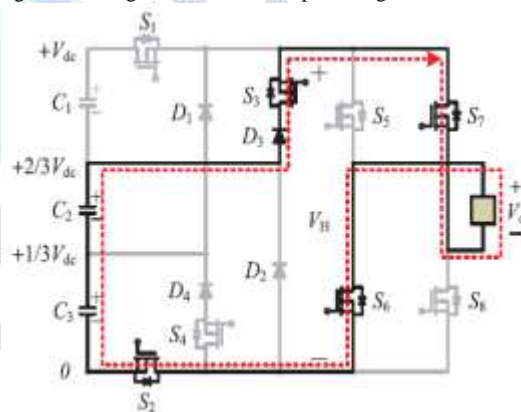


Fig. 7. Switching combination of output voltage level $-2/3V_{dc}$.

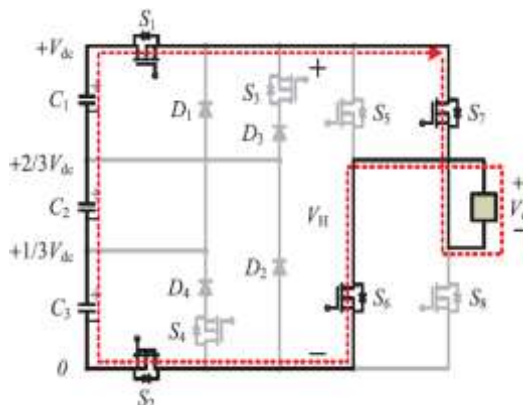


Fig. 8. Switching combination of output voltage level $-V_{dc}$.

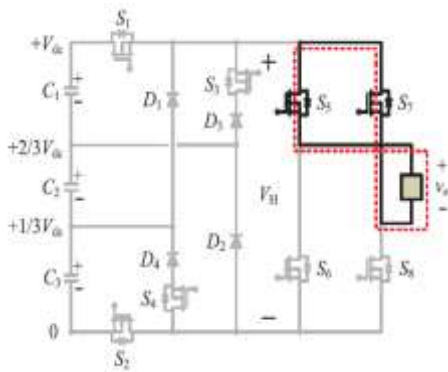


Fig. 9. Switching combination of output voltage level 0.

The required seven voltage output levels ($\pm 1/3V_{dc}$, $\pm 2/3V_{dc}$, $\pm V_{dc}$, 0) are generated as follows.

- 1) To generate a voltage level $V_0 = 1/3V_{dc}$, S_1 is turned on at the positive half cycle. Energy is provided by the capacitor C_1 and the voltage across H-bridge is $1/3V_{dc}$. S_5 and S_8 are turned on, and the voltage applied to the load terminals is $1/3V_{dc}$. Fig. 3 shows the current path at this mode.
- 2) To generate a voltage level $V_0 = 2/3V_{dc}$, S_1 and S_4 are turned on. Energy is provided by the capacitor C_1 and C_2 . The voltage across H-bridge is $2/3V_{dc}$. S_5 and S_8 are turned on, and the voltage applied to the load terminals is $2/3V_{dc}$. Fig. 4 shows the current path at this mode.
- 3) To generate a voltage level $V_0 = V_{dc}$, S_1 and S_2 are turned on. Energy is provided by the capacitor C_1 , C_2 , and C_3 . The voltage across H-bridge is V_{dc} . S_5 and S_8 are turned on, and the voltage applied to the load terminals is V_{dc} . Fig. 5 shows the current path at this mode.
- 4) To generate a voltage level $V_0 = -1/3V_{dc}$, S_2 is turned on at the negative half cycle. Energy is provided by the capacitor C_3 , and the voltage across H-bridge is $1/3V_{dc}$. S_6 and S_7 are turned on, and the voltage applied to the load terminals is $-1/3V_{dc}$. Fig. 6 shows the current path at this mode.
- 5) To generate a voltage level $V_0 = -2/3V_{dc}$, S_2 and S_3 are turned on. Energy is provided by the capacitor C_2 and C_3 . The voltage across H-bridge is $2/3V_{dc}$. S_6 and S_7 are turned on, and the voltage applied to the load terminals is $-2/3V_{dc}$. Fig. 7 shows the current path at this mode.
- 6) To generate a voltage level $V_0 = -V_{dc}$, S_1 and S_2 are turned on. Energy is provided by the capacitor C_1 , C_2 , and C_3 , the voltage across H-bridge is V_{dc} . S_6 and S_7 are turned on, the voltage applied to the load terminals is $-V_{dc}$. Fig. 8 shows the current path at this mode.
- 7) To generate a voltage level $V_0 = 0$, S_5 and S_7 are turned on. The voltage applied to the load terminals is zero. Fig. 9 shows the current path at this mode.

C. Topology Comparison

TABLE I : SWITCHING COMBINATIONS REQUIRED TO GENERATE THE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

Output voltage V_o	Switching combinations							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

TABLE II : COMPONENTS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

TABLE III : VOLTAGE STRESS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	V_o	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	V_o	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

Table II presents the number of components required to implement a seven-level inverter using the proposed topology and three previously ones [9], [10] that can be considered as the standard multilevel configurations, the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multicellular inverter.

Table II shows that the new topology achieves the reduction in the number of power devices.

Table III shows the voltage stress comparison between different type inverters.

V. CONTROL TECHNIQUE

The main aim of the modulation strategy of multilevel inverters is to synthesize the output voltage as close as possible to the sinusoidal waveform. Many modulation techniques have been developed for harmonic reduction and switching loss minimization. The modulation methods used in multilevel inverters can be classified according to switching frequency. Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. Output voltage from an inverter can also be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by pulse width modulation control used within an inverter. In this method, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the ON and OFF periods of the inverter components. This is the most popular method of controlling the output voltage and this method is termed as Pulse-Width Modulation (PWM) Control.

Mainly the power electronic converters are operated in the switched model. This means the switches within the converter are always in either one of the two states -turned off or turned on. Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states. This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired dc or low frequency ac component is retained. This process is called Pulse Width Modulation, since the desired average value is controlled by modulating the width of the pulses.

VI. Advantages of PWM technique

The advantages possessed by PWM techniques are as under:

- The output voltage control can be obtained without any additional components.
- The lower order harmonics can be eliminated or minimized along with its output voltage control.
- The filtering requirements can be minimized as higher order harmonics can be filtered easily

VII.Sinusoidal Pulse Width Modulations

In this type of modulation the width of each pulse is varied in proportion to the amplitude of sine wave evaluated at the centre of the same pulse. The gating signal is provided by comparing a sinusoidal reference signal with a triangular carrier signal. The frequency of the reference signal determines the output frequency of the inverter and its peak amplitude A_r controls the modulation index. As mentioned earlier, it is desired that the ac output voltage $V_o = V_{ao}$ follow a given waveform (e.g., sinusoidal) on a continuous basis by properly switching the power valves. The carrier based PWM technique fulfills such a requirement as it defines the ON and OFF states of the switches of one leg of a VSI by comparing a modulating signal V_r (desired ac output voltage) and a triangular waveform V_c (Carrier Signal). In practice, from Fig, when $V_r > V_c$ the switch S_+ is on and the switch S_- is off; similarly, when $V_r < V_c$ the switch S_+ is off and the switch S_- is on. A special case is when the modulating signal V_r is sinusoidal at frequency f_r and amplitude A_r and the triangular signal V_c is at a frequency f_c and amplitude A_c . This is the Sinusoidal PWM (SPWM) scheme. In this case, the modulation index m_a (also known as the amplitude-modulation ratio) is defined as

$$m_a = A_r/A_c \tag{4.1}$$

and the normalized carrier frequency m_f (also known as the frequency-modulation ratio) is

$$m_f = f_c/f_r \tag{4.2}$$

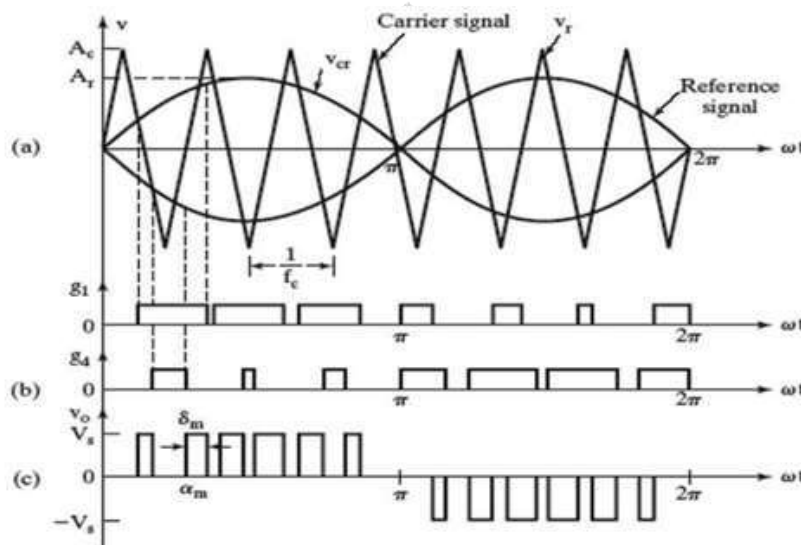


Fig.13 Sinusoidal Pulse Width Modulation

IV. PI CONTROL USED IN MODIFIED SPWM

Modified SPWM based on PI control is used in this paper [18], [19]. Fig. 14 shows the block diagram of PI control. The block diagram can be expressed in S domain as

$$u(s) = \left[K_p + \frac{K_i}{s} \right] e(s). \tag{3}$$

From (3), the equation can be transformed in the Z domain as

$$u(z) = \left[K_p + \frac{K_i}{1 - z^{-1}} \right] e(z). \tag{4}$$

Then, transform (4) becomes a difference equation is expressed as

$$u[n] = K_p e[n] + K_i e[n] - K_i e[n - 1] + u[n - 1] \tag{5}$$

Fig. 15 shows system configuration and control block. System detects output voltage first and compares this signal with a built-in reference. Then, the system feedbacks an error to PI controller. Finally, the PI controller exports a control signal to gate driver. The main idea of modified SPWM is to record the previous error of output voltage and generate a suitable correction at the latest cycle. Because the frequency of carrier is 18 kHz and the frequency of output sine wave is 60 Hz, the number of times of switching is 300 times. Fig. 16 shows the schematic of modified SPWM. $v_{ref}[n]$ is defined as the reference output voltage, $v_o[n]$ is the feedback of output voltage, and $e[n]$ is error between reference output and feedback output which is expressed as

$$e[n] = v_{ref}[n] - v_o[n] \tag{6}$$

Let $K_1 = K_p + K_i, K_2 = K_p$, then $e[n]$ is multiplied by K_1 and $e[n - 300]$ multiplied by K_2 . Then, add the previous output signal $u[n - 300]$. Finally, it can obtain the output of PI controller after the process by the anti-windup.

$$u'[n] = K_1 \cdot e[n] - K_2 \cdot e[n - 300] + u'[n - 300]. \quad (7)$$

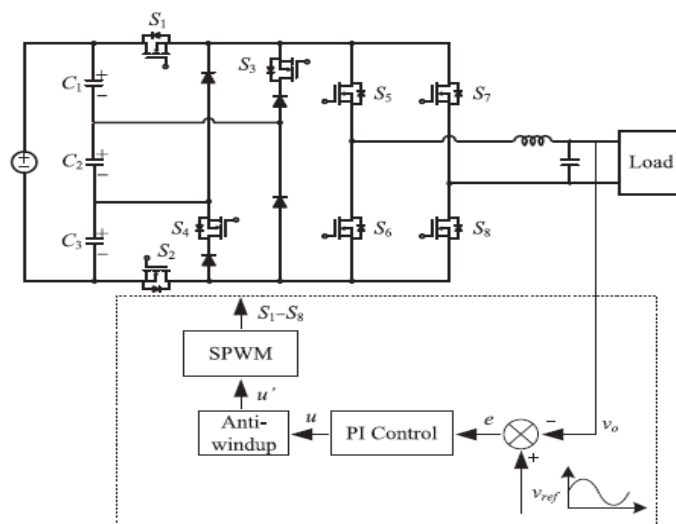


Fig. 15. Seven-level inverter with control algorithm.

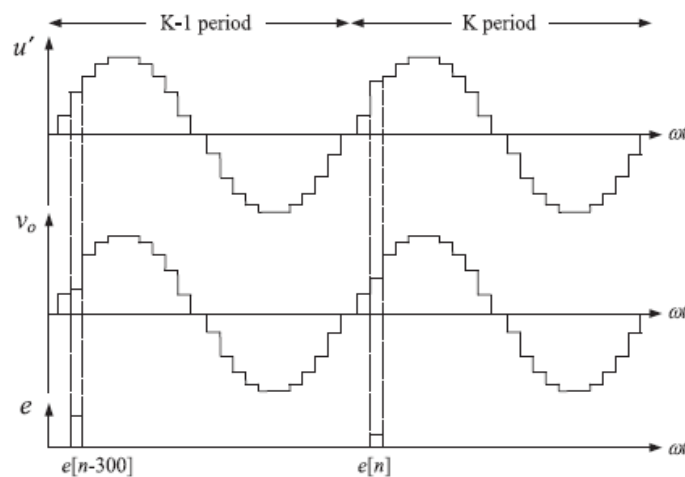


Fig. 16. Schematic of modified SPWM.

TABLE IV
Specifications of the proposed inverter

Input Voltage Vdc	18 V
Output Voltage Vo	Vp=18V, Vrms=12
Rated Output Power Po	30 W
Switching Frequency	10 Khz



Fig.17 Experimental Setup

VII. SIMULATION RESULTS

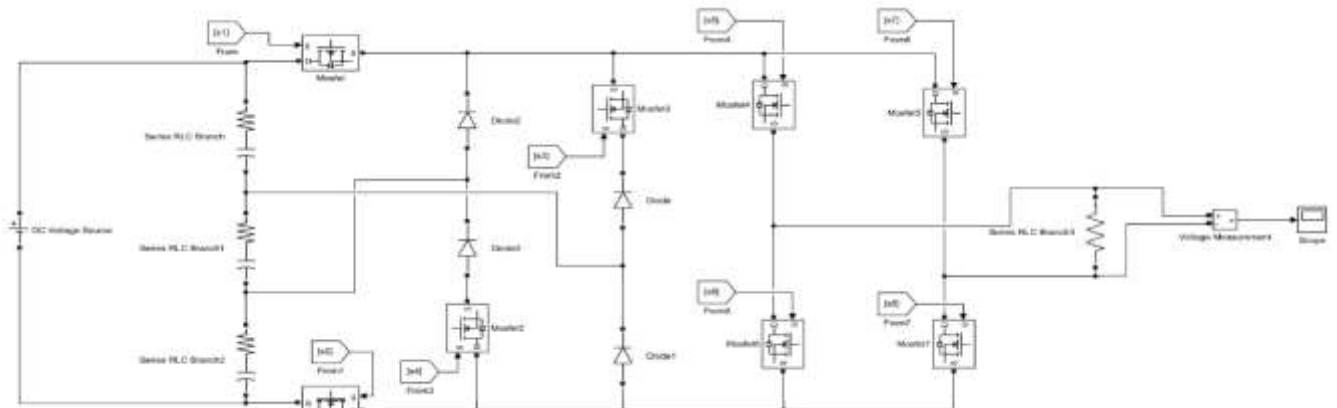


Fig.18 Output Waveform

V. CONCLUSION

Seven level multi-string inverters is the best suited topology for the dc to ac conversion and gives better output in space vector modulation. In seven level multi-string inverters due to the better ac to dc conversion the harmonic losses will be totally reduced. Hence we require small size filter in proposed method. So it is better to prefer, seven levels multi-string inverter for industrial drives to get low cost, easy operation, high efficiency.

A novel seven-level inverter was designed and implemented with PIC controller in this paper. The main idea of the proposed configuration is to reduce the number of power device. The reduction of power device is proved by comparing with traditional structures. Finally, a laboratory prototype of seven-level inverter with 18V input voltage and output 12 V_{rms}/30W is implemented.

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