Design and Implementation of 8-Bit Low Power Parallel Adder/Subtractor Circuit Using Reversible Computing

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Abstract - New technology innovation is facing a big challenge of miniaturization and low power electronics. Reversible logic proves to be an emerging solution. Reversible logic has various applications in modern low power computing environment. Adders play a major role in ALU and processors of any computing environment. Adders are not only suitable for addition but for subtraction and multiplication also. For many commercial applications, decimal arithmetic is highly demanding. The main aim of this paper is to design the improved reversible 4-bit & 8-bit full adder/subtraction circuit using Dual Key Gate (DKG) and Dual key Gate Pair (DKGP) gates that work singly as full adder/full subtraction are used to realize the basic building blocks of logic circuits. The reversible 4-bit & 8-bit full adder/subtraction circuit aresynthesized and simulated in VHDL language using EDA (ElectronicDesign Automation) tool-Xilinx ISE design suit14.2.

Keywords - Low power CMOS, quantum computing, reversible logic gates, parallel adder/subtraction, power consumption.

I. Introduction

The advancement in higher-level integration and fabrication process has emerged in better logic circuits and energy loss has also been dramatically reduced over the last decades. This trend of reduction of heat in computation also has its physical limit according to Landauer [1,2] who proved that in logic computation every bit of information loss generates *kTln2 joules* of heat energy, where *k* is Boltzmann's constant of 1.38 $x10^{-23}$*J/K*, and *T* is the absolute temperature of the environment. At room temperature the dissipating heat is around 2.9 x 10^{-21}*J*. Energy loss by Landauer limit is important because it is likely that the growth of heat generation due to information loss will be noticeable in future. Bennett [3] showed that zero energy dissipation would be possible if the network consists of reversible gates only. Reversible logic has also found its applications in several disciplines such as quantum computing [4], nanotechnology [5], DNA technology [6] and optical computing [7].

Any digital circuit is redesigned using reversible design units. These reversible design units are called reversible logic gates. These are n×.n digital logic gates with some specific characteristics. Some characteristics of reversible logic gates are as follows:

1. Equal numbers of input and output signals.
2. Output combination at any instance accurately provides the applied input combination.
3. There is one to one mapping between input and output signals bits.
4. Low fan out.
5. Any output bit is high for half the number of total input combinations possible.

With these characteristics, various reversible logic gates have been proposed till now. Some examples of these reversible logic gates are Feyman, Toffoli, Fredkin, HNG, MHNG, DKG & DKGP gates etc. Reversible digital circuit designing approach utilizes these reverse logic gates to design target digital circuit with an approach. These reversible logic gates are used to design various digital circuits with reversible logic approach with an aim to create a loss less digital system. Figure 1 shows the block diagram of a simple n×n reversible logic gate.

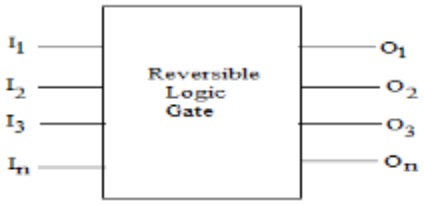


Fig. 1 Block Diagram of Reversible Gate

In this paper, improved design techniques of reversible logic implementation for 4-bit & 8-bit full adder/subtraction circuits are presented. We have compared the proposed designs with the existing ones and found that modified designs are better than the existing ones in terms of quantum cost and power dissipation.

II. REALIZATION OF LOGIC GATES

- ***Reversible DKGP Gate***

The 4* 4 reversible DKGP gate can work singly as a reversible full adder or a full subtractor. If logic 0 is given to input A of reversible DKGP gate, it works as a full adder. If logic 1 is given to input A, the reversible gate works as a full subtractor. The DKGP gate and its quantum circuit are shown in Figs. 2 and 3 respectively. From the quantum circuit, the quantum cost of DKGP gate is calculated directly as 15 as it contains 2 positive controlled TG and 5 CNOT gates.

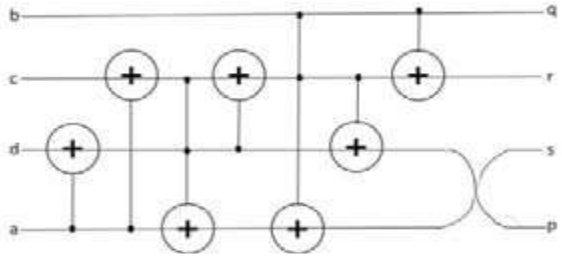


Fig. 2Quantum circuit of DKGP gate

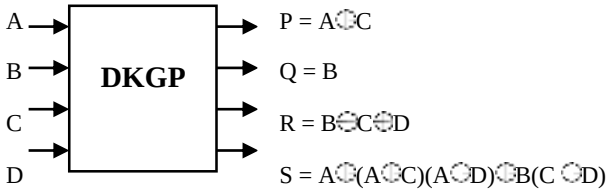


Fig. 3 Reversible DKGP gate

- ***Reversible DKG Gate***

The 4* 4 reversible DKG gate can also work singly as a reversible full adder or a full subtractor. It works as a full adder or a full subtractor when the value of input A='0' and A='1' respectively. The DKG gate and its quantum circuit are shown in Figs. 4 and 5 respectively. From the quantum circuit, the quantum cost of DKG gate is calculated directly as 17 as it contains 2 positive controlled TG, 1 negative controlled TG, and 4 CNOT gates.The DKG gate can be used as Copy, NOT, EXOR, EXNOR, AND, OR and NAND gates.

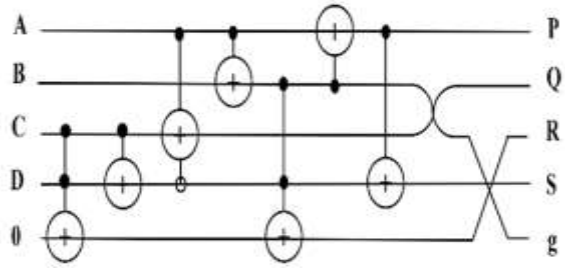


Fig. 4 Quantum circuit of DKG gate

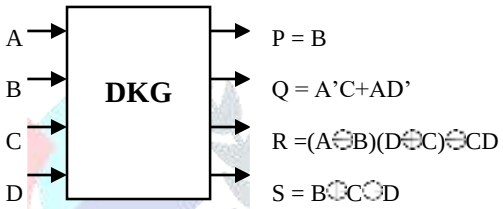


Fig. 5 Reversible DKG gate

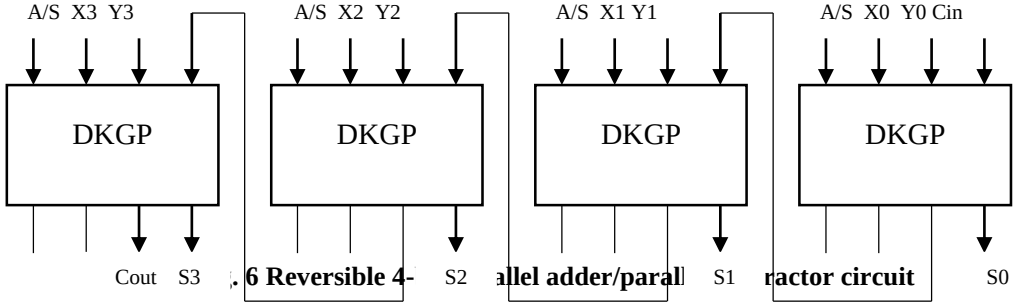
III. 4-BIT REVERSIBLE PARALLEL ADDER/SUBTRACTOR

Conventionally parallel adder/subtractor circuits are realized using full adder and EXOR gates. If the control input F='0', the circuit works as parallel adder, adding two 4-bitnumbers. If the control input F='1', the circuit works as parallel subtractor, subtracting two 4-bit numbers. This is done using 2's complement method.

Full adder/subtractor adds or subtracts two 1-bit inputs along with carry input or borrow input, producing sum/ difference and carry out/borrow out. If two n-bit numbers are to be added or subtracted, 'n' number of full adder/ subtractors are cascaded in such a way that carry out/borrow of one stage is given as carry in/borrow in of next stage so that carry/ borrow is propagated from 1st stage to last stage. This circuit constitutes parallel adder/subtractor where the inputs are applied to all the stages of the circuit simultaneously.

Proposed Design 1st : 4-bit parallel adder/subtractor using DKGP Gates

A 4-bit reversible parallel adder/subtractor implemented using the reversible DKGP gates is shown in Fig. 6. When the control input A=0, the circuit acts as a parallel adder, thus adding two binary numbers of 4 bits each and produces a 4-bit sum and a carry out. If the control input A=1, the circuit acts as a parallel subtractor, thus subtracting two binary numbers of 4 bits each and produces a 4-bit difference and a borrow out. The unused outputs are the garbage outputs.



. 6 Reversible 4- allel adder/paral ractor circuit

Proposed Design 2nd : 8-bit parallel adder/subtractor using DKG Gates

The figure 7shows the proposed design of 8-bit parallel adder/subtractor using DKG reversible logic gates. As its name suggest 8-bit so it makes use of 8 DKG gates only. In this design DKG gate serves as full adder. Each DKG gate is used to add two bits along with carry bit. The carry generated from next DKG gate is given to DKG gate and so on. Hence, the carry is propagated in a serial computation. The quantum cost of the DKG gate is 17. So the total quantum cost of the circuit is 136.

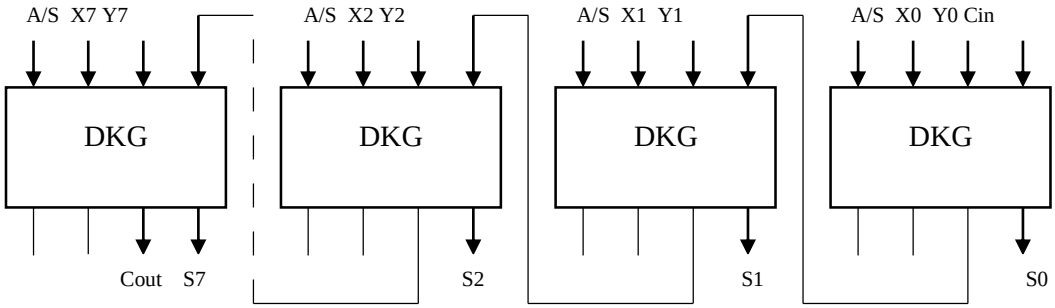


Fig. 7 Reversible 8-bit parallel adder/parallel subtractor circuit

Proposed Design 3rd : Modified 8-bit parallel adder/subtractor using DKGP Gates

A 8-bit reversible parallel adder/subtractor implemented using the reversible DKGP gates is shown in Fig. 8.

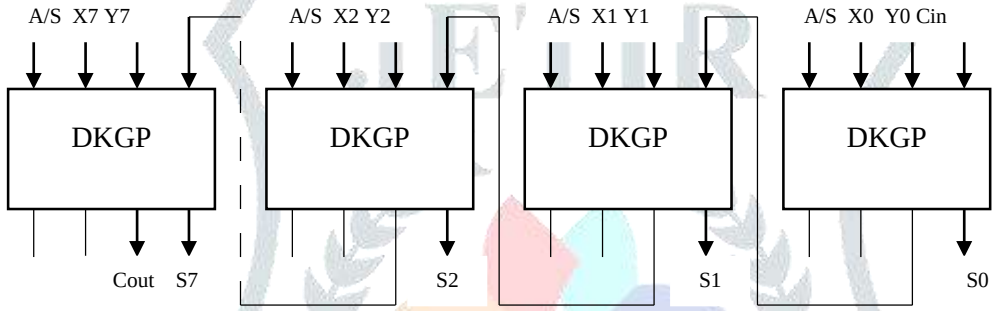


Fig. 8 Reversible Modified 8-bit parallel adder/parallel subtractor circuit

When the control input A/S=0, the circuit acts as a parallel adder, thus adding two binary numbers of 4 bits each and produces a 4-bit sum and a carry out. If the control input A/S=1, the circuit acts as a parallel subtractor, thus subtracting two binary numbers of 4 bits each and produces a 4-bit difference and a borrow out. The unused outputs are the garbage outputs. The quantum cost of the DKGP gate is 15. So the total quantum cost of the circuit is 120.

IV. IMPLEMENTATION & RESULTS

Table1: Comparison of Proposed work with Existing work

Parallel Adder/Subtractor Circuit	Quantum Cost	Power Consumption (W)
Parallel Adder/Subtractor Design [12]	68	2.722 W
Proposed 4-bit Parallel Adder/Subtractor Design [fig. 6]	60	1.478 W
Proposed 8-bit Parallel Adder/Subtractor Design [fig. 7]	136	2.559 W
Proposed Modified 8-bit Parallel Adder/Subtractor Design [fig. 8]	120	1.372 W

V. SIMULATION METHODOLOGY

The performance of the proposed design is verified by simulation using Xilinx ISE 14.4. The results obtained from the simulation for various adder/subtractor circuits are verified and shown in the fig. 9-11.

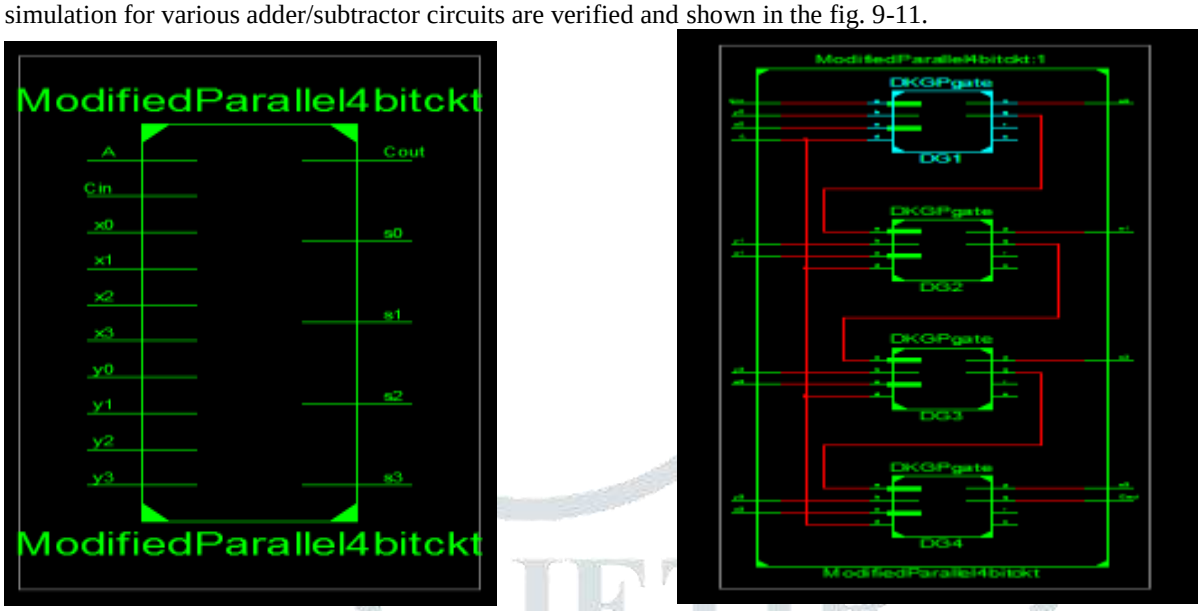


Fig. 9RTL view of proposed Reversible 4-Bit adder/subtractor circuit

The fig. 9 shows the RTL schematic of top module for our proposed reversible 4-bit paralle adder/subtractor circuit (proposed design 1st) using DKGP gates, it contains inputs a, b each of which contains 4 bits and Cin is the input carry & A as comtrol input which decides wether the circuit works as adder or subtractor. The S is the output which contains 4 bits and Cout is the output carry. The fig. 10 shows the RTL schematic of top module for our proposed reversible 8-bit paralle adder/subtractor circuit (proposed design 2nd) using DKG gates, it contains inputs a, b each of which contains 8 bits and Cin is the input carry & A as comtrol input which decides wether the circuit works as adder or subtractor. The S is the output which contains 8 bits and Cout is the output carry.

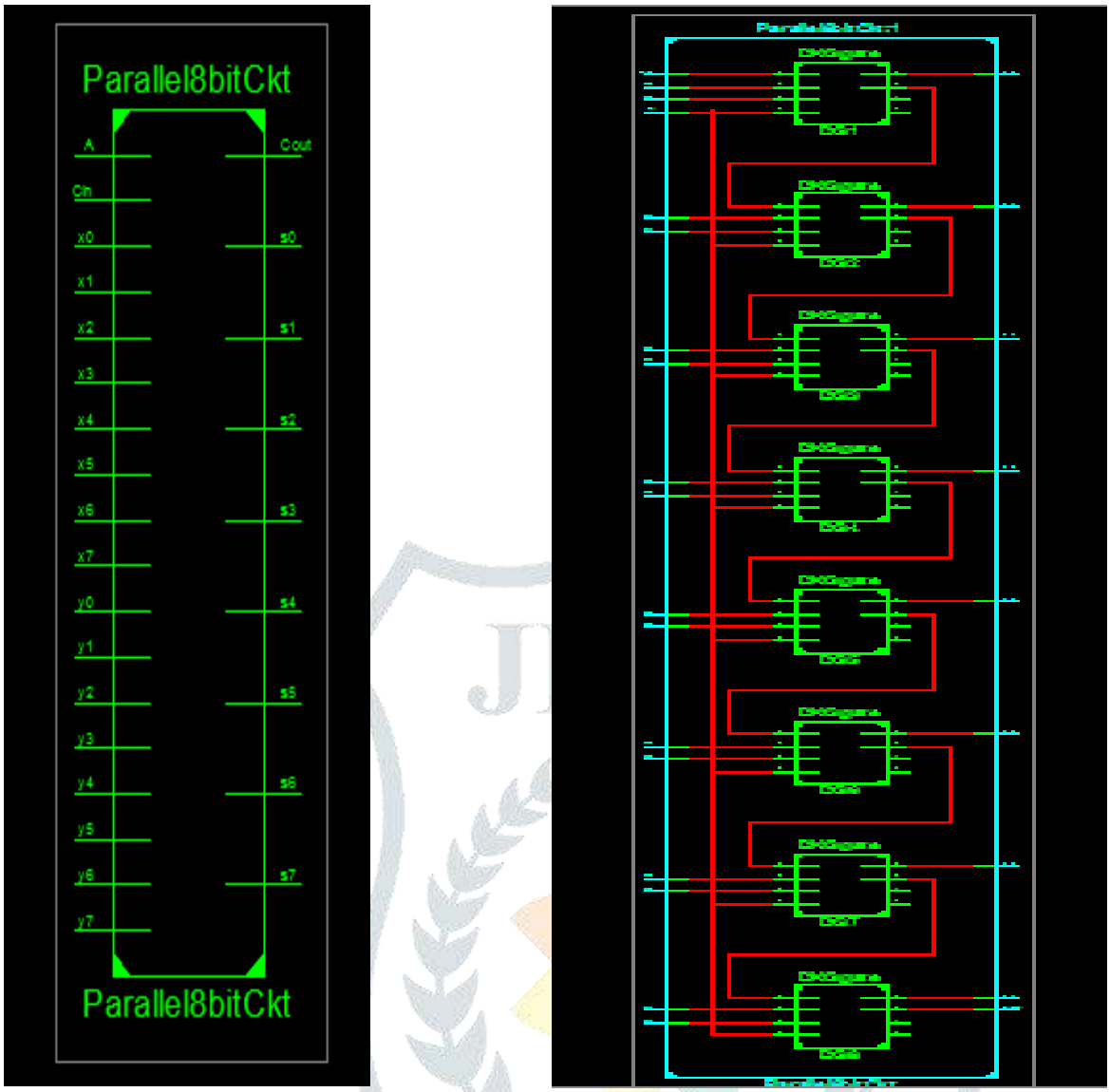


Fig. 10RTL view of proposed Reversible 8-Bit adder/subtractor circuit

The fig. 11 shows the RTL schematic of top module for our proposed modified reversible 8-bit paralle adder/subtractor circuit (proposed design 3rd) using DKGP gates, it contains inputs a, b each of which contains 8 bits and Cin is the input carry & A as comtrol input which decides wether the circuit works as adder or subtractor. The S is the output which contains 8 bits and Cout is the output carry.

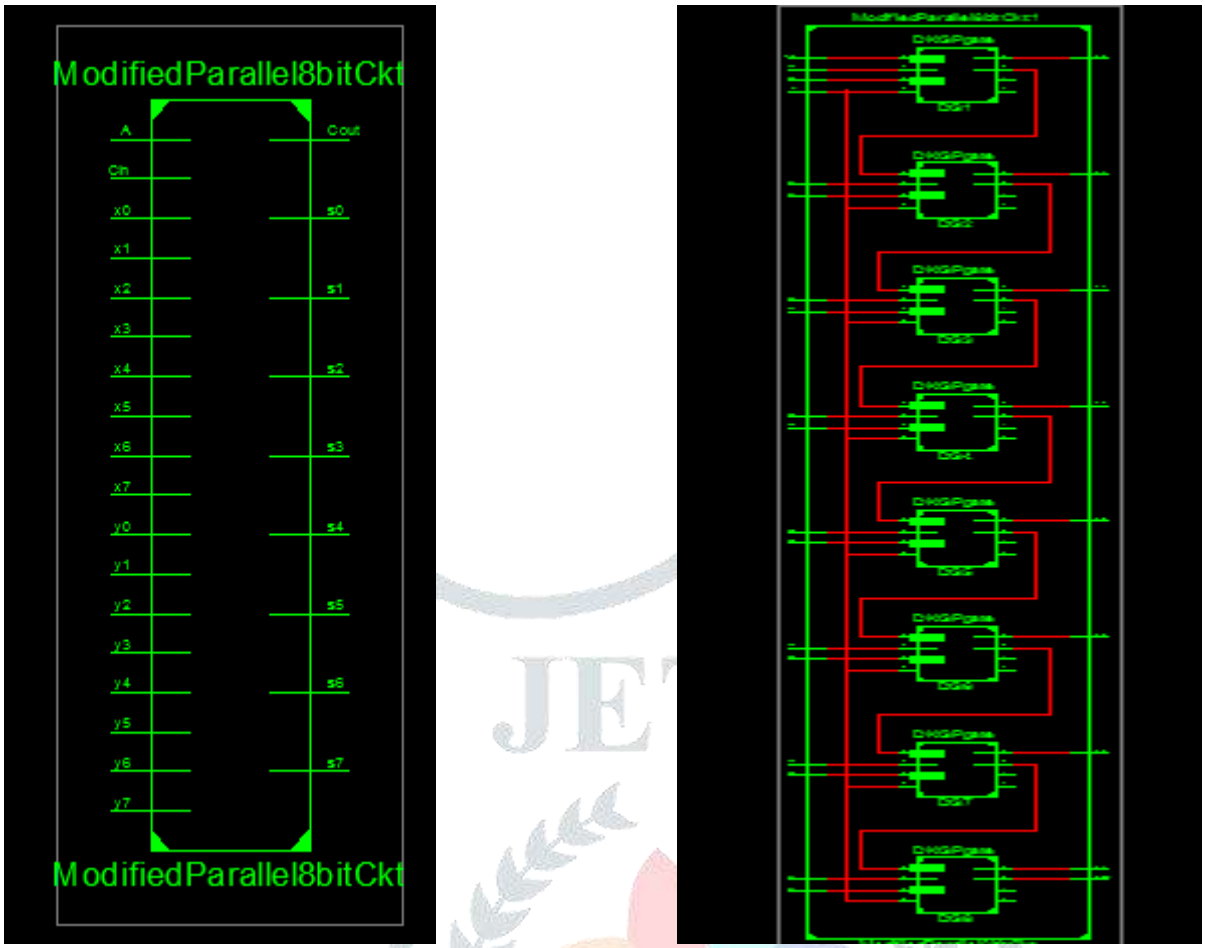


Fig. 11RTL view of proposed modified reversible 8-Bit adder/subtractor circuit

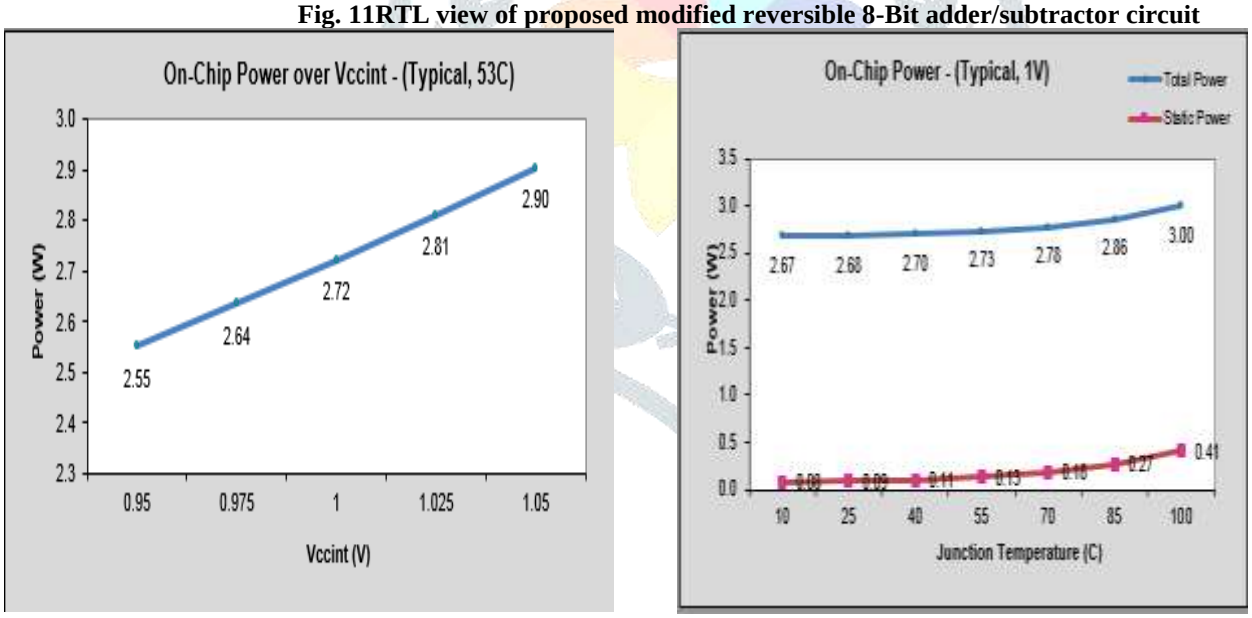


Fig. 12 Power Consumption Graph of Existing 4-bit adder/subtractor circuit [12]

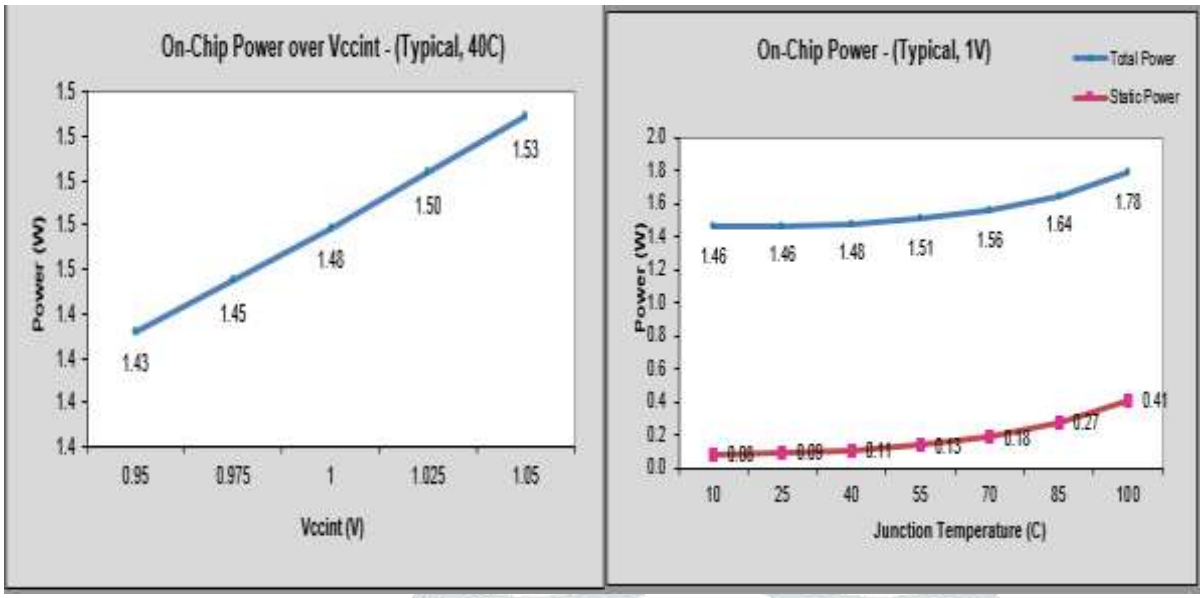


Fig. 13 Power Consumption Graph of Proposed 4-bit adder/subtractor circuit

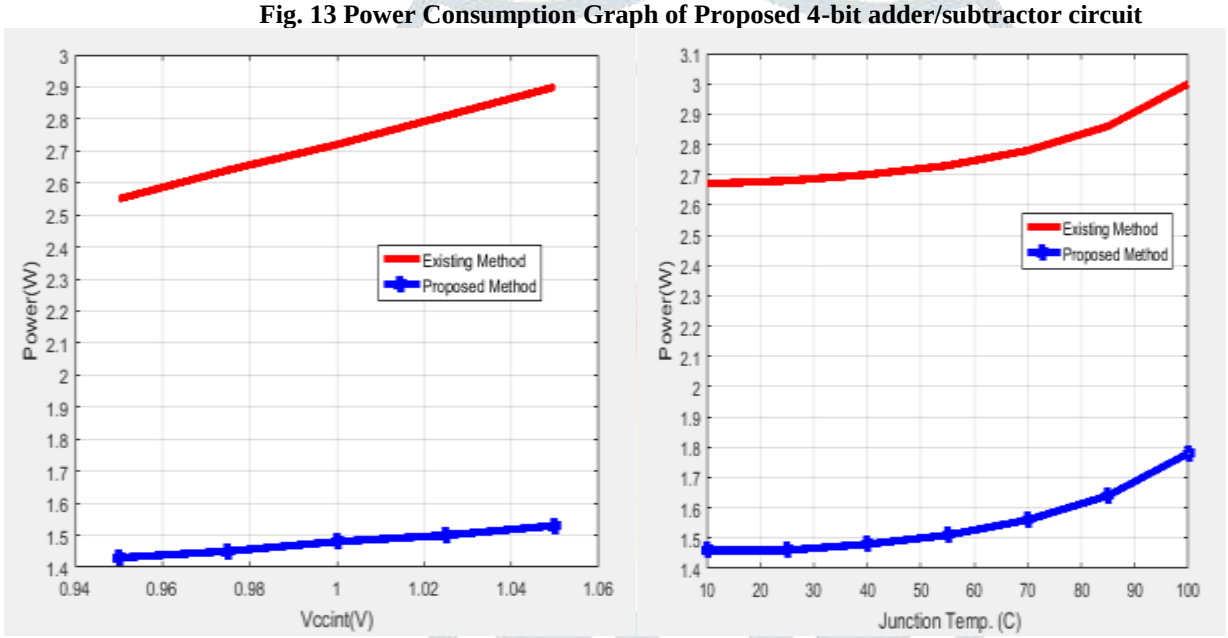


Fig. 14 Comparative Results of Power Consumption Graph for Proposed & Existing 4-bit adder/subtractor circuit [12]

In the fig. 14 the graph between the Vcc and Output power shows that the proposed design consumes 1.45 Watt power while the existing design consumes 2.72 Watt power. Simillarly the graph between the Junction Temperature and Power shows that the propose design consumes1.45 Watt power while the existing design consumes 2.72 Watt power.

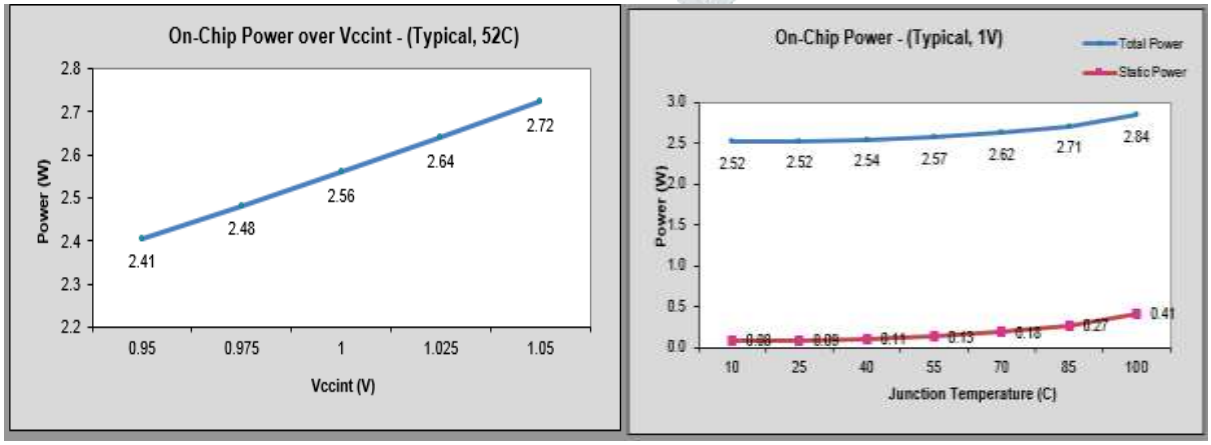


Fig. 15 Power Consumption Graph of Proposed 8-bit adder/subtractor circuit

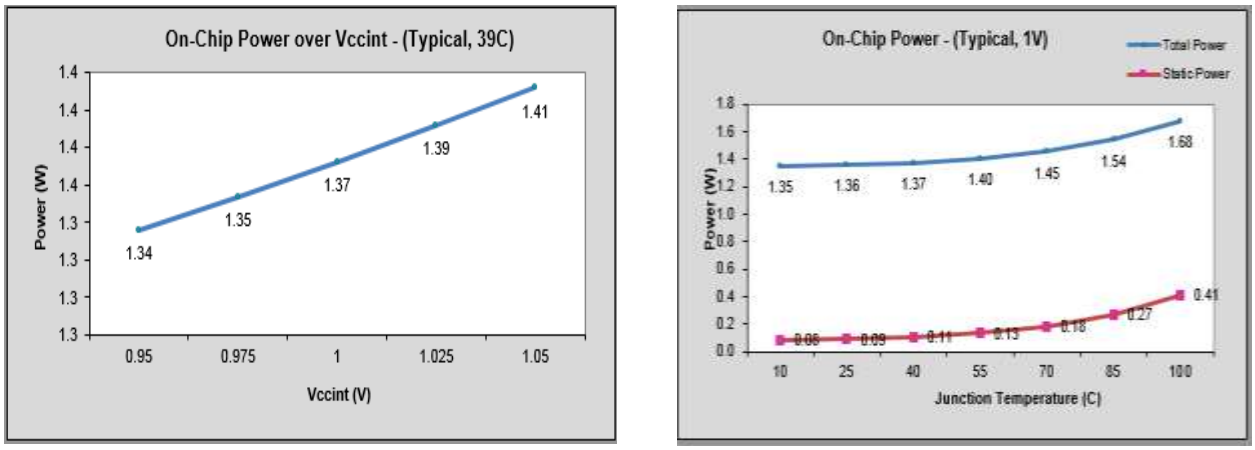


Fig. 16 Power Consumption Graph of Proposed Modified 8-bit adder/subtractor circuit

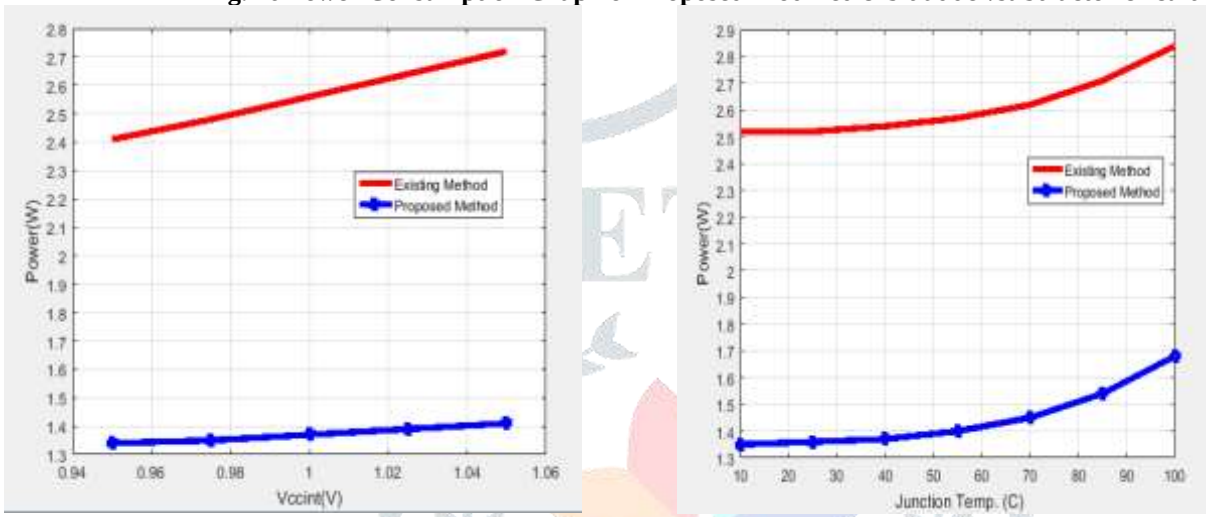


Fig. 17 Comparative Results of Power Consumption Graph for Proposed & Modified Proposed 8-bit adder/subtractor circuit

In the fig. 17 the graph between the Vcc and Output power shows that the propose design consumes 2.56 Watt power while the modified proposed design consumes 1.37 Watt power. Simillarly the graph between the Junction Temperature and Power shows that the propose design consumes 2.56 Watt power while the modified propose design consumes 1.37 Watt power.

Hence it cam be concluded that the proposed parallel adder/subtractor circuit consumes less power as compared to the existing parallel adder/subtractor circuit.

VI. CONCLUSION

This work presents the design of reversible parallel adder/subtractor circuits. The proposed designs are compared with existing design given in [12] & modified proposed design. A comparison is performed between the proposed and the existing parallel adder/subtractor circuits designs which signify that the proposed design outperforms the existing designs in terms of quantum cost and power consumption. Thus, this design forms the basis for a reversible arithmetic circuit design and contributing to no or less power dissipation. The next steps, which should be considered for future work, can design the n-bit reversible parallel adder/subtractor circuit.

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