Three-Phase Symmetrical Multilevel Inverter with reduced switches

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Abstract: ***This paper presents a new design and implementation of a three-phase multilevel inverter for distributed power generation system victimization low FM and curving pulse dimension modulation additionally. It's a standard sort and it are often extended for further range of output voltage levels by adding extra standard stages. The impact of the planned topology is its proficiency to maximize the amount of voltage levels using a reduced range of isolated dc voltage sources and electronic switches. Moreover, this paper proposes a big issue that is developed to outline the amount of the desired components per pole voltage level. A close comparison primarily based on is provided so as to categorize the various topologies of the s addressed within the literature. Additionally, an example has been developed and tested for varied modulation indexes to verify the management technique and performance of the topology. Experimental results show a well-matching and smart similarity with the simulation results.***

Keywords—Low frequency modulation, multi-level inverter, multi-level inverter comparison factor, sinusoidal pulse-width modulation (SPWM), symmetrical DC power sources, three-phase.

I. Introduction

Recently, multi-level inverters (MLIs) have gotten incredible consideration as a solitary stage inverter. Despite the fact that, they require high number of segments, yet because of their points of interest for example, creating yield voltage with to a great degree low distortion factor (DS), low dv/dt, little yield channel measure, low electromagnetic interface (EMI), and low total harmonic distortion (THD), still have awesome consideration [1]– [6]. For all intents and purposes, all of these points of interest seem emphatically as the quantity of dc-control sources expanded as on account of sustainable power source frameworks. The general idea of is to use separated dc sources or then again a bank of arrangement capacitors to create air conditioning voltage waveforms with higher abundance and close sinusoidal waveform. There are three ordinary sorts of named as Neutral point diode (NPD) clipped [7], flying capacitor [8], furthermore, fell H-Bridge [9]. All of them are experiencing expanded segments number per level, and complex control engineering [9]. Among the diverse topologies for, they can be grouped into two principle classifications: 1) single dc-source inverter such as, and inverters; 2) multi-dc sources inverters such as inverter [10]. While, multi-dc sources inverter is partitioned into symmetrical and nonsymmetrical topologies. Mainly, nonsymmetrical topologies create more voltage levels contrasted with symmetrical topologies. All of these topologies can be reached out for more voltage levels by expanding the number of the essential setup (fundamental cell). Numerous topologies were displayed in the most recent decade centering on limiting the essential multilevel topologies disadvantages. The creator in introduced a topology named multilevel dc interface. It comprises of a gathering of essential cells associated in arrangement design. Every cell produces or 0 voltage over the associated cells, there is an H-extension to change the extremity of the combined voltage. The required number of dynamic switches for yield voltage levels is for the inverters. Be that as it may, this topology requires expanded number of parts contrasted with the traditional topologies, and high voltage stresses. In any case, the creators displayed a topology named transistor-braced H-connect. The essential cell can deliver a five-levels per shaft in the yield voltage. Notwithstanding, it experiences likewise the expanded segments checks, necessities of electrolytic capacitors, complex control approach. Then again, the creators introduced three-stage uneven multi-level course inverter. The yield voltage levels combined by arrangement associated cells. For two cells arrangement, it produces four levels for every shaft. Notwithstanding, rather than utilizing H-scaffold to getting the contrary voltage polarities, it utilizes just the stage move connection between the three legs, by subtracts every leg's voltage with the neighboring one to deliver the line voltage, a similar subtraction thought was exhibited. While, the creators displayed another single dc-connect control supply topology, the introduced topology creates seventeen voltage levels (0,E/16, E/8, 3E/16, E/4, 5E/16, 3E/8, 7E/16,E/2, 9E/16, 5E/8, 11E/16, 3E/4, 13E/16,7E/8, 15E/8, 15E/16 AND E) on the yield voltage by utilizing three level flying capacitor inverter and falls H-connect. Be that as it may, this topology uses a solitary dc-control supply. It utilizes expanded number of electrolytic capacitors as coasting dc-control supplies. The creators in [16] exhibited a twofold sub-module circuit. The exhibited cell produces a three yield voltage levels over its terminals utilizing eight switches and two capacitors. It made strides the voltage adjusting over capacitors at low exchanging frequencies, anyway an additional segments contrasted and the proportional half extension modules required. A few topologies, for example, were introduced for large scale application. They fundamentally utilize a dc-air conditioning inverter stage to change over the dc yield voltage from the PV modules to the required air conditioning voltages. That in transforms changed into three air conditioning confined voltages utilizing a medium recurrence transformer having three optional windings. This setup experiences numerous constraints like expanding segments tallies, surprising expense, commotion, low effectiveness, and enormous establishment measure. In view of a settled game plan, another sub-group of was exhibited. The settled really lay in multi dc-control sources topologies class. They have two arrangements; one delivers an odd number of yield voltage levels furthermore, the other is having a place with much number of yield voltage levels. Keeping in mind the end goal to produce a four voltage levels, it requires

three dc-control supplies, four capacitors, and 18 switches. Notwithstanding, it has no diodes contrasted with the inverters however it requires two additional dc-control supplies. Plus, it utilizes electrolytic capacitors that has expanded the framework cost and size. A half and half fell inverter was displayed. Its task relies upon developing unidirectional staircases waveforms produced from an arrangement associated cells. Every cell comprises of one capacitor and four exchanging gadgets. Despite the fact that this topology utilizes just a single dc-source, however it has numerous confinements because of capacitors, presence of three-stage transformer, also, high voltage weight on the H-connect switches as the number of levels is expanded. The creators introduced an adjusted flying capacitors topology; it requires three dc-control supplies, nine capacitors, what's more, 36 changing gadgets to create five levels for shaft voltages. It experiences a similar constraint established and capacitor's voltage adjusting issues. In diverse essential cells were exhibited named as cinch twofold cell. To create three voltage levels, it requires five switches, two capacitors and two diodes. Analyzed to the half and full-connect inverters, it has higher semiconductor misfortunes than the half-connect inverter. Another essential cell is named five-level cross-associated circuit was exhibited. It creates five yield voltage levels. Be that as it may, it requires six exchanging gadgets and two capacitors for its activity. Changed cells were made by consolidating regular known essential cells, for example, half scaffold, full extension, that can be associated in arrangement, in parallel, in fell, or in cross designs. The subsequent cells plan to defeat the fundamental cells disadvantages. The subsequent cells are delegated blended substitution cells, uneven compensation cells, cross-associated substitution cells, cinched twofold compensation cells, and T-associated. Be that as it may, every one of them experience the ill effects of electrolytic capacitor constraints.

A new sub-groups of the were created. They principally comprise of a high voltage fundamental stage connected with low voltage assistant stages. The primary stage generally uses a traditional voltage source inverter or - three level inverter. It has high voltage single dc-control supply and helper fell cells either are a full H-extension or half H-connect cells. Nearly these topologies are appropriate in medium voltage applications. It has low parts considers disconnected dc-control supplies what's more, switches. By and by, it appears to have a high conduction misfortune since a zero voltage state in the post requires switches (for half H-connect) or ' (for full H-connect) be in ON-state.

Clearly, from the above overview, there are a wide range of topologies for. Some of them utilize single dc-control supply what's more, others utilize numerous dc-control supply s. Also, some of them utilize numerous electrolytic capacitors as skimming power supplies also, some of them not. All of tended to topologies experiencing expanded number of parts tallies and use of electrolytic capacitors as skimming power sources which include more confused issues in the control framework. On the other hand, presenting new topology that can comprehend the expressed challenges and proposing new factor for recognizing extraordinary topologies are exceedingly prescribed. This paper is handling to diminish the segments tally contrasted and the traditional and the tended to topologies in the writing with keeping a similar post voltage levels number. This prompts lessened inverter measure, limited exchanging misfortunes, low conduction misfortunes, also, basic control engineering. Also, an examination system in light of segments per level factor has been proposed in this paper. This factor is utilized to characterize the expected parts to deliver one voltage level over the yield post. In this manner, it goes about as a correlation device that is portraying how the distinctive topologies of completely use their segments. This factor is characterized in (1). In the event that this factor has a high esteem, this shows an expansive number of parts tallies is required to deliver one post voltage level and the other way around. Consequently, the examination target is to diminish this factor

$$F_{\frac{C}{L}} = \frac{N_C + N_D + N_{SW} + N_{PS} + N_{tsf} + N_X}{N_{Pole}}. \quad (1)$$

TABLE I
MLI TOPOLOGIES COMPARISON

Presented in		N_{Pole}	N_{PS}	N_{SW}	N_D	N_C	N_{tsf}	$F_{C/L}$
[11]		3	3	18	0	0	0	7.0
[12]		5	3	15	12	6	0	7.2
[13]		3	6	12	0	0	0	6.0
[14]		3	1	9	12	2	0	8.0
[15]		17	1	48	0	12	0	3.6
[16]		3	1	24	0	6	0	10.3
[17]		3	1	28	0	0	3	10.7
[18]	(a) four-level	4	3	18	0	4	0	6.3
	(b) five-level	5	3	24	0	4	0	6.2
	(c) six-level	6	5	30	0	6	0	6.8
[19]		12	1	144	0	35	3	15.2
[20]		5	3	36	0	9	0	9.6
[21]	(a) the half-bridge based cell	3	1	12	0	6	0	6.3
	(b) the full-bridge based cell	5	1	24	0	6	0	6.2
	(c) the clamp-double	3	1	15	6	6	0	9.3
	(d) the three-level FC	3	1	12	0	6	0	6.3
	(e) the three-level NPC	3	1	12	6	6	0	8.3
	(f) the five-level cross-connected SM	9	1	36	0	12	0	5.4
[22]	(a) Mixed commutation cells	4	1	18	0	6	0	6.3
	(b) Asymmetrical commutation cells	4	1	18	0	6	0	6.3
	(c) Cross connected commutation cells	5	1	24	0	6	0	6.2
	(d) Clamped double commutation cells	4	1	15	6	6	0	7.0
	(e) T-connected NPC using BB switch	3	1	12	0	6	0	6.3
	(f) Alternative Active 3-L NPC	3	1	18	0	6	0	8.3
[24]	Hybrid MLI topologies	6	7	30	0	0	0	6.2
[25]		7	8	36	6	0	0	7.1
[26]		6	13	30	0	0	0	7.2
[27]		3	4	12	0	0	0	5.3
[28]		3	6	12	0	0	0	6.0
[29]		4	3	11	20	0	0	8.5
[30]		5	3	18	24	6	0	10.2
[31]		5	6	24	0	0	0	6.0
[32]		5	6	24	0	0	0	6.0

Table I shows the computed factor for the conventional types of the multilevel inverters and the introduced topologies .From this table, it is clear that the topology presented in records the lowest value for this factor and so it requires the smallest count of the components to produce the same voltage level number.

II. PROPOSED MODULAR MLI

Another measured three-stage MLI with lessened segments include is proposed and examined this paper. The proposed three phase symmetrical inverter is appeared in Fig. 1(a). Each arm comprises of arrangement association of fundamental cells with an arrangement associated switch, for instance arm an is comprises of one cell associated in arrangement with switch Q_1. Including the basic dc voltage source (E) in to each arm shapes the shaft, making the post voltages (VAo, VBo,VCo) With a specific end goal to acquire the zero state post voltage another change Q_2 is added to the shaft, likewise Q_4 and Q_6 for shaft (B) and (C). Fig. 1(b) demonstrates the essential fundamental cell, where every cell comprises of two switches s1 and s2 and single dc voltage source. The two switches work in a corresponding mold. Along these lines, every cell can deliver two voltage levels (0, E): when S_1 in ON-STATE, zero voltage is created over the cell terminals, and when S_2 in ON-STATE, E volt is connected over the cell terminals. Moreover, utilizing just a single cell per each post and applying reasonable control signs to the s_1,s_2,Q_1 and Q_2, three voltage levels for every shaft (i.e. 0,E ,2E) are created. The yield post voltage for cells associated in arrangement is appeared in Fig. 1(c).

Table II outlines the diverse exchanging states and the comparing yield voltages for both the fundamental cell and the shaft voltage (V_{A0}) of the proposed MLI topology. The proposed topology is a

particular kind in this manner it can be stretched out to any levels. Conditions (2)– (5) give the relations of the proposed topology as

$$N_{\text{Pole}} = N_{\text{Cell}} + 2 \quad (2)$$
$$M_{\text{Level}} = 2N_{\text{Cell}} + 3 \quad (3)$$
$$N_{SW} = 3(2N_{\text{Cell}} + 2) \quad (4)$$
$$N_{PS} = 3N_{\text{Cell}} + 1. \quad (5)$$

Then for the example of NCell = 1, Npole = 3 , [based on(2)] which is the pole voltage levels and M_{Level}=5 [based on (3)] which is the output line-to-line voltage levels. Note that the number of output phase voltage levels N_{ph} will be derived to be seven levels in low frequency modulation and nine levels for high frequency modulation.

III. MODULATION TECHNIQUES FOR THE PROPOSED MLI

The MLI modulation techniques are classified into two main groups according to the switching frequency used to

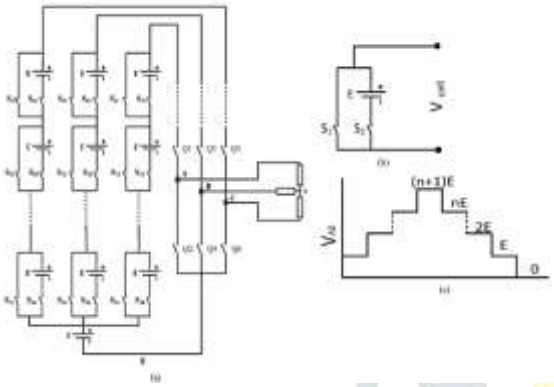


Fig. 1. (a) Generalized power circuit of the suggested three-phase symmetrical MLI. (b) Basic cell. (c) Pole voltage (V_{A0}) waveform for -cell.

TABLE II
DIFFERENT SWITCHING STATES AND THE CORRESPONDING OUTPUT VOLTAGES

Switching states	Switch				Basic-unit Output voltage	Pole voltage (V_{A0})
	S_1	S_2	Q_1	Q_2		
1	ON	OFF	ON	OFF	0	E
2	OFF	ON	ON	OFF	E	$2E$
3	OFF	OFF	OFF	ON	-	0

drive inverter switches: 1) low frequency modulation technique, 2) pulse-width modulation (PWM) techniques that cover conventional techniques PWM, sinusoidal pulse-width modulation (SPWM), space vector pulse-width modulation(SVPWM), sub-harmonic pulse-width modulation(SHPWM), and switching frequency optimal pulse-width modulation (SFO-PWM). In this paper, two modulation techniques are investigated to achieve sinusoidal output voltages waveforms as described in the following.

A. Low Frequency Modulation Technique

The low frequency modulation is considered as the basic modulation technique due to its lower switching frequency than the other modulation methods. It causes the switching loses reduced dramatically. In order to investigate the performance of the proposed MLI, a three levels per pole by using single basic cell in each pole is used as shown in Fig. 2. It is simulated via PSIM and MATLAB/SIMULINK software packages. In order to generate the required switching signals for the proposed MLI, a rectified sine waveform has a frequency equals to the output voltage frequency (50 Hz) is compared.

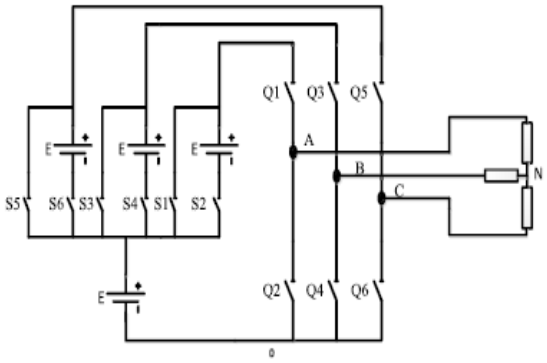


Fig. 2. Proposed three-phase MLI topology.

With a dc voltage signal has an amplitude equal to half of the sine wave amplitude as shown in Fig. 3. The intersection points between them identify six periods (P_1 to P_6). Four switching signals are constructed from these periods combination in order to generate a sinusoidal output voltage. The control equations for the (S_1, S2, Q1, and Q_2) are given in (6)–(9), respectively. The same scenario is applied to inverter

TABLE III
SWITCHING STATES OF THE PROPOSED TOPOLOGY (SWITCH ON: 1, S WITCH OFF: 0)

V_{AB}	V_{BC}	V_{CA}	S_1	S_2	Q_1	Q_2	S_3	S_4	Q_3	Q_4	S_5	S_6	Q_5	Q_6
E	$-2E$	E	1	0	1	0	0	0	0	1	0	1	1	0
$2E$	$-2E$	0	0	1	1	0	0	0	0	1	0	1	1	0
$2E$	$-E$	$-E$	0	1	1	0	0	0	0	1	1	0	1	0
$2E$	0	$-2E$	0	1	1	0	0	0	0	1	0	0	0	1
E	E	$-2E$	0	1	1	0	1	0	1	0	0	0	0	1
0	$2E$	$-2E$	0	1	1	0	0	1	1	0	0	0	0	1
$-E$	$2E$	$-E$	1	0	1	0	0	1	1	0	0	0	0	1
$-2E$	$2E$	0	0	0	0	1	0	1	1	0	0	0	0	1
$-2E$	E	E	0	0	0	1	0	1	1	0	1	0	1	0
$-2E$	0	$2E$	0	0	0	1	0	1	1	0	0	1	1	0
$-E$	$-E$	$2E$	0	0	0	1	1	0	1	0	0	1	1	0

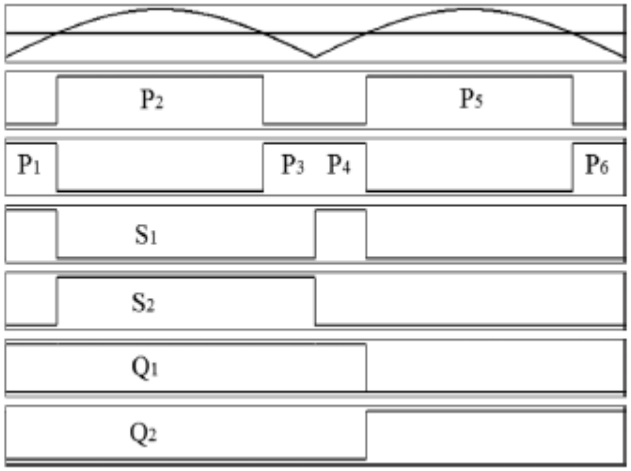


Fig. 3. Switching patterns for low frequency modulation technique.

Poles (V_{B0}) and (V_{C0}) after shifting the basic sinusoidal voltage with -120, 120, respectively. Therefore, the required switching signals for the overall three poles can be generated.

$$S_1 = P_1 + P_4 \quad (6)$$
$$S_2 = P_2 + P_3 \quad (7)$$
$$Q_1 = P_1 + P_2 + P_3 + P_4 \quad (8)$$
$$Q_2 = P_5 + P_6 \quad (9)$$

Where (+) stands to logic OR. Balancing three phase output voltage can be achieved by operating the MLI according to switching states shown in Table III. The suggested MLI has 12 modes of operation per one cycle. It is essentially to note that: when switches Q1, Q2 and Q5 are in OFF-STATE, switches S_1*to* S_6 have two possibilities for operation. Switches S_1*to* S_6 may be in ON-STATE or at OFF-STATE. Both of them will not affect the output waveforms. However, keeping switches S_1*to* S_6 in the OFF-STATE will reduce the overall voltage stresses on Q1, Q3 *and Q5*

B. Sinusoidal Pulse-Width Modulation Technique (SPWM).

The straight way to generate the SPWM signals is to compare a sinusoidal waveform signal with a triangular waveform. The comparison operation will produce the Boolean signals that are required to synthesize the switches control pulses. The SPWM technique is successfully applied for the proposed topology. Two different approaches have been proposed as follows.

1) Scheme I: SPWM Using Single Carrier Signal: This scheme uses one carrier signal centered with the sinusoidal modulation signal (sine waveform), and it has an amplitude equal to peak-to-peak value of the modulation signals as shown in Fig. 4. It worth mentioning that the modulation signal is shifted by dc level equals to (CR/2), where CR is the carrier signal amplitude. The resulted Boolean output from the comparison between the carrier and the modulating signal produces the main pulse signal G_1. Also the pulse signal GP_1 is generated by comparing the modulating signal with zero value. After logical processing on $G_1$and GP_1, the switching pulses S_1, S2, Q1 and Q_2 can be generated as specified in (10)–(13).

$$S_1 = (G_1 \times \overline{GP_1}) + (\overline{G_1} \times GP_1) \quad (10)$$
$$S_2 = (G_1 \times GP_1) \quad (11)$$
$$Q_1 = GP_1 + \{(G_1 \times \overline{GP_1}) + (\overline{G_1} \times GP_1)\} \quad (12)$$
$$Q_2 = \overline{\{\overline{GP_1} \times \overline{(G_1 \times \overline{GP_1})}\}} \quad (13)$$

Where (X) stands for logic AND, (+) stands for logic OR, (-) stands for invert, and S_1, S2, Q1 and Q_2 are the signals which will be applied to the gates drive belong to switches, respectively. In order to avoid dc-power sources short circuit, (S_1, S2) and (Q1, Q2) operate in a complementary mode with dead time.

2) **Scheme II: SPWM Using Two Carrier Signals**: This plot contrasts single regulating sign and two indistinguishable also, moved in level bearer signals. The two have abundancy break even with the tweaking signal pinnacle. Furthermore, the transporter signals are moved by a dc counterbalance equivalents to the transporter flag abundancy (CR_1) as appeared in Fig. 5. Utilizing a similar technique followed in conspire I, plot II can be executed. Be that as it may, because of utilizing two bearer signals, there are two Boolean signs named G_1 what's more, G_2 came about because of the examination. Via Carrying out a few coherent activities on these two signs (G_1, G2) as given in

(14)– (17), the required control beats for MLI can be acquired

$$S_1 = (G_1 \times \overline{G_2}) \quad (14)$$
$$S_2 = G_2 \quad (15)$$
$$Q_1 = \overline{\overline{G_2} \times \overline{(G_1 \times \overline{G_2})}} \quad (16)$$
$$Q_2 = \overline{G_2} \times \overline{(G_1 \times \overline{G_2})}. \quad (17)$$

SIMULATION RESULTS:

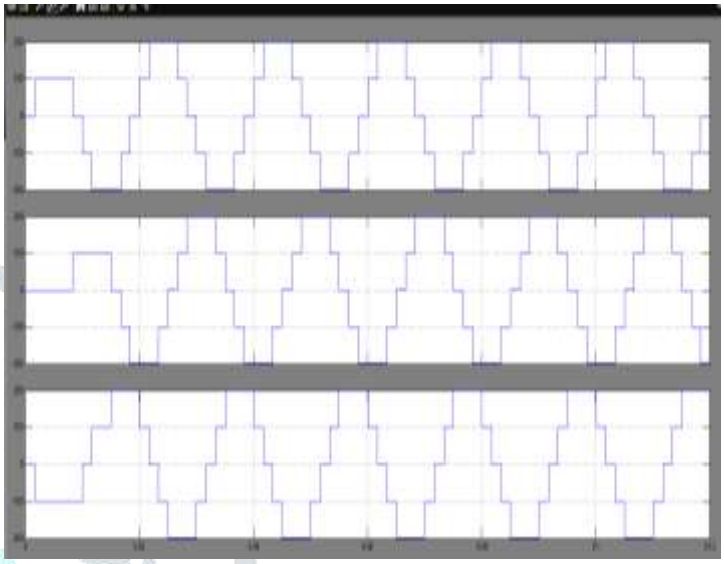


Fig. 4. Output phase voltages (Vab, Abc, and Vca ,) with low frequency (50 Hz)modulation technique.

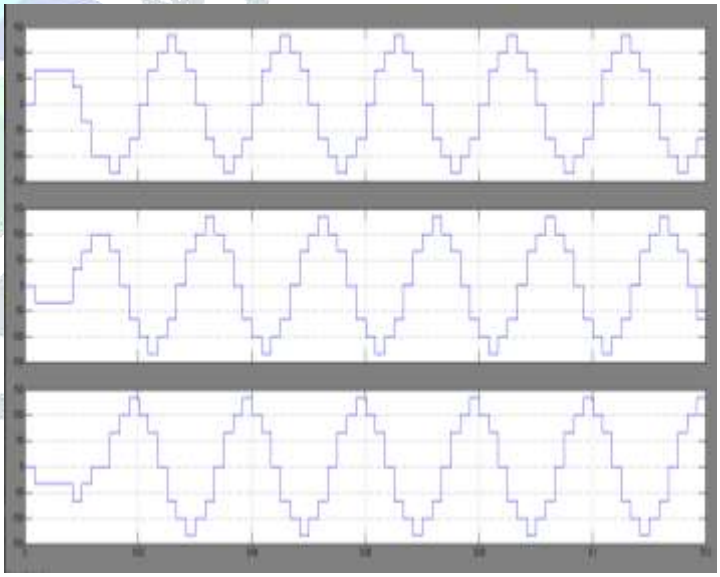


Fig. 5. Output phase voltages (Van, Abn, and Vcn ,) with low frequency (50 Hz)modulation technique

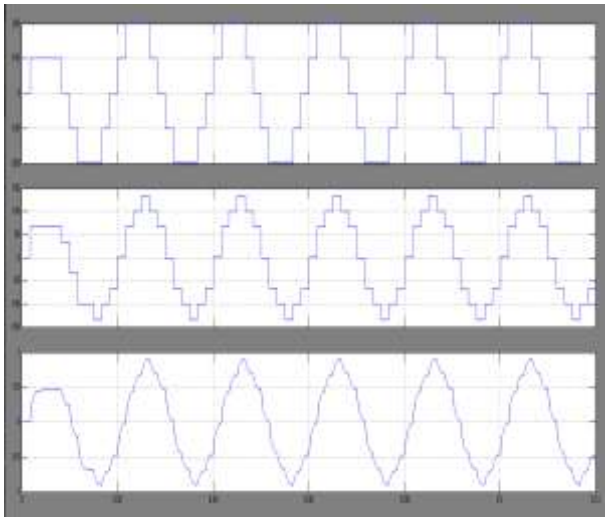


Fig. 6. Inverter outputs with R- L load (Vab, Van and Ian) with low frequency modulation technique.

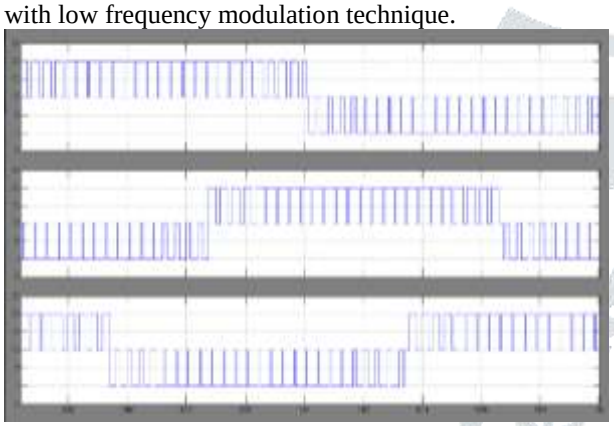


Fig.7. Pole voltages for scheme I, m_i =0.95 and fs =2.5 kHz.

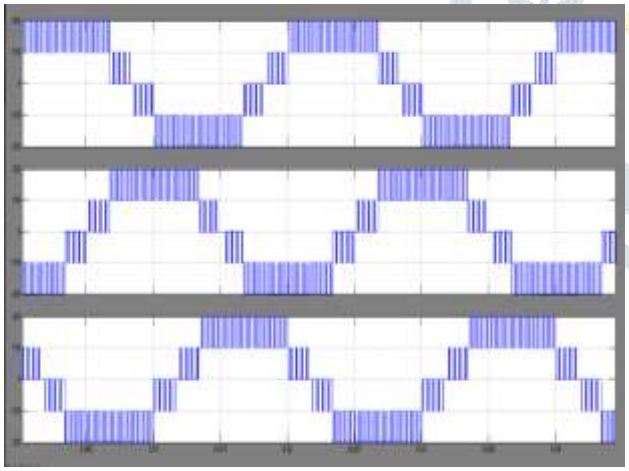


Fig.8. Line-to-line voltages for scheme I, m_i =0.95 and fs =2.5 kHz

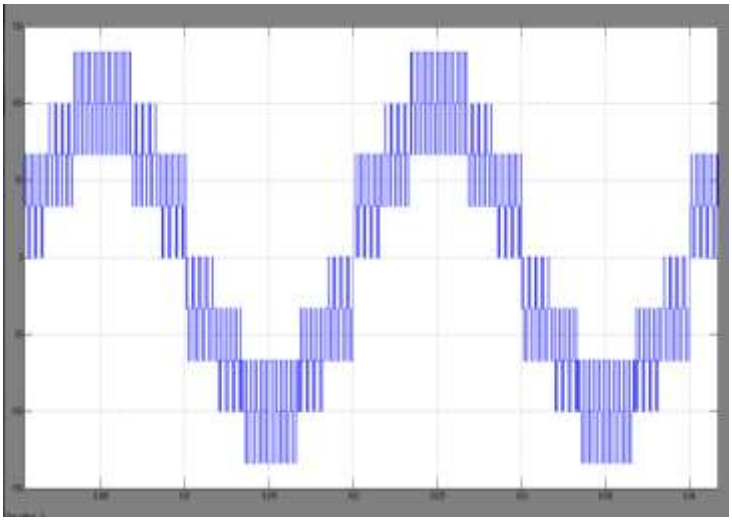


Fig.9. Phase voltages for scheme I, mi =0.95 and fs =2.5 kHz.

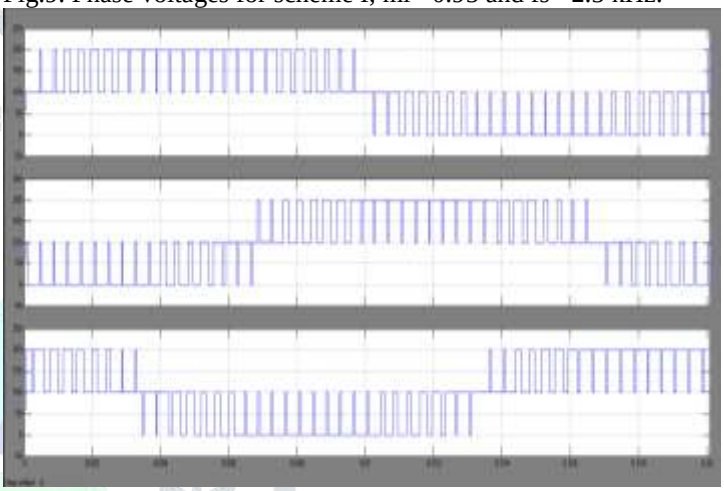


Fig. 10. Pole voltages for scheme II, m_i =0.95 and fs =2.5 khZ

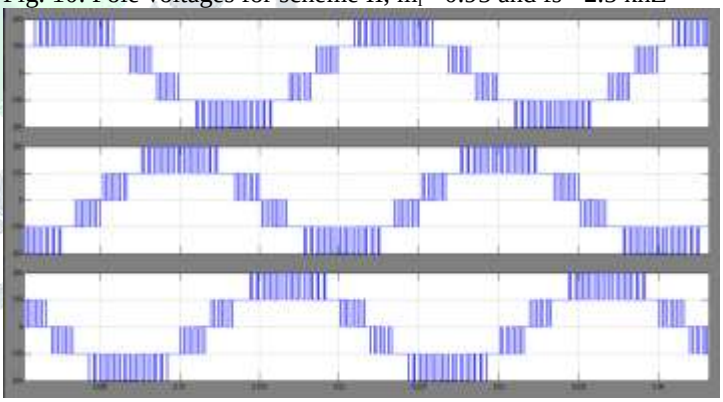


Fig. 11. Line-to-line voltages for scheme II, m_i =0.95 and fs =2.5 kHz.

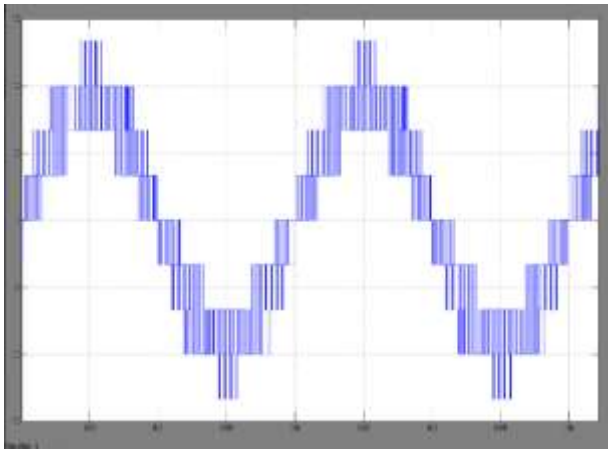


Fig.12. Phase voltages for scheme II, m_i =0.95 and fs =2.5 kHz.

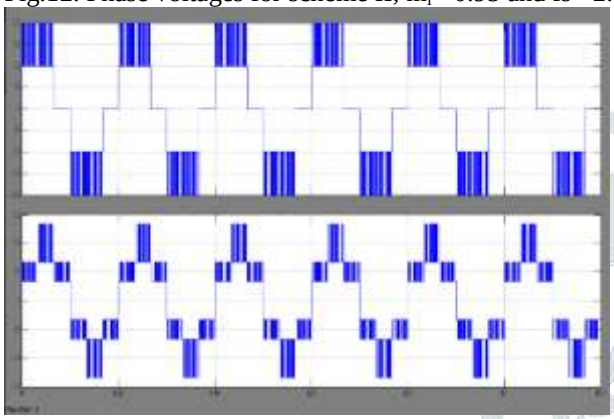
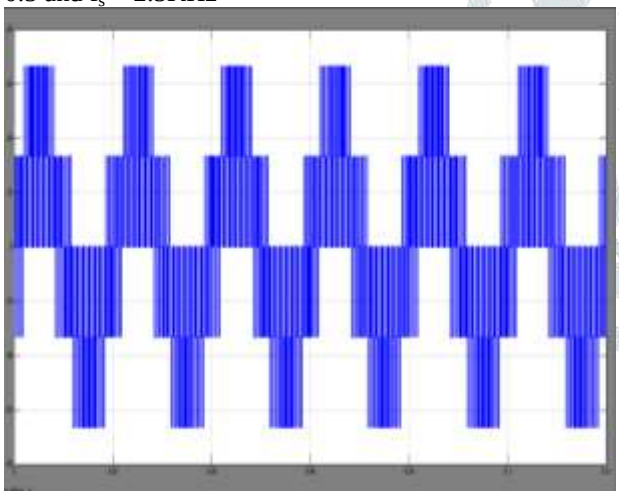
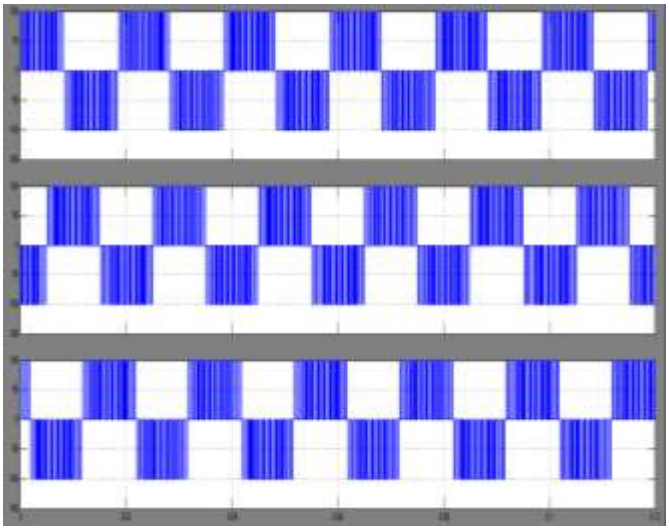


Fig. 13. Line-to-line voltage and phase voltage at for scheme I, m_i = 0.5 and f_s = 2.5KHz



A. Phase voltage



b. Line to line voltagesFig.

Fig14. Line-to-line voltage and phase voltage for scheme II, m_i = 0.5 and f_s = 2.5KHz

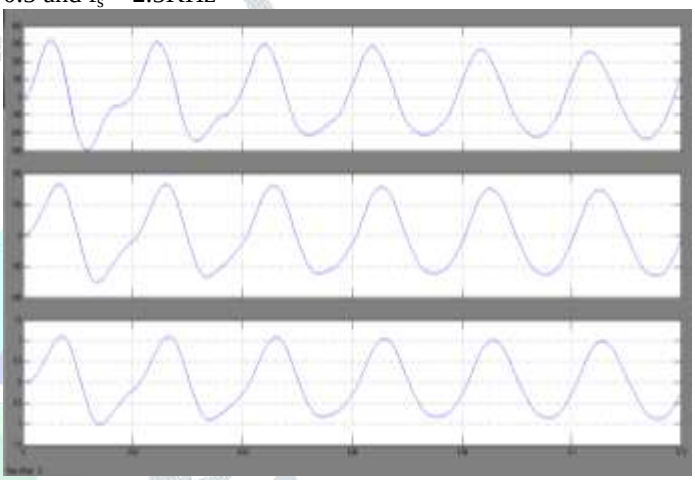


Fig.15. Inverter output voltages: (a) three phase line-to-line voltages (b) line-to-line voltage, phase voltage and the phase current under R-L load.

Conclusion

Another secluded multilevel inverter (MMLI) topology utilizing two tweak control methods is introduced. The proposed MLI has a few focal points contrasted and existing MLIs topologies. A lower number of segments consider such confined dc-control supplies, exchanging gadgets, electrolyte capacitors, furthermore, control diodes are required. So it displays the benefits of high productivity, bring down cost, improved control calculation, littler inverter's impression and expanded the general framework dependability. Because of the particularity of the displayed topology, it can be expanded to higher stages number prompts a decent execution issues, for example, low dv/dt, low EMI , and low THD and dispensing with the yield channel will be acquired. Alongside the low recurrence adjustment, two SPWM plans are effectively connected to control the recommended MLI. This paper likewise proposes a noteworthy factor $F_{c/L,}$ which characterizes the required segments to create one voltage level over the yield post terminals. The issue identified with the cost of each utilized segment is out of extent of this paper. The framework reenactment model and its control calculation are created utilizing MATLAB programming bundle apparatuses to approve the proposed MLI topology. A research facility model has been created and tried for different balance lists to check the control systems and execution of the

topology, the comparability between the recreation also, got trial comes about was affirmed.

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