AN EFFICIENT PLACE AND ROUTE IN VLSI PHYSICAL DESIGN

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Abstract:

In this project the series of steps are followed in Place and Route to meet the desired constraints efficiently using a cadence encounter tool for a Design. Placing logic cells, clock tree building and routing are the main steps followed in Place and Route. During this process mainly focus is done on CTS building by varying variables in the specification file and clearing fan-out violations by using cloning of cells through TCL scripting after route stage. Optimization techniques are used to meet desired timing constraints in each step in the design flow.

Keywords – flow, CTS, fan-out, TCL scripting.

I. INTRODUCTION

Very-large-scale integration (VLSI) design is an Integrated Circuit (IC) developing process where a single chip which is an integration of transistors in millions in the form of cells for a design functionality specified by the client. Based on the client specifications required for a design, behavioral and logical synthesis will be done by the corresponding synthesis teams. After logical synthesis net-list will be generated. The generated inputs will be given to physical design engineers whereby through graphical user interface, design will be analyzed at each stage of the place and route flow.

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VLSI Physical design is a process of transforming structural representation (net-list) into layout representation which can be manufactured by satisfying a set of constraints. The net-list consists of a logical description of cells with their connectivity in the circuit. Time delays, required area, power dissipation, and process technology of the design are included in constraints. The flow shown below represents the challenges that must be addressed by a physical design intended for designs.

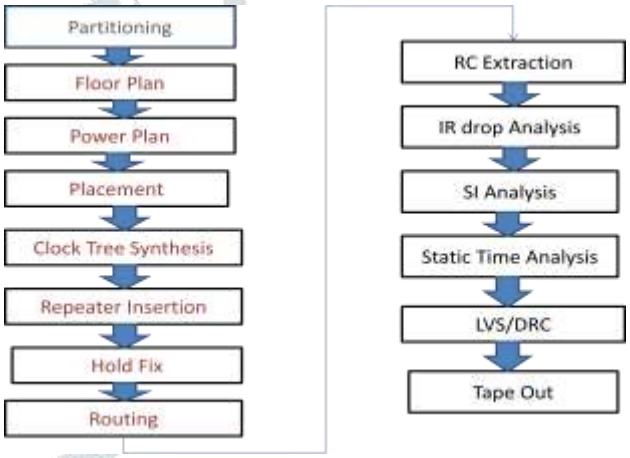

Fig 1: Physical design flow

In the design flow shown above, at clock tree synthesis stage the tree laid for the clock which decides the functionality of the chip should be more efficient. To make clock tree building efficient different experiments on the specification file (shortly spec file) was done. By this experiment we can know the required specifications to be given in the spec file such as max delay, max skew, max transition etc.., of the cells. At the route stage due to the real routing comes in to existence net delays were considered. Fan-out violations can be cleared once route stage completed, these violations are

cleared by using the cloning of cells through TCL scripting.

The remaining explanation of the paper will be explained as mentioned as below. Section II about work done related to the proposed method, Section III explains proposed methodology, Section IV shows experimental results of the design, Section V gives the conclusion about the implementation done for the design.

II. RELATED WORK:

Clock tree synthesis will be done the tool itself automatically once the floor plan, power plan, placement of the design completed, but according to the need required to build CTS we can constraint the design by changing specification file. Non default rule (NDR) to be specified after placement so that the clock nets will have double width and double spacing by which clock frequency will be more compared to other nets. Once NDR was done specification file to be generate to build CTS for which NDR will also get applied. After routing stage fan-out violations can be decreased without effecting timing. The above two experiments for the design are explained below.

1. Specification file

Default specification file will be generated by the tool according to the design constraints. In this specification file variables like maximum skew, maximum transition value, maximum delay, and usable buffers with different drive strengths are declared to build CTS of the design. By varying these variables in the specification file and with different runs in the cadence encounter tool we can conclude the final specifications with which effective clock tree can be build. The flow of changing spec file and working on the CTS can be observed from the step by step iteratively as shown in the below fig 2.

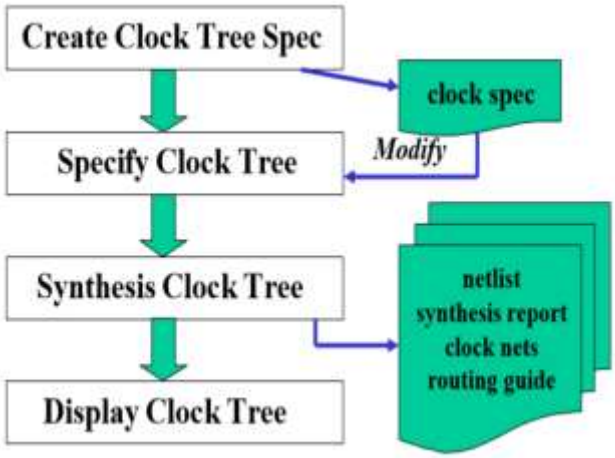

Fig 2: CTS spec file generation flow

2. Fan-out violations cleared using cloning

After the routing stage fan-out violations can be cleared, so that the driving capability of the cells can be made better. Cloning is one of the techniques used to overcome this problem so that the driving capability can be split to other same type of cell. This can be well understood by observing the following fig 3.

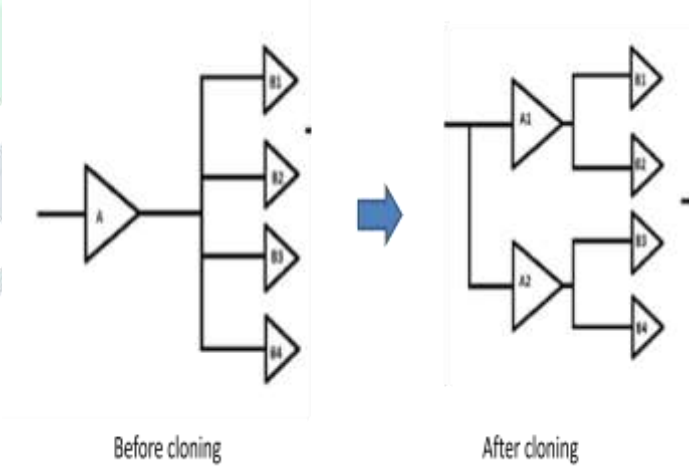

Fig: cloning to reduce fan-out problem

III PROPOSED METHODOLOGY:

In the place and route the main target is to build the clock tree efficiently such that clock should reach each flip-flop so that functionality of the design will not go. To make clock much efficient in the proposed method with different

experiments are been done with different drive strength cells. The main reason to use different drive strength cell is to reduce the delays, transition and skew of the cells. For example if there is requirement of buffer with drive strength of 8 and availability will be buffer with drive strength of 24. Transition time will decrease but delay will affect as the drive strength 24 is having more size.

In the proposed method with three different experiments are been done cells with drive strength less than 8, more than 8 and all drive strength. After clock tree building by observing the clock transition, skew, and delays from clock report generated after CTS run, using all drive strength cells got the best results. After CTS next stage routing will be done for the design. Once routing gets completed, engineering change order (ECO) stage is the stage we can interact with the tool and can do changes. In the design the fan-out violations are obtained which we can clear at ECO stage. Here proposed a method to clear violations by cloning cells which has high fan-out i.e., having more cell as load through TCL scripting.

IV IMPLEMENTATION AND RESULTS:

Step 1: In the cadence encounter tool while Place and Route flow we should take care of floor-plan and power-plan calculations from which we can get effective congestion and timing utilization. After power-plan, in the placement stage scan cells by reordering and spare cells all over the design should be added as per the guidelines given.

Step 2: In the CTS stage different runs are done with the following constraints used and results are showed as below

variables	values
Maxdelay	0.01ns
Mindelay	0 ns
Maxskew	250 ps
sinkMaxTran	200 ps
BuffrMaxTran	200 ps
Detail Report	YES
OptAddBuffer	YES

Fig 4: Input variables of specification file

parameters	Low Drivestrength Cells (less than 3)	High Drivestrength Cells (more than 8)	Both Low & High Drivestrength Cells
No of buffers	80	11	11
No of levels	6	2	2
Rise/Fall skew	75.4 ps	49.2 ps	41.4 ps
Max Rise / Fall Buffer Tran	440.3 / 379.2 ps	487.6 / 285.1 ps	41.4 / 253.1 ps
Max Rise / Fall Sink Tran	1066.2/906.1 ps	199.5 / 177.1 ps	195 / 173 ps
Min Rise / Fall Buffer Tran	79.5 / 71.3 ps	225.9 / 192.5 ps	221.6 / 192.9 ps
Min Rise / Fall sink Tran	216.2 /188.5 ps	150.2 / 131.1 ps	150.1 / 130.3 ps
View slow : skew	75.4 ps	49.1 ps	41.4 ps
View fast : skew	93.5 ps	43.2 ps	34.2 ps

Fig 4: clock report generated

Step 3: In the route stage real routing will be done by the tool where the net delays come to consideration. Once the routing gets completed in the ECO stage, the TCL script written to clear fan-out violations is sourced. Fan-out violations are get reduce from 15 to the value 3.

V. CONCLUSION:

The place and route in the VLSI design has become efficient by using:

1. Both low and high drive strength cells with skew of 34 ps.

2. Decreased fan-out problem which will effect timing.

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