Design and analysis of a 5:32 Address decoder for a high speed SRAM based

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Abstract— Address Decoder is an important digital block in SRAM which takes up to 50% of the total chip access time and notable amount of the total SRAM power in normal read/write cycle. To design address decoder need to consider two objectives, first selecting the good circuit technique and second sizing of transistors in circuit. Novel address decoder circuit is presented and analyzed in this paper. Address decoder using NAND-NOR alternate stages with predecoder and replica inverter chain circuit is proposed and compared with traditional and universal block architecture, using UMC 90nm CMOS technology.

***Index Terms*— Access time, Block Architecture, Decoder, CMOS , SRAM,**

I. INTRODUCTION

SRAM IP cores are frequently used as program registers, buffers and cache memory in most digital application and computing systems because of its compatible speed with processor and it is accessed at minimum once at every clock cycle. In memory hierarchy to connect bulk storage to the processor, SRAM are used as level cache. In recent developed VLSI system, processor speed is much higher than the available bulk storage speed. SRAM is the only available and CMOS compatible memory which is having seed compatible with processor but it takes large area to implement. Therefore memory hierarchy is used. SRAM is used as register memory inside the processor and upper level cache in memory hierarchy at microprocessor to speed up the system and to increase system performance. Due to large amount of storage cells in memories it can be found various solutions of address decoder designs leading to power consumption reduction and performance improvement. Usually different kind of precharging dynamic decoders are used. Design of dynamic decoder is complex and having more probability of wrong sensing SRAM IP cores are frequently used as program registers, buffers and cache memory in most digital application and computing systems because of its compatible speed with processor and it is accessed at minimum once at every clock cycle. In memory hierarchy to connect bulk storage to the processor, SRAM are used as level cache.

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Traditional static decoder gives more accurate result but it is having more number of transistors with large delay. Some solutions use hierarchical decoders with pre-decoding and also implemented binary tree decoder built by DE multiplexers. SRAM operation start with decoding of address, therefore row and column decoders is most important component in all random-access memories. SRAM performance is determined by the time taken to access data and power consumption. Row decoders takes an n-bit address data as input and gives 2^n outputs, one of them is having unique output which activates cell of SRAM. Small decoders are realize by single block by using 2-input and 3input logic gates but for large decoders hierarchy is used.

II. UNIVERSAL BLOCK DECODING SCHEME

As shown in Table 1, NAND gate gives unique logic low output when both of its input is high and it gives high output for other combination. Therefore we cannot make decoder by only using NAND gate. NOR gate gives unique logic high output when both of its input is low and it gives high output for other combination. Both these gate need inverter at output to make decoder and this increase number of transistor as well as delay in circuit. But their unique and different property can be used as combination and gives excellent result, because NAND gives output low but demands high all input and NOR gives output

high but demands low input.

Input Combination		Output For Different Gates			
A	B	AND	OR	NAND	NOR
0	0	0	0	1	1
0	1	0	1	1	0
1	0	0	1	1	0
1	1	1	1	0	0

Table 1 : Truth Table for Logic Gates

To design Decoder, Gate with unique output is required. As shown in Table 1,NOR Gate give unique high output for both low inputs and NAND gives unique low output for both high input. Based on this principle, universal design scheme is proposed to design decoder by using combination of NAND and NOR. For high logic output, the last stage of decoder is consist of NOR gates and previous to that with NAND gates, the alternate stages will continue up to input stage. Number of decoder inputs will decide the no. of stages of decoder and hence the first level i.e. either NAND or NOR gates. For even no. of input, the first stage is of NOR and for odd number of inputs it is of NAND for block architecture. Fig. 1 shows the architecture of this decoder. In this case 4:16 decoder has been taken as example.

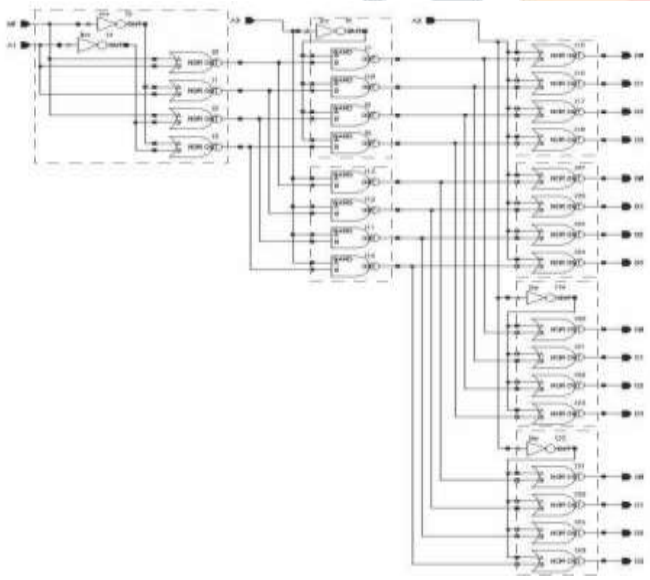

Fig 1: Schematic of a 4:16 Decoder, divided into blocks

Problem in block architecture decoder is that, it is not fully optimized in terms of transistor count, delay and power dissipation. Also due to different path lengths for different inputs, i.e. LSB need to travel every stage from input to output while MSB need to travel only last stage, that's why some address combination gives multiple outputs high due to path delay differences. As shown in fig. 2, when address is 00000, before line 0 at decoder output become high, line 15 became high for some duration. This is because different path delay in at output stage. Layout is shown in fig. 3.

This results in false selection of cell and extra power dissipation. Only single inverter is driving the stage of large gate so delay of decoder will increases for large input. Also as number of stages increase delay increases. To eliminate these problems new decoding scheme is proposed.

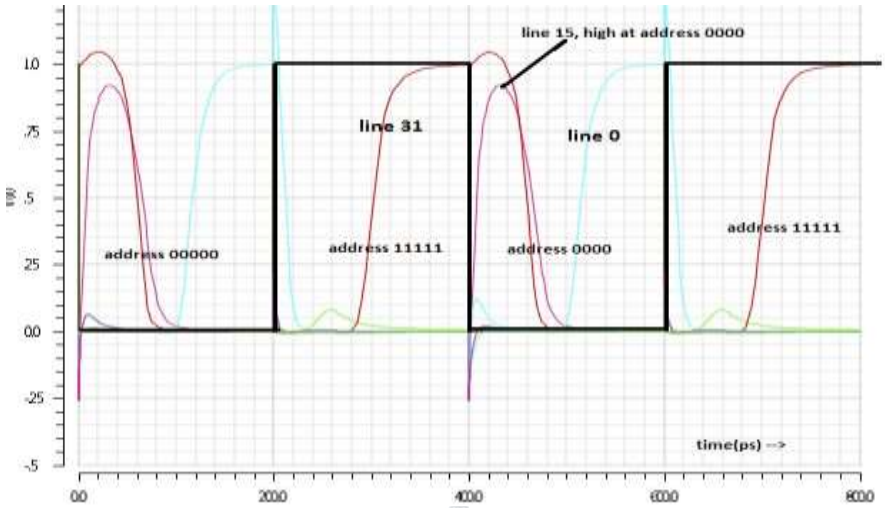

Fig 2 : Simulation Result of Universal decoder

Fig 3 : Layout of Universal Decoder

III. PROPOSED DECODING SCHEME

We have proposed a 5:32 decoder for SRAM (Fig. 4) using pre-decoder and inverter replica based circuit in addition to alternate NAND and NOR stage. In this architecture pre-decoder circuit reduces the gate count, also number of stages from input to output which results in reduction in delay and power consumption. By the application of predecoder circuit we can reduce number of stages, it can be performed at combination 4,8,16… input decoder structure. Here we have reduced one stage.

Fig. 4 shows the proposed 5:32 decoder, here NAND and NOR stages works to produce unique output. We have used predecoder circuitry to reduce the number of stages as compared to universal architecture, also reduced the count of transistors which makes proposed decoder faster and dissipates less power. Replica circuitry is used to overcome the problem of multiple selections due to variable path delay. It provides the same delay to MSB as that of LSB, and therefore the fixed delay circuit is formed for every logic combination change. First stage of this decoder is always predecoder, which can be made either NAND or NOR gates depends on number of input line. In this case first stage is NOR based architecture. NOR gate provides high unique high output when all its input is low. Next stage is NAND gate because it gives unique low output when all input combination is high. Again NAND output can be decoded by NOR stage and when input combination increases we can employ predecoder.

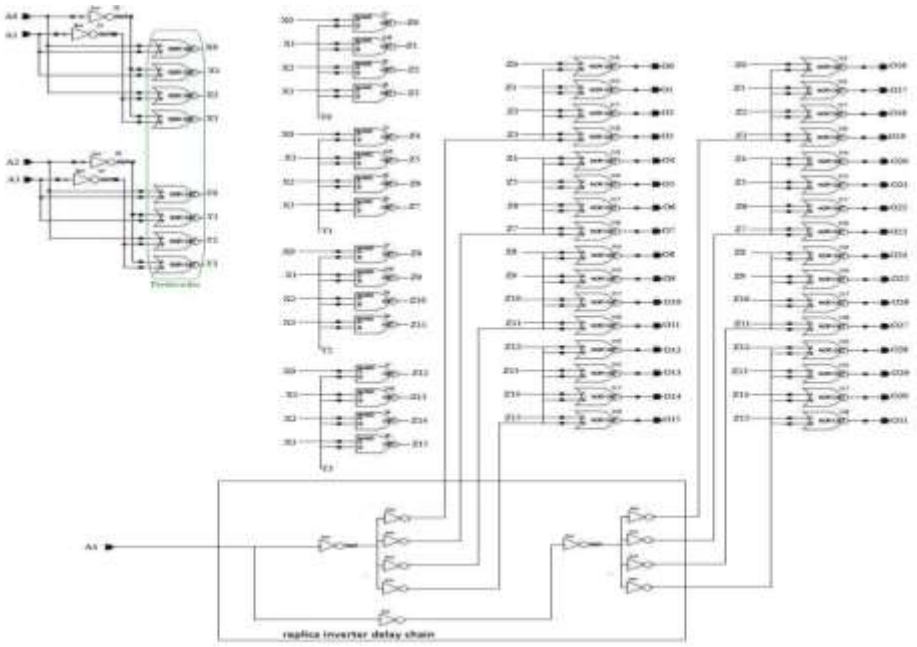

Fig 4 : Proposed 5:32 decoder using Predecoder and replica circuit

Based on this simple approach this type of decoder can be designed and it is basic principle of this designed technique. Third stage of this decoder needs inverter for decoding but simple inverter gives false decoder due to different path delay in different gate stage. So replica circuit overcomes the problem of multiple selections. CMOS inverter have optimal fan-out 4,so for driving 16x2 stage we need 8 inverter with 4 high and 4 low logic. Based on this approach replica chain is made and decoder is designed. Layout of proposed decoder is shown in fig. 5.

Simulation results shows that the transistor count, delay and power dissipation in proposed decoder is smallest in comparison with Traditional and Block architecture. Fig. 6 shows that, as the size of decoder increases, the performance of proposed decoder is improved over block and traditional decoder architectures.

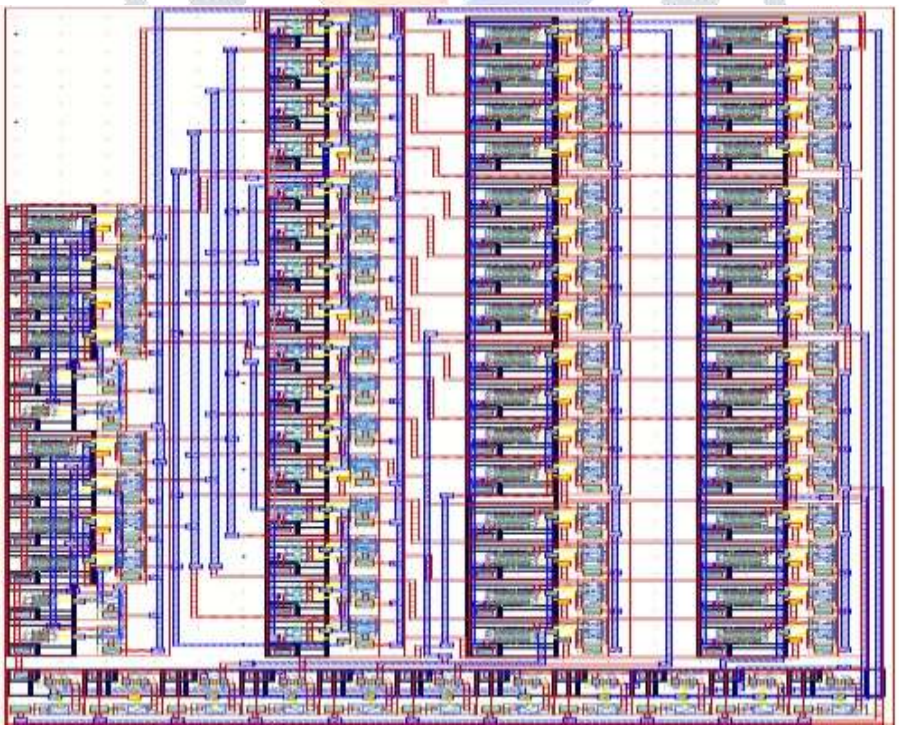

Fig 5 : Layout of proposed decoder

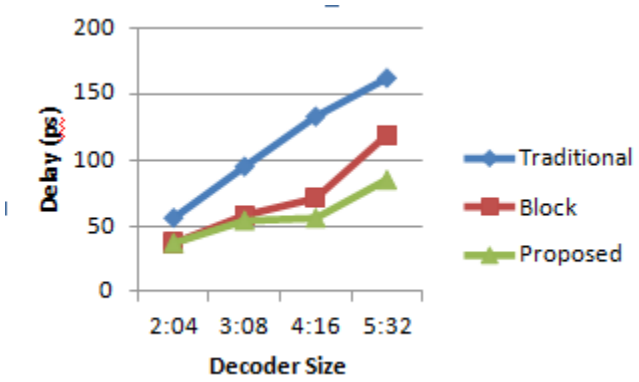

Fig 6 : Delay comparison of proposed architecture with traditional and Block architecture

IV. RESULTS AND COMPARSIONS

For 5:32 decoder, comparison between traditional, universal block and proposed architecture is shown in table 2. It shows the delay, number of transistors and power dissipation in proposed architecture is less than that of traditional and universal block architecture. Fig. 6 shows the proposed decoder is having better performance over traditional and block and it improves with the increase in size of decoder with respect to other. Fig. 07 shows the simulation of proposed decoder. Table 3 represents the results for corner analysis of proposed decoder where the largest delay is found out for SS case and it is 129.5ps whereas the smallest is for FF case and it is 116ps.

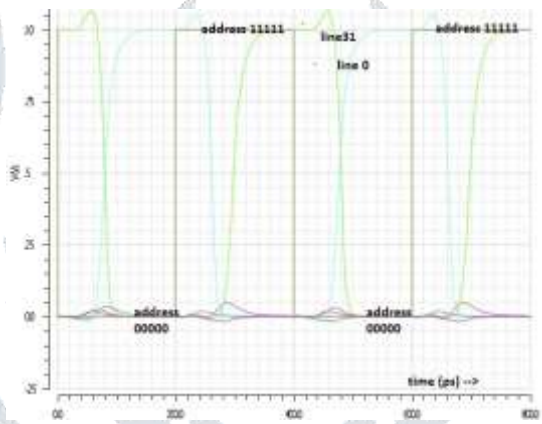

Fig 7 : Simulation result of the proposed 5:32 Decoder

	Traditional	Block	Proposed
Delay (ps)	162	119	98
No. of Transistors	370	250	250
Power (uW)	295	210	155

Table 2: Comparison between Traditional, Block and Proposed method

Conditions	Propagation Delay (ps)
TT	98
SS	129.5
FF	81.6
FS	97
SF	101

Table 3: Result of Corner Analysis

V. CONCLUSION

Decoder with NAND and NOR stages, pre-decoder and replica circuit is designed, it gives less power consumption and delay than that of traditional and block architecture. Delay and power dissipation in proposed decoder is 60.49% and 52.54% of traditional and 82.35% and 73.80% of universal block architecture respectively. High speed decoder is the important block for fast SRAM. Proposed decoder is used to implement a 1-kb 8-bit 1.25-GHz SRAM Memory.

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