IMPLEMENTATION OF LOW POWER MULTIPLIER USING APPROXIMATE 15-4 COMPRESSOR

[1]P.Agraja, [2]B.Sreekanth Reddy

[1]M.Tech student, [2]Asst. Professor

[1,2]Department of Electronics and Communication Engineering

[1,2]G.Narayanamma Institute of Technology and Science (for women), Hyderabad, Telangana

***Abstract:** This paper deals with the multiplier using approximate 15-4 compressor. The proposed multiplier has overcome the problems of power and delay. We propose a multiplier using accurate and approximate (four designs) a majority of 15-4 compressors and its performance is compared with a multiplier which uses accurate and approximate 3-2, 4-2 as well as 15-4 compressors. Some of the basic compressors like 3-2, 4-2 are used in the reduction stage of multiplier to reduce the power and increase the performance. Basically, small size compressors are used in small size multipliers but for large size multipliers it takes more time and consumes more power. To overcome this problem, we go for large size compressors like 15-4 for 16 bits or 32 bits. Approximate 15-4 compressor is proposed using four different designs. The basic building block for the 15-4 compressor is a 5-3 compressor.*

***Index Terms –** 3-2 compressor, 4-2 compressor, accurate and approximate 5-3 compressor, accurate and approximate 15-4 compressor, multiplier, low power multiplier.*

I. INTRODUCTION

Nowadays, Digital Signal Processing plays a vital role to handle the complexity of a digital signal. Mainly this type of processors takes care of convolution, correlation and filtering of digital signals and used to perform the complex operations like DFT (Discrete Fourier Transform) and FFT (Fast Fourier Transform). Adders, shifters and multipliers are used to accomplish these tasks. Among the three modules, the multiplier is complex to design. Multiplication is the complex operation which takes more time and consumes higher power than the other two operations (shifters, adders). So, designing the high-speed multipliers with low power is one of the challenging tasks. Multiplier has three stages they are first is to generate the partial products, second is to reduce the partial products and stage addition. Out of three stages reduction of partial products takes a lot of time and consumes more power than other two stages. Many techniques have been proposed to reduce the critical path in the multiplier. Using compressor in the partial products reduction stage is a popular technique for reducing the critical path. Compressors are the basic circuits which are made up of half adders and full adders which count the number of ones in the given input. There are several compressors which are required to reduce the partial products in the multiplier. Various compressors like 3-2, 4-2, 5-2, 5-3, 7-2 and so on exist, but these compressors are used only for small size of multipliers like 2 × 2, 4 × 4 and 8 × 8. Higher order compressors like 15-4 are used for higher order multipliers like 16 × 16, 32 × 32 in order to reduce the power and delay. High order compressors provide better performance in terms of power and speed but, it consumes more area than the low order compressors.

All these techniques perform the accurate computation and these modules produce the correct result with 100% accuracy in exact computing. Optimizing of all the parameters is not necessary in the exact computing for some of the applications. However, accurate computing is not essential for every application. Some of the applications like image processing and multimedia can tolerate limited errors and provide results. Approximate (inexact) computing techniques have become more popular because of its low complexity, less power consumption and faster operation. Error Distance (ED) and Error Rate (ER) are plays an important role in the approximate computing. Error distance is the arithmetic distance between an approximate output and actual output. Whereas error rate is given by a number of erroneous outputs over the total number of outputs.

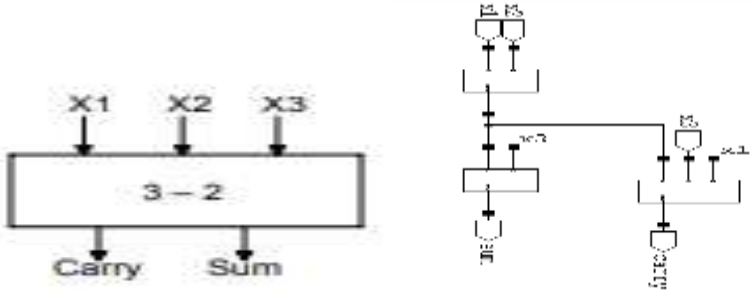
The paper is organized as follows. Compressors are explained in section II. Design of approximate 5-3 compressor is presented in section III. Design of 15-4 compressor using 5-3 compressor is elaborated in section IV. Multiplier designs using 15-4 compressor is described in the section V. Proposed multiplier is explained in section VI. Section VII describes simulation results. Finally, the conclusion is presented.

II. COMPRESSORS

A. 3-2 Compressor

Compressor 3-2 compresses three inputs to two outputs. This compressor is similar to a full adder which consists of two XOR gates and one MUX gate. It takes 3 inputs X_1, X_2, X_3 and generates two outputs i.e., a SUM bit and a CARRY bit. The critical path is from X_2 to SUM.

The basic equation of 3-2 compressor is $X_1 + X_2 + X_3 = SUM + 2*CARRY$



(a) (b)

Fig. 1: (a) 3-2 Compressor (b) Implementation of 3-2 Compressor

The equations of 3-2 compressor are

$SUM = X_1 \oplus X_2 \oplus X_3$

$CARRY = (X_1 \oplus X_2) \cdot X_3 + (\sim(X_1 \oplus X_2)) \cdot X_1$

B. 4-2 Compressor

The 4-2 compressor reduces four bits to two bits. In 4-2 compressor there are 4 inputs X_1, X_2, X_3, X_4 and 2 outputs Sum and Carry along with two more bits like carry-in (C_{in}) and a carry-out (C_{out})[8]. Including these two more bits 4-2 compressor has 5 input bits and 3 output bits. The input C_{in} bit is output from the previous lower significant compressor. The C_{out} is the output to the next significant compressor. The 4-2 compressor consists of two full adder modules using XOR and MUX gates. The critical path is from C_{in} to Sum.

The basic equation of 4-2 compressor is

$X_1 + X_2 + X_3 + X_4 + C_{in} = Sum + 2*(Carry + C_{out})$

$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{in}$

$C_{out} = (X_1 \oplus X_2) \cdot X_3 + (\sim(X_1 \oplus X_2)) \cdot X_1$

$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X_4) \cdot C_{in}\ (\sim (X_1 \oplus X_2 \oplus X_3 \oplus X_4)). X_4$

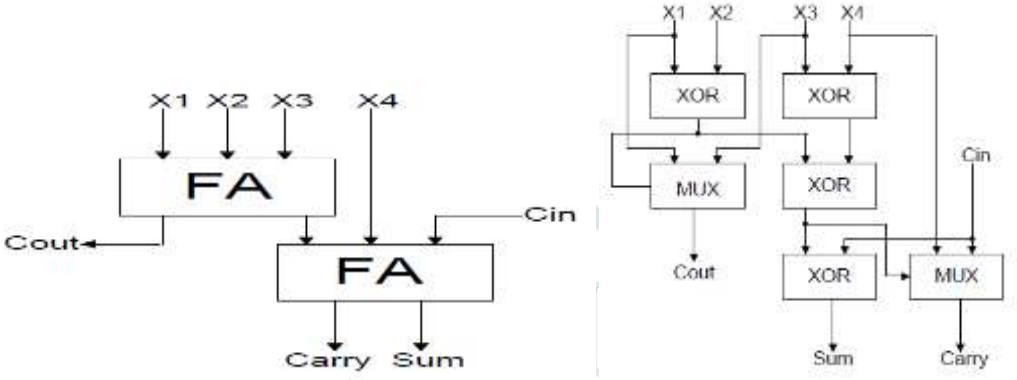


Fig.2: (a) 4-2 Compressor Implemented with Full Adders (b) Implementation of 4-2 Compressor.

III. 5-3 COMPRESSOR

5-3 compressor reduces 5 input bits into 3 output bits. Exact 5-3 compressor has more delay and consumes more power [9]. To reduce power and delay we are using approximate 5-3 compressor. In this approximate compressor totally, there are four designs. Approximate compressors give better results than accurate compressor.

A. Exact/Accurate Compressor

Compressor 5-3 is used to compress the five bits into three bits. It has five inputs X_0, X_1, X_2, X_3, X_4 and generates three outputs O_2, O_1, O_0[10]. This compressor consists of two full adders and one-half adder which has five XOR gates and two MUX's and one AND gate. This compressor has more delay and consumes more power. The critical path is between X_3 to O_2.

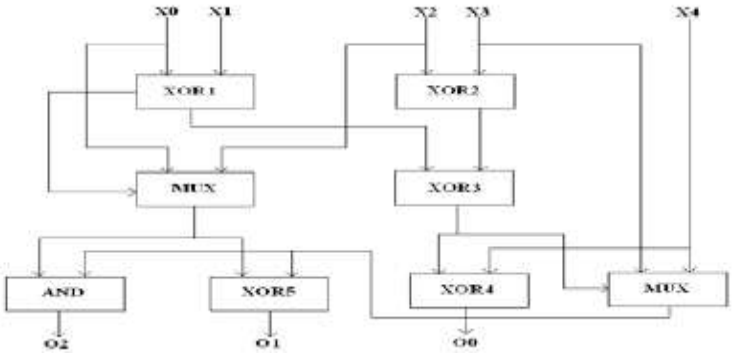


Fig. 3: Accurate 5-3 Compressor

Equations of accurate 5-3 compressor are,

$O_o = X_0 \oplus X_1 \oplus X_2 \oplus X_3 \oplus X_4$

$O_1 = (X_0 \cdot (\sim(X_0 \oplus X_1)) + X_2 \cdot (X_0 \oplus X_1) \oplus (X_3(\sim (X_0 \oplus X_1 \oplus X_2 \oplus X_3)) + (X_4 \cdot (X_0 \oplus X_1 \oplus X_2 \oplus X_3)$

$O_2 = (X_0 \cdot (\sim(X_0 \oplus X_1)) + X_2 \cdot (X_0 \oplus X_1) \cdot (X_3 (\sim (X_0 \oplus X_1 \oplus X_2 \oplus X_3)) + (X_4 \cdot (X_0 \oplus X_1 \oplus X_2 \oplus X_3).$

Table 1: Truth Table of 5-3 Compressor

Inputs X [4:0]	O_2	O_1	O_0
If all the inputs are 0	0	0	0
One of inputs is 1	0	0	1
Any two inputs are 1	0	1	0
Any three inputs are 1	0	1	1
One of inputs is 0	1	0	0
If all the inputs are 1	1	0	1

B. Approximate 5-3 compressor - Design 1

In design1, the output O_2 is approximated as O'_2 and remaining outputs remain same as accurate compressor (O_0, O_1). The approximated output matches with accurate output for 26 inputs out of 32 inputs because of this it does not gets 100% accuracy. The accuracy of design 1 is 81.25% but it gives better performance than accurate. The critical path is from X_3 to O_1.

Error distance is the arithmetic distance between the approximated output and accurate output. The weights of outputs O2, O1, O0 are 4, 2, 1 respectively. In this design the output O_2 is approximated as O'_2. The error distance is 4 or -4 for this design.

The approximated output O'_2 equation is given by,

$O'_2 = X_3 \cdot X_2$

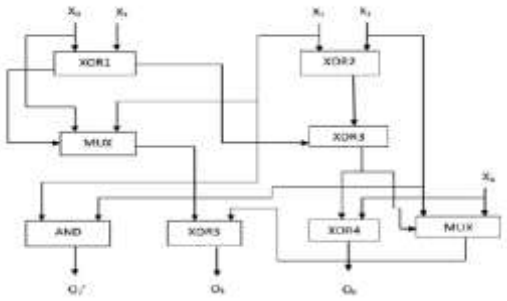


Fig. 4: Design 1 Approximate 5-3 Compressor

C. Approximate 5-3 compressor - Design 2

In this design, out of three outputs only two outputs are approximated they are O_2, O_1 and O_0 is same as the original expression of accurate compressor. The approximate output matches the accurate output for 24 inputs out of 32 inputs of this design. The critical path is between X_0 to O_0. The output differs in eight outputs because of this reason the accuracy of this design is 75%. By changing the outputs this design obtains minimum error distance. The error distance is 2 or -2.

The equations of approximated outputs are,

$O'_1 = X_4 \cdot [X_0 \cdot (\sim(X_0 \oplus X_1)) + (X_2 \cdot (X_0 \oplus X_1))]$

$O'_2 = X_4 \oplus [X_0 \cdot ((X_0 \oplus X_1)) + (X_2 \cdot (X_0 \oplus X_1))]$

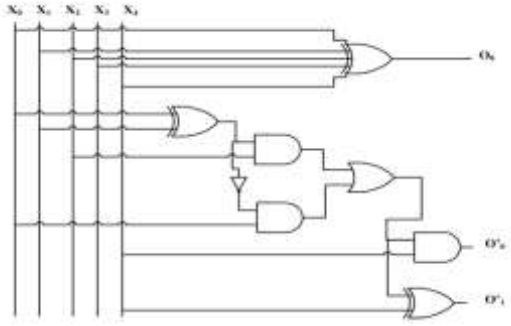


Fig. 5: Design 2 Approximate 5-3 Compressor

D. Approximate 5-3 compressor - Design 3

In the design shown in Fig. 6, except O_1 remaining outputs (O_2, O_0) are same as the accurate expression. Output O_1 is replaced by O'_1. Only eight outputs are different from accurate compressor. Accuracy of this design is 75%. The critical path is from X_4 to O_2. The minimum error distance is 2 or -2.

The equation of the approximated output O'_1 is

$O'_1 = X_4 \oplus [X_0 \cdot (\sim(X_0 \oplus X_1)) + (X_2 \cdot (X_0 \oplus X_1))]$

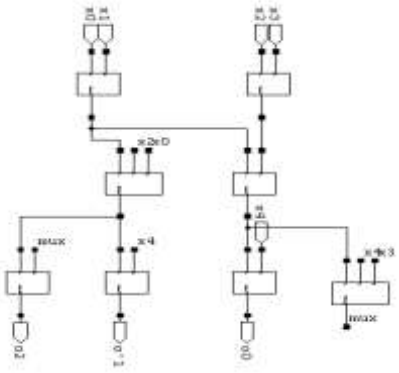


Fig. 6: Design 3 Approximate 5-3 Compressor

E. Approximate 5-3 compressor - Design 4

In this design, the remaining outputs (O_2, O_0) expressions are same as original expression except O_1. The output O_1 is replaced by O'_1. Only twelve outputs differ out of 32 outputs so, the accuracy of this design is 62.5%. The critical path is from X_4 to O_2. The minimum error distance is 2 or -2.

Expression for approximated output

$O'_1 = X_2 \oplus X_3$

Table 2: Error Distance for Accurate and Four Designs of Approximate 5-3 Compressor

X [4:0]	Error Distance of 5-3 compressor				
	Accurate 5-3	Design 1	Design 2	Design 3	Design 4
0	0	0	0	0	0
1	0	0	-2	2	0
2	0	0	0	-2	2
3	0	0	0	0	0
4	0	0	0	0	2
5	0	0	0	0	0
6	0	4	-2	-2	-2
7	0	4	0	0	-2
8	0	0	0	0	0
9	0	0	0	0	-2
10	0	0	-2	0	0
11	0	0	0	0	0
12	0	0	0	0	0
13	0	0	2	-2	0
14	0	4	0	0	-2
15	0	0	0	0	0
16	0	0	0	0	0
17	0	0	0	0	-2
18	0	0	-2	-2	0
19	0	0	0	0	0
20	0	0	0	0	0
21	0	0	-2	2	0
22	0	4	0	0	-2
23	0	0	0	0	0
24	0	0	0	0	-2
25	0	0	2	-2	-2
26	0	0	0	0	0
27	0	-4	0	0	2
28	0	0	0	0	0
29	0	-4	0	0	2
30	0	0	2	-2	0
31	0	0	0	0	0

IV. 15-4 COMPRESSOR

This compressor has 15 inputs ($X_0 - X_{15}$) and four outputs ($O_0 - O_3$). This will compress 15 inputs into four outputs. It has five full adders, two 5-3 compressors and one parallel adder. In the first stage, each full adder takes three inputs and produces two outputs a sum and a carry. All sum outputs are given to one of the 5-3 compressors and all carry outputs are given to the other 5-3 compressor. The outputs of 5-3 compressors are given to the parallel adder. In 4-bit parallel adder, inputs B_3 and A_0 are grounded. The parallel adder outputs are final outputs O [3:0].

By using accurate 5-3 compressor we proposed an accurate 15-4 compressor as shown in fig.8. Similarly, by using four designs of approximate 5-3 compressor we designed four designs of approximate 15-4 compressor. Full adders and parallel adder are kept as original adders in approximate 15-4 compressor. 5-3 compressors are used in first three designs of approximate 15-4 compressor which uses the design 1, 2 and 3 of approximate 5-3 compressors respectively. But in design 4 of approximate 15-4 compressor we use design 1 and design 4 of approximate 5-3 compressor. Design 1 approximated5-3 compressor is used to handle carry outputs because output carry has more weightage than sum. Moreover, pass rate of design 1 is greater than design 4. Design 4 approximate 5-3 compressor is used to handle sum signals.

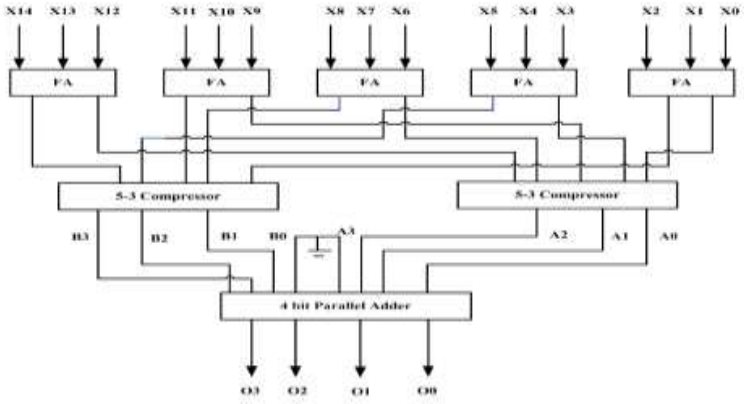


Fig. 7: Design of Accurate 15-4 Compressor.

V. MULTIPLIER DESIGN

Four approximate multipliers are designed using four approximate 15-4 compressors. An accurate multiplier is designed using approximate 15-4 compressor. Approximate multipliers using the approximate 15-4 compressors are compared with accurate multipliers using accurate 15-4 compressors. A 16×16 multiplier is designed using 15-4 compressor, 3-2 compressor, half adders and 4-2 compressors. In Fig.9 Where, each dot represents the partial product. Rectangular boxes indicate the use of 4-2 and 15-4 compressor in the multiplier.

Six 15-4 compressors are used to design one multiplier in the partial product reduction and finally four multipliers are designed. These compressors are used from 13th column onwards and add two zeros in that column to make use of the 15-4 compressor. Similarly, add one zero in the 14th column. In accurate multiplier, all accurate 15-4 compressors are used along with accurate 3-2 and 4-2 compressors. Approximate compressors are used in these six columns of multipliers. Design 1 of approximate 15-4 compressor is used in multiplier 1. Similarly, design 2, 3 and 4 of approximate 15-4 compressors are used in multiplier 2, 3 and 4 respectively.

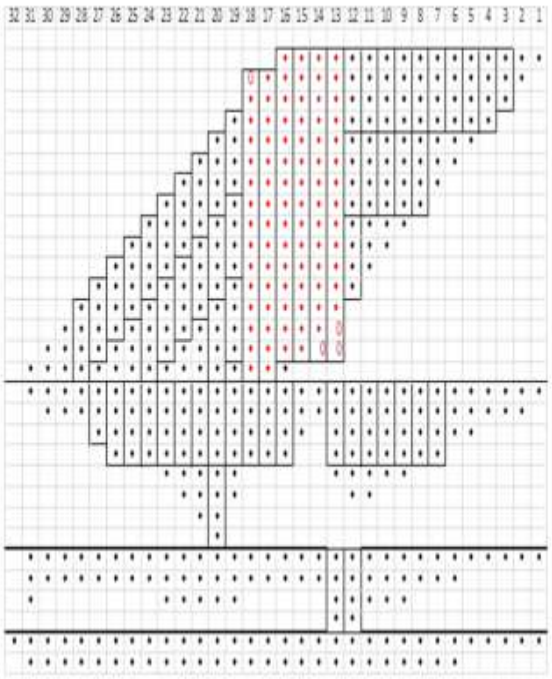


Fig. 8: A 16 × 16 Multiplier using 15-4 Compressor

VI. LOW POWER MULTIPLIER DESIGN

Compressor 15-4 is used in 16-bit multiplier with two 16-bit inputs a [15:0] and b [15:0] and produces 32-bit outputs z [31:0]. In multiplier, the reduction of partial products is done column-wise. For reduction of partial products 15-4 compressor is used which compress fifteen inputs to four outputs, full adders and half adders are also used which reduces two outputs i.e., sum and carry respectively. If any partial product is not involved in any adders those products are given to the next stage and carry is bypassed to next higher order column. At each stage, this process is continued until the last stage is reduced to two rows. In the first stage, all the AND gates are used to generate the partial products. In second stage, the compressor 3-2 is used for reducing the partial products. Finally, partial products are computed. The reduction stage consists of 15-4 compressor, 4-2 compressor, half adders and 3-2 compressor.

Instead of six approximate 15-4 compressors, we considered seventeen approximate 15-4 compressor which is from 8th column to 24th column in proposed multiplier. To make 15 inputs we add zeros for other remaining inputs where in 8th column there are only 8 inputs to make 15 inputs add zeros for remaining inputs and carry on for other columns. Along with 15-4 compressors in the multiplier other accurate compressors like 4-2, 3-2 and half adders are used in reduction of partial products stage. In accurate multiplier, all accurate 15-4 compressors are used along with accurate 3-2 and 4-2 compressors. Approximate compressors are used in these six columns of multipliers. Design 1 of

approximate 15-4 compressor is used in multiplier 1. Similarly, design 2, 3 and 4 of approximate 15-4 compressors are used in multiplier 2, 3 and 4 respectively.

VII. SIMULATION RESULTS

Xilinx ISE 13.3 is used to verify the functionality of the architecture. The tanner EDA is used to calculate the power, speed and delay. All designs are complied with 45nm technology and a typical library of tanner EDA is used to get the results.

Table 3: Result Analysis of Different 5-3 Compressors

Parameters	5-3 Compressor				
	Accurate	Design 1	Design 2	Design 3	Design 4
Delay (ηs)	255.50	255.29	255.20	255.36	255.28
Power(μW)	36.89	30.15	20.95	33.03	20.95
Pass rate (%)	100	81.25	75	75	62.5

From above table, accurate 5-3 compressor has large delay and consumes more power than other designs. Design 2 approximate 5-3 compressor consumes less power and delay than any other approximate compressors. Pass rate of accurate compressor is 100%. Pass rate of design 2 is less than other designs.

Table 4: Results of Various 15-4 Compressors

Parameters	15-4 compressor				
	Accurate	Design 1	Design 2	Design 3	Design 4
Delay (ps)	5.625	6.127	5.548	5.598	6.020
Power (nW)	0.396	0.381	0.315	0.374	0.224
Pass rate (%)	100	64.6	58.43	58.43	58.43

Table 4 gives the performance of 15-4 compressor and its pass rate. Design 4 gives better performance than any other designs because design 1 and design 4 are used in 5-3 compressor where design 1 has good pass rate than other designs.

Table 5: Comparison between 16 × 16 Multiplier and Proposed Multipliers

16 × 16 Multiplier using	16 × 16 Multiplier [9]		Low Power 16 × 16 multiplier	
	Delay(ps)	Power(nW)	Delay(ps)	Power(nW)
Accurate 15-4 Compressor	40.29	6.973	33.57	4.886
Design 1 of approximate 15-4 compressor	40.29	6.701	33.57	4.247
Design 2 of approximate 15-4 compressor	40.29	6.552	33.57	3.977
Design 3 of approximate 15-4 compressor	40.29	7.123	33.57	5.251
Design 4 of approximate 15-4 compressor	40.29	6.883	33.57	4.629

Table 5 shows the results of 16 × 16multiplier using different approximate 15-4 compressors. Multiplier designed using 15-4 compressor has area overhead because the total number of gates in 15-4 compressor is higher. Power improvement of proposed multiplier is less compared to existing multiplier. Delay of multipliers designed using different 15-4 compressors Is similar to the multiplier using accurate 15-4 compressor. Because 15-4 compressors are used only in reduction of partial products of the multiplier. Proposed multiplier gives better results than other existing multipliers because seventeen 15-4 compressors are used in the proposed multipliers.

VII. CONCLUSONS

This paper explains about the different compressors like 3-2, 4-2, accurate and approximate 5-3 compressor and four designs of approximate 15-4 compressor using 5-3 compressor as basic module. Approximate 16 × 16 multiplier is designed using 15-4 compressors. Approximate 16 × 16 multipliers provide better performance than accurate multipliers by compromising error rate. The proposed low power approximate 16 × 16 multiplier is also designed. Low power approximate 16 × 16 multiplier gives better performance than approximate 16 × 16 multiplier. Finally, our proposed multipliers consume low power and it is capable of giving good performance in case of error distance but, there is slight overhead of area as compared to other approximate multipliers.

REFERENCES

[1] Mateus Beck Fonseca, Jo Baptista S. Martins, Eduardo A. Cesar da Costa, "Design of power efficient butterflies from Radix-2 DIT FFT using adder compressors with a new XOR gate topology", Analog Integr Circ Sig process (2012) 73:945-954.
[2] Manohar Ayinala, Keshab k. Parhi, "Parallel pipelined FFT Architectures with Reduced Number of Delays", GLSVLSIS12, May 3-4, 2012.
[3] Y. Kim, Y. Zhang and P. Li, "An energy efficient approximate adder with carry skip for error resilient neuromorphic VLSI systems," in Proc. Int. Conf. Comput. – Aided Design (ICCAD), Nov. 2013, pp. 130-137.
[4] S. Veeramachaneni, K. M. Krishna, L. Anivash, S. R. Puppala and M. B. Srinivas, "Novel architectures for high-speed and low-power 3-2, 4-2, and 5-2 compressors", in Proc. Int. Conf. VLSI Design (VLSID), Jan. 2007, pp. 324-329.
[5] R. Menon and D. Radhakrishnan, "High Performances 5:2 compressor architectures", Proc. IEE-Circuits, Devices Syst., vol. 153, no. 5, pp. 447-452, Oct. 2006.
[6] A. Pishvaie, G. Jaberipur and A. Jhanian, "High performance CMOS (4:2) compressors," Int. J. Electron., vol. 101, no. 11, pp. 1511-1525.
[7] O. Kwon, K. Nowka, and E. Swartzlander, Jr.,"A 16-bit by 16-bit MAC design using fast 5:3 compressor cells," J.Vlsi Signal process. Syst. Signal, Image Video Technol., vol. 31, no. 2, pp. 77-89, Jul. 2002.
[8] Amir Momeni, Jie Han, Paolo Montuschi and Fabrizio Lombardi, "Design and analysis of Approximate Compressors for Multiplication," IEEE Transactions on Computers, vol. 64, no. 4, April 2015, pp. 984-994.
[9] R. Marimuthu, Y. Elsie Rezinold, and P. S. Mallick, "Design and Analysis of Multiplier Using Approximate 15-4 Compressor", IEEE Trans., vol. 5, 2017, pp. 1027-1036.
[10] R. Marimuthu, M. Pradeepkumar, D. Bansal, S. Balamurugan and P. S. Mallick, "Design of high speed and low power 15-4 compressor," in Proc. Int. Conf. Commun. Signal process. (ICCSP). Apr.2013. pp.533-536.