Grid Voltage and Current Harmonics Reduction usingFuzzy logic control of Dual interfacing converter

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Abstract

In this project the compensation of neighborhood load harmonic current utilizing a single DG interfacing converter may make the intensification of supply voltage harmonics delicate burdens, especially when the fundamental grid voltage is very mutilated. Dissimilar to the op generation tion of unified power quality conditioners (UPQC) with arrangement converter, another harmonic current supply voltage and grid current harmonic pay methodology is proposed utilizing facilitated control of two shunt interfacing converters. In particular, the primary converter is in charge of neighborhood load supply voltage harmonicsuppression. The second converter is utilized to alleviate the harmonic current created by the communication between the primary interfacing converter and the nearby nonlinear load. To understand a basic control of parallel converters, an altered mixture voltage and current controller is additionally created in the paper. By utilizing this proposed controller, the grid voltage stage bolted circle and the identification of the heap current and the supply voltage harmonics are pointless for both interfacing converters. In this way, the computational heap of interfacing converters can be fundamentally lessened.

I. Introduction

There are developing requests of utilizing power molding circuits in low and medium voltage control circulation system. Contrasting with massive detached filters that are very touchy to circuit parameters varieties, the dynamic power molding hardware including dynamic power filter (APF), dynamic voltage restorer (DVR), and unified power quality conditioner (UPQC) is favored due the quick element reaction and the great resistance to system parameter changes. Then again, the high entrance of distributed generation (DG) unit with power devices interfacing converter offers the likelihood of power appropriation systemharmonic current compensation utilizing multi-utilitarian DG interfacing converter.

Past research predominantly centered around the control of a single DG shunt interfacing converter as an APF, as their energy devices circuits have comparative topology. To understand an upgraded dynamic separating objective, the ordinary current control techniques for grid tied DG interfacing converter might be adjusted. To start with, the wide data transfer capacity current controllers are utilized so that the frequencies of harmonic load current can fall into the transmission capacity of the present controller. On the other hand, the particular frequencyharmonic pay utilizing multi-resounding current controller has gotten a consider generation measure of constrictions, as detailed. In the killjoy controller is created for different DG units with dynamic harmonic separating capacity. In the neural system strategy is utilized to enhance the harmonic separating execution of DG interfacing converters that are associated with a grid with substantial variety of grid impedance. Notwithstanding the pay of harmonics at low voltage dissemination arranges, the dynamic separating of music in higher voltage circulation system utilizing multi-level converters. Nonetheless, it is critical to note that previously mentioned compensation strategies are primarily utilized as a part of grid tied converter systems. In late writing, the hybrid voltage and current control is likewise created to understand a fundamental voltage control for DG control direction and a harmonic current control for nearby load harmoniccompensation. Contrasted with the previously mentioned customary current control strategies, the crossover controller permits an interfacing converter to repay music in both network tied and islanding micro grids with help of the low transmission capacity interchanges between DG units, it likewise harmonic extraction to accomplish harmonic power sharing among parallel DG systems.

II. Review of Conventional APF and DVR

This area quickly audits the control of shunt APFs for network current harmonic alleviation and arrangement DVRs for supply voltage harmonic suppression. To contrast and the proposed parallel-converter utilizing adjusted half and half voltage and current controller as appeared in the following segment, the surely knew double-loop current control and voltage control are connected to APFs and DVRs, individually.

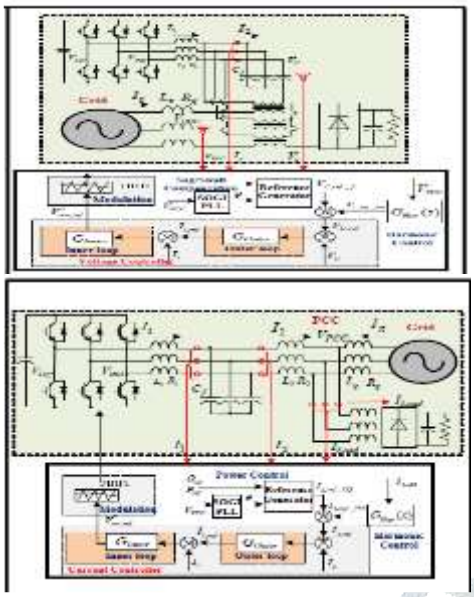


Fig.1. Diagram of local harmonic compensation using interfacing converter

A. Shunt Interfacing Converters for Grid Current Harmonic Mitigation

Fig. 1(a) demonstrates the topology and control system of an interfacing converter for compensating generation ting harmonic current from a neighborhood nonlinear load. To start with, the neighborhood load is associated with the output of the interfacing converter, and afterward, they are coupled to the primary network through the grid feeder. The parameters of the interfacing converter LCL filter and the network feeder are recorded as $z1(s) = sL1 + R1$, $z2(s) = sL2 + R2$, $z3(s) = 1/(sCf)$, and $zg(s) = sLg + Rg$, where $L1$, $L2$, $R1$, and $R2$ are the inductance and resistance of the filter arrangement stifles, Cf is the capacitance of the shunt capacitor, and Lg and Rg are grid inductance and resistance.

The present control plan is appeared in the lower some portion of Fig. 1(a). As per the customary APF control hypothesis, the neighborhood stack current is measured and the harmonic segments are distinguished as:

$$I_{2,ref\_h} = H_{Har}(s) \cdot I_{Load} \quad (1)$$

Where $HHar(s)$ is the exchange capacity of the harmonic segment indicator and $ILoad$ is the nearby load current.

At the point when both the key and the harmonic parts are resolved, the reference current is acquired as $I2, = I2,\_f + I2,ref\_h$ and it is utilized as the contribution for a double-loop line current $I2$ control.

$$I_{1,ref} = H_{Outer}(s) \cdot (I_{2,ref} - I_2) \quad (2)$$

$$V^*_{out,ref} = H_{Inner}(s) \cdot (I_{1,ref} - I_1) \quad (3)$$

Where $HOuter(s)$ and $HInner(s)$ are the controllers of the external and the internal control loops, separately. $I1$, and $I1$ are the reference and the quick inverter output current, separately. $Vout, *$ is the output voltage reference of the inverter.

B. Series Interfacing Converters for Supply Voltage Harmonic Mitigation

It is important generation to note that notwithstanding when the harmonic current of shunt nonlinear burdens is adjusted, the supply voltage to neighborhood load is not gen generation simply sinusoidal. This can be brought on by a couple reasons including the fundamental system voltage consistent state harmonic bends. Assume the system current Ig in Fig. 1(a) is without swell, the harmonic voltage drop on the grid feeder $Rg$and Lg is zero. For this situation, the harmonic voltage at PCC is the same as the harmonics from the principle network. To address the previously mentioned issue, an arrangement DVR can be introduced as appeared in Fig. 1(b), where the system is combined with the power distribution arrange utilizing an arrangement associated coordinating transformer. The auxiliary of the transformer is associated with a converter with output LC filter.

To begin with, the PCC voltage is measured by the DVR controller and the central and harmonic PCC voltage segments are isolated. At that point, the supply voltage harmonic parts are repaid by setting up the harmonic voltage reference of the DVR as $Vref\_h = VPCC\_h$ [35] and the basic voltage reference $Vref\_f$ of the DVR is resolved by the droop and swell compensation necessity of the system [3].

At the point when the central and harmonic part references are resolved, the DVR reference voltage is gotten as $VC, = VC,\_f + VC,ref\_h$. A while later, a double-loop voltage control is connected to guarantee a quick voltage following as

$$I_{1,ref} = H_{Outer}(s) \cdot (V_{C,ref} - V_C) \quad (4)$$

$$V^*_{out,ref} = H_{Inner}(s) \cdot (I_{1,ref} - I_1) \quad (5)$$

Where $HOuter$ (s) and $HInner$ (s) are the controller of the external and the inward control loops, separately. , and VC are the reference and the immediate estimation of DVR voltage, separately.

III. THE PROPOSED COORDINATED CONTROL METHOD

To have harmonic current alleviation of the supply voltage and the grid current harmonics, a compensation technique utilizing facilitated control of two parallel interfacing converters is proposed in this segment. The hardware and control outlines of the proposed system are appeared in Fig. 2 and Fig. 3, individually. Initial, a DG unit with two parallel interfacing converters having a similar DC rail is associated with PCC. Each interfacing converter has a output LCL filter and the nearby nonlinear load is put at the outputfilter capacitor of converter1. In this topology, the supply voltage to neighborhood nonlinear load is upgraded by controlling the harmonic part of interfacing converter1. In the interim, the network current harmonic is relieved by means of the power molding through interfacing converter2. Their definite control systems are talked about separately, as demonstrated as follows:

A. Control Strategy for Converter

To start with, the line current $I2,1$ of converter1 and the PCC voltage $VPCC$ as appeared in Fig. 2 are measured to compute the genuine and receptive outputpower of this converter.

$$\begin{cases} P_{C1} = \dfrac{3\tau}{2(s+\tau)}\left(V_{PCC,\alpha}\cdot I_{2\alpha,C1} + V_{PCC,\beta}\cdot I_{2\beta,C1}\right) \\ Q_{C1} = \dfrac{3\tau}{2(s+\tau)}\left(V_{PCC,\beta}\cdot I_{2\alpha,C1} - V_{PCC,\alpha}\cdot I_{2\beta,C1}\right) \end{cases} \quad (6)$$

where $PC1$ and $QC1$ are the output genuine and receptive power of converter1, $VPCC,\alpha$ and $VPCC,\beta$ are the PCC voltage in the two-hub stationary reference outline, and $I2\alpha,C1$ and $I2\beta,C1$ are the line current of converter1, and is the time τconstant of low pass filters. The time steady of the low pass filter is for the most part controlled by two components. To begin with, the genuine and receptive power swells brought on by line current music must be appropriately sifted through. Besides, the quick element control should be kept up. As per the outline rule.

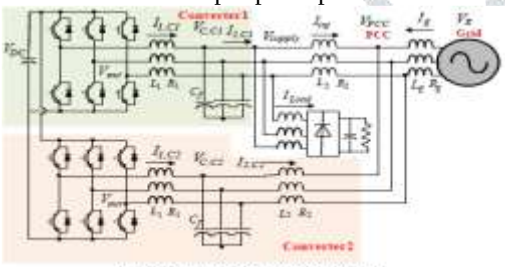


Fig. 2. Diagram of the proposed topology.

Fig2: diagram of proposed topology

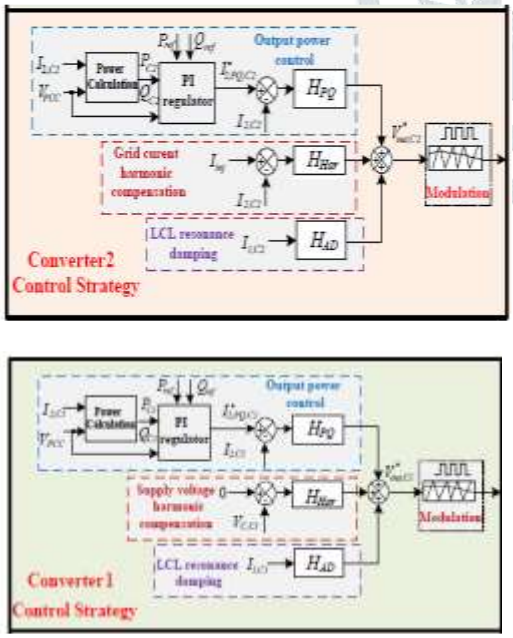


Fig.3. Diagram of the proposed interfacing converter control strategies

Note that the power reference is gen generation decided by the accessible power from the back phase of the DG unit. At the point when there is vitality stockpiling system in the DG unit, the power reference can likewise be controlled by the vitality administration arrangement of a DG unit or a micro grid. Along these lines, for straightforwardness, the harmonic pay administration is typically initiated when there is adequate power rating in the interfacing converters.

The output of the power reference gen generation tor is the line current reference $I2,,,1$

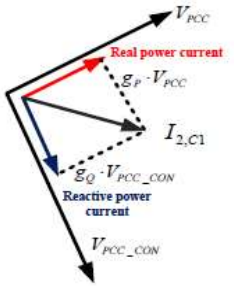


Fig. 4. Phasor diagram of converter1 line current.

$$I^{*}_{2,PQ,C1} = g_P\cdot(V_{PCC,\alpha} + jV_{PCC,\beta}) + g_Q\cdot(V_{PCC,\beta} - jV_{PCC,\alpha}) \quad (7)$$

Where gp and gQ are two customizable additions that can control converter1 output genuine and receptive power, separately. This controller just uses a duplicate of the momentary PCC voltage vector ($,\alpha + jVPCC,\beta$) and the conjugated part as the present reference. This depends on a reality that the genuine output power is in extent to the line current $I2$ that outsiders to immediate PCC voltage vector, while the receptive power is corresponding to the line current that outsiders to the conjugated PCC vector$VPCC,\beta - jVPCC,\alpha$, as appeared in Fig. 4.

The additions gp and gQ in are controlled by two PI controllers as

$$\begin{cases} g_P = (k_{p\_PQ} + \dfrac{k_{i\_PQ}}{s})\cdot(P_{ref} - P_{C1}) \\ g_q = (k_{p\_PQ} + \dfrac{k_{i\_PQ}}{s})\cdot(Q_{ref} - Q_{C1}) \end{cases} \quad (8)$$

Where kp_PQ and ki_PQ are PI controller coefficients. $Pref$ and $Qref$ are the reference genuine and receptive power, individually.

Customarily, the half and half controller in controls the DG key voltage for power control and the harmonic current for load harmonic current relief. As this converter is in charge of repaying harmonic parts of the supply voltage, the controllers in the half breed voltage and current controller is changed with harmonic supply voltage control and central

line current control as:

$$V^*_{out,C1} = \underbrace{H_{PQ}(s)\cdot(I^*_{2,PQ,C1} - I_{2,C1})}_{\text{Power Control}} + \underbrace{H_{Har}(s)\cdot(V^*_{C,C1} - V_{C,C1})}_{\text{Voltage Harmonic Mitigation}} + \underbrace{H_{AD}(s)\cdot I_{1,C1}}_{\text{Active Damping}} \quad (9)$$

where $Vout,C1*$ is reference voltage for PWM preparing, $I2,PQ,C1*$ is the line current reference of the Power Control term, $VC,C1*$ is the reference voltage of the Voltage Harmonic Mitigation term, $VC,C1$ is the filter capacitor voltage, and $I1,C1$ is the converter1 output current. As appeared in Fig. 2, the filter capacitor voltage ($VC,1$) is the same as the heap voltage ($Vsupply$). The controllers of the Power Control, Voltage Harmonic Mitigation and Active Damping terms are recorded as

$$H_{PQ}(s) = k_{p1,C1} + \frac{2\kappa_{i,f,C1}\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \quad (10)$$

$$H_{Har}(s) = k_{p2,C1} + \sum_{h=5,7,11,13} \frac{2k_{v,h,C1}\omega_c s}{s^2 + 2\omega_c s + (h\cdot\omega_o)^2} \quad (11)$$

$$H_{AD}(s) = k_{AD,C1} \quad (12)$$

where $kp1,C1$ is the relative pick up and $ki,f,C1$ is the thunderous controller pick up for the power control controller HPQ (s), $kp2,C1$ is the corresponding addition and $kv,h,C1$ is the full controller pick up for the voltage harmonic relief controller $HHar(s)$, and $kAD,C1$ is the relative control that can effectively stifle the LCL filter reverb generation .

It is important to note that lone the essential relative additions $kp1,1$ and $kp2,C1$ is much lower than the full controller pick up $kv,h,C1$. Accordingly, the output of the Power Control term in (9) has low harmonic part. Because of this element, the contorted network voltage can be straightforwardly utilized as the contribution of (7), as its harmonic part can be naturally sifted through by (10). In the meantime, it can be seen that the output of the second Voltage Harmonic Mitigation term just has low major parts, as just resounding controllers at the chose harmonic frequencies are received in the control term. Accordingly, the Power Control term and Voltage Harmonic Mitigation term are exceptionally all around decoupled. As needs be, an interfacing converter can dispatch energy to the system and repay supply voltage music in the meantime. Furthermore, dissimilar to the routine DVR with PCC harmonic voltage extractions, the Voltage Harmonic Mitigation term can understand dynamic supply voltage harmonicscompensation with no harmonic extractions. What's more, it can be seen that a shut circle control is acknowledged without utilizing stage bolted loops.

At last, it is important to accentuation that contrasting with the customary half breed controller that uses the hang control to acknowledge mod generation mod generation power control flow, the principal current control in (9) could successfully enhance the power control dynamic reaction.

A. Control Strategy for Converter2

The control procedure of converter2 is like that of converter1, as additionally exhibited in Fig. 3. Be that as it may, both the fundamental and the harmonic converter streams are controlled. In the first place, the controllers as appeared in (6) to (8) are embraced to get the power control term reference $I2\alpha,1$ and $I2\beta,C1$ are the line current of converter1, and τ for converter2. Subsequently, another mixture controller is utilized to understand the shut circle line current control of conveter2 as:

$$V^*_{out,C2} = \underbrace{H_{PQ}(s)\cdot(I^*_{2,PQ,C2} - I_{2,C2})}_{\text{Power Control}} + \underbrace{H_{Har}(s)\cdot(I^*_{2,Har,C2} - I_{2,C2})}_{\text{Current Harmonic Mitigation}} + \underbrace{H_{AD}(s)\cdot I_{1,C2}}_{\text{Active Damping}} \quad (13)$$

where $Vout,C2*$ is reference voltage for converter2 PWM handling, $I2,PQ,C2*$ is the present reference for converter2 control, $I2,Har,C2*$ is the present reference for converter2 line current harmonic control, $I1,C2$ is the converter2 output current. The controllers of Power Control, Current Harmonic Mitigation and Active Damping terms are recorded here as

$$H_{PQ}(s) = k_{p1,C2} + \frac{2k_{i,f,C2}\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \quad (14)$$

$$H_{Har}(s) = k_{p2,C2} + \sum_{h=5,7,11,13} \frac{2k_{i,h,C2}\omega_c s}{s^2 + 2\omega_c s + (h\cdot\omega_o)^2} \quad (15)$$

$$H_{AD}(s) = k_{AD,C2} \quad (16)$$

. Similar to converter1, the Power Control term and the Current Harmonic Mitigation term are exceptionally very much decoupled. In this manner, PLLs is a bit much and the contribution of Power Control term $I2,,2*$ can have a few bends when utilizing an immediate duplicate of PCC voltage. Moreover, take note of that the distinction between the converter1 line current and the heap current $Iinj$ (found in Fig. 2, equivalents to $I2,1 - ILoad$) is received as the contribution of Current Harmonic Mitigation term of converter2 as $I2,Har,C2* = Iinj$. As just harmonic full controllers are utilized as a part of the Current Harmonic Mitigation term and the corresponding increase $kp2,2$ is much littler than $ki,h,C2$ in (15), converter2 can effectively compensating generation the harmonic current from converter1 with no harmonic current recognition. For this situation, the infused current Ig to the primary network is harmonic free.

In rundown, the proposed topology and the altered cross breed controller can understand an upgraded nature of supply voltage to the neighborhood stack and the grid current to the primary system in the meantime. Through the organized control of two parallel converters, the previously mentioned control quality change target is acknowledged in a computationally compelling way, without including any PLLs and harmonic voltage/current extractions in the whole procedure. What's more, when the principal current direction in the Power Control term in (13) and (9) is supplanted by the surely knew hang control for major voltage control, the proposed technique can be utilized as a part of an islanded micro grid in a comparative way.

C. Frequency Domain Analysis

As both converter1 and converter2 have frequency specific element at the major and they chose harmonic frequencies, the supply voltage harmonic and system current

harmoniccompensation execution can be analyzed by frequency area investigation utilizing Bode plots. Initial, a LCL filter of a converter is appeared in Fig. 5, where the neighborhood load is disentangled as a harmonic current source associated with the shunt capacitor of converter LCL filter. The reaction of the filter plant is given as

$$\left(\frac{V_{out}}{z_1}+\frac{V_{PCC}}{z_2}-I_{Load}\right)\cdot\left(\frac{1}{z_1}+\frac{1}{z_2}+\frac{1}{z_c}\right)=V_C \quad (17)$$

$$V_{out}-V_C=z_1\cdot I_1 \quad (18)$$

$$V_C-V_{PCC}=z_2\cdot I_2 \quad (19)$$

In light of the control methodologies in (9) and (13), the exchange capacity of the LCL filter circuit (see (17) to (19)) for both converter1 and converter2, and expecting that $Vout,C2* = Vout,C2$ and $Vout,C1* = Vout,C1$, the shut circle current and voltage reaction of parallel converters can

$$V_{C,C1}=R_{11}(s)V^*_{C,C1}+R_{12}(s)I^*_{2,PQ,C1}-R_{13}(s)I_{2,C1} \quad (20)$$

$$I_{2,C1}=R_{21}(s)V^*_{C,C1}+R_{22}(s)I^*_{2,PQ,C1}+R_{13}(s)V_{PCC} \quad (21)$$

$$I_{2,C2}=R_{31}(s)I^*_{2,PQ,C2}+R_{32}(s)I^*_{2,Har,C2}-R_{33}(s)V_{PCC} \quad (22)$$

be set up as

Where the coefficients $R11(s)$ to $R33(s)$ in portray the reaction of these two converters to different excitations of the system. In particular, (20) predominantly centers the execution of converter1 at harmonic frequencies, while expects to depict the execution of the system at around basic frequency. As it were, converter1 has voltage source trademark at harmonic frequencies however current source trademark at around the essential frequency. Then again, as both essential and harmonic line current are controlled for converter2, just a single current source proportional circuit in can be utilized to show the execution of converter2. With a specific end goal to make the examination more direct, a mind boggling circuit arrange as appeared in Fig. 6 is produced to show how the harmonic voltage and current harmonic are at the same time adjusted. Take note of that this identical circuit arrange in Fig. 6 is just viable at the chosen harmonic frequencies.

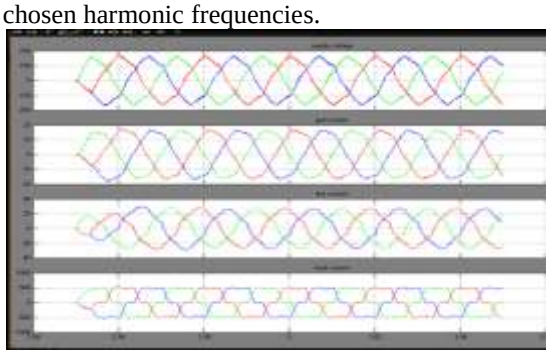


Fig.5. only the local load harmonic current is compensated. (From upper to lower: $Vsupply$, Ig, $I2$, $ILoad$)

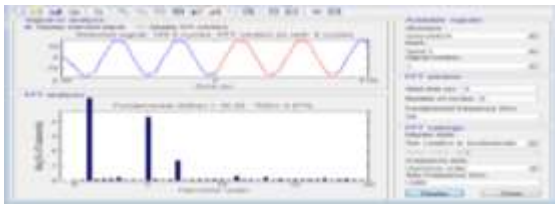


Fig.6. The harmonic spectrum of grid current Ig

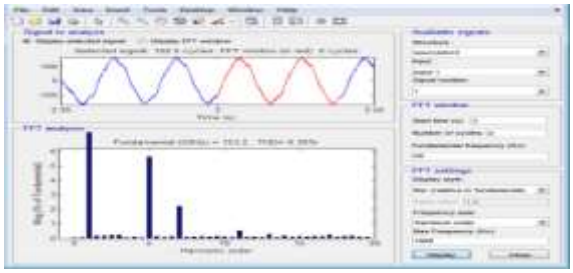


Fig.7. the harmonic spectrum of supply voltage $Vsupply$

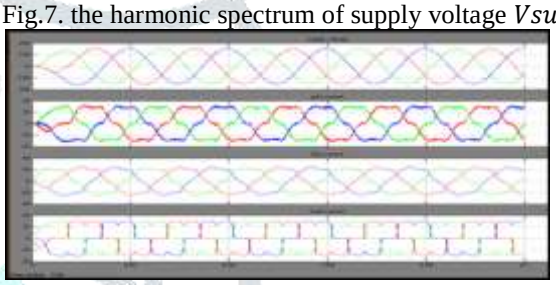


Fig.8. only the supply voltage harmonic component is compensated. (From upper to lower: $Vsupply$, Ig, $I2$, $ILoad$)

Fig.9. The harmonic spectrum of grid current Ig

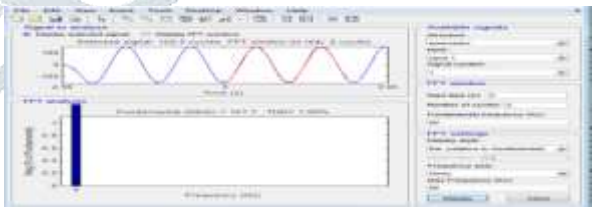


Fig.10. The harmonic spectrum of supply voltage $Vsupply$

Fig:11 Grid Voltage

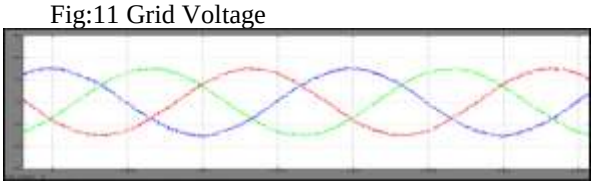


Fig:12 Grid Current

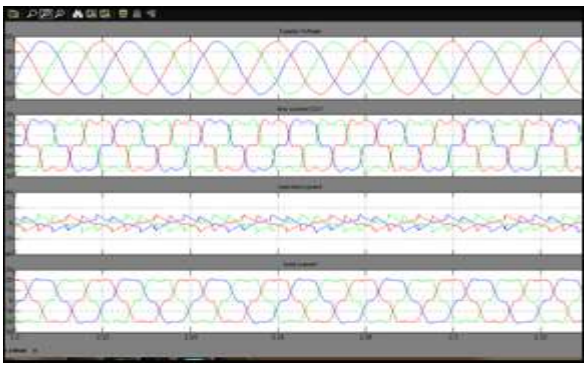


Fig.13. Performance of converter1. (From upper to lower: $Vsupply$, $I2,1$, $Iinj$, $ILoad$)

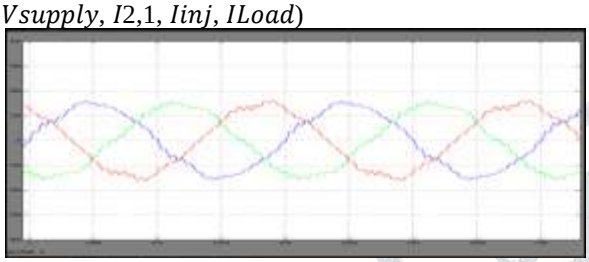


Fig14: Filter Capacitor Voltage

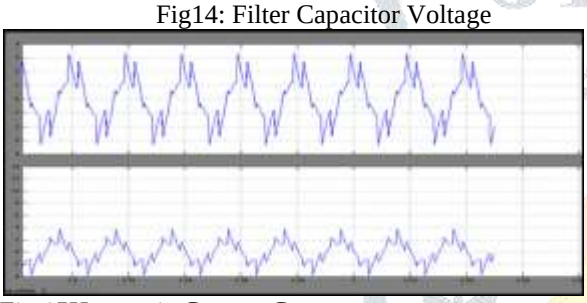


Fig:15Harmonic Current Component

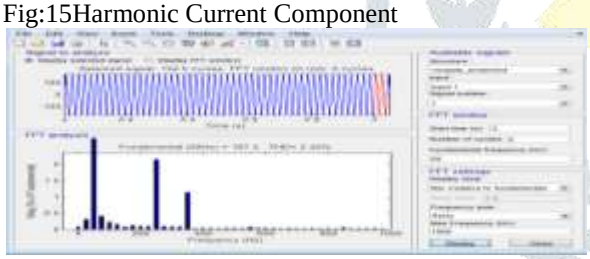
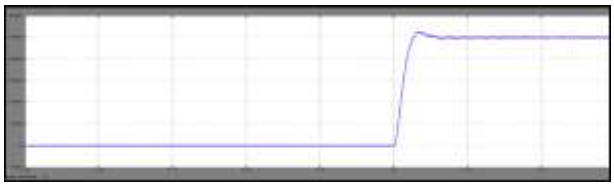


Fig.16. The harmonic spectrum of supply voltage $Vsupply$

Fig.17. The harmonic spectrum of grid current Ig



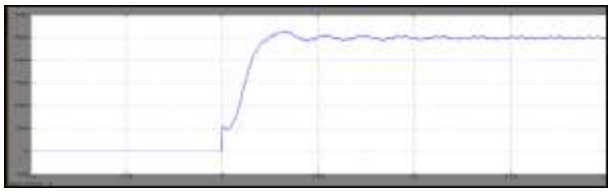


Fig. 18. Real and reactive power of converter1and converter2

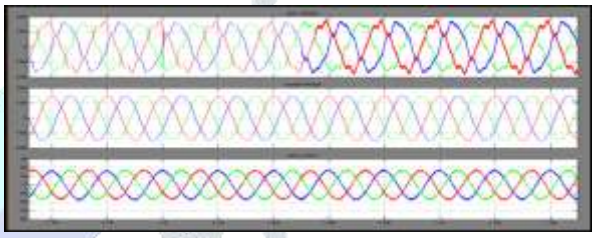
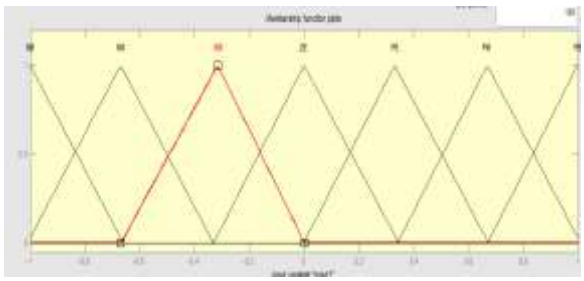


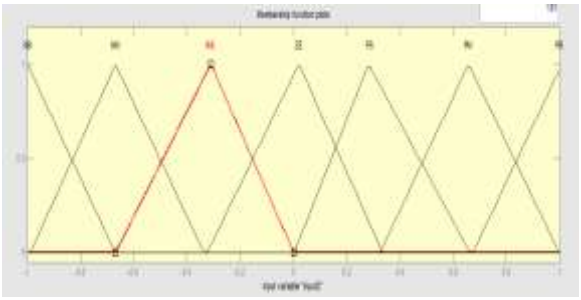
Fig. 19. The performance of the dual-converter system during 10% grid voltage sags, with 10.03% THD

Simulation results by using fuzzy controller:

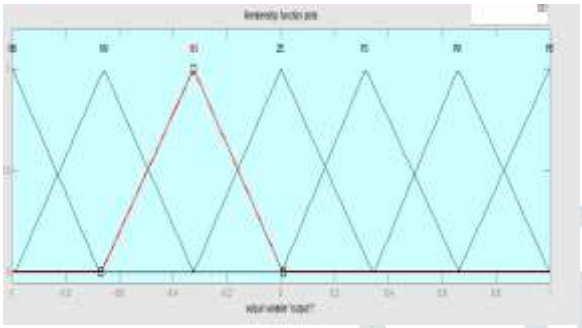
Fuzzy rule is a sort of many-regarded justification in which reality estimations of elements may be any bona fide number some place in the scope of 0 and 1. By separate, in Boolean method of reasoning, reality estimations of components may simply be 0 or 1. Fluffy basis has been contacted manage the possibility of partial truth, where reality regard may go between absolutely apparent and completely false. Moreover, when semantic factors are utilized, these degrees might be overseen by particular capacities.



Membership function for error in current



Membership function for change in error current



Membership function for voltage

The three variables of the FLC, the error, the change in error and the output, have SEVEN triangle membership functions for each. The basic fuzzy sets of membership functions for the variables are as shown in the Figs.8. The fuzzy factors are communicated by semantic factors „positive enormous (PB)", ", „positive little (PS)", „zero (Z)", „negative little (NS)",", „negative huge (NB)", for every one of the three factors. A lead in the govern base can be communicated in the shape: If (e is NB) and (de is NB), at that point (album is Z). The tenets are set in view of the information of the framework and the working of the framework. The administer base alters the obligation cycle for the PWM of the inverter as per the adjustments in the contribution of the FLC. The quantity of principles can be set as wanted. The quantities of guidelines are 49 for the five enrollment elements of the blunder and the adjustment in mistake (contributions of the FLC).

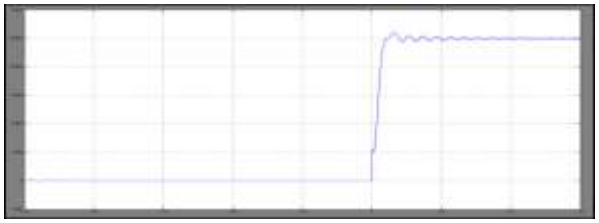
Table. 1. Fuzzy table

INPUT/ OUPUT	NB	NM	NS	ZE	PS	PM	PB
NB	PB	PB	PB	PB	PM	PS	ZE
NM	PB	PB	PM	PM	PS	ZE	NS
NS	PB	PM	PS	PS	ZE	NS	NM
ZE	PM	PM	PS	ZE	NS	NM	NM
PS	PM	PS	ZE	NS	NM	NM	NM
PM	PS	ZE	NM	NM	NB	NB	NB
PB	ZE	ZE	NB	NB	NB	NB	NB

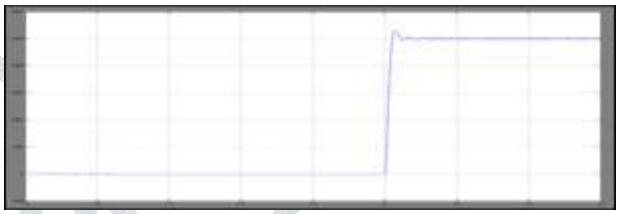
Fig. 18. Real and reactive power of converter1and converter2

Real power of converter 1

Reactive power of converter1



Real power of converter 1



Reactive power of converter1

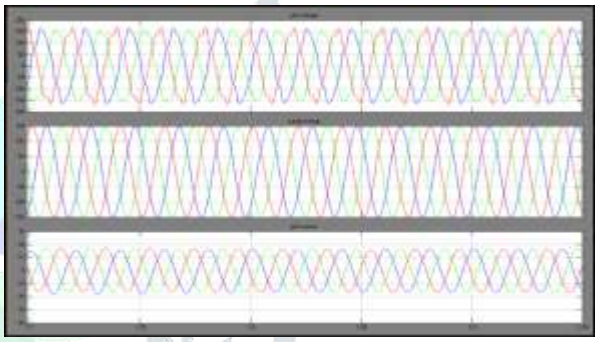


Fig. 20. The performance of the dual-converter system during 10% grid voltage sags, with 10.03% THD.

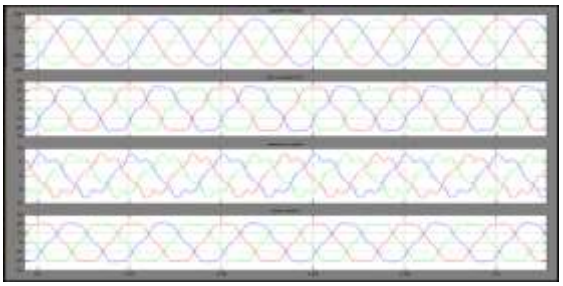
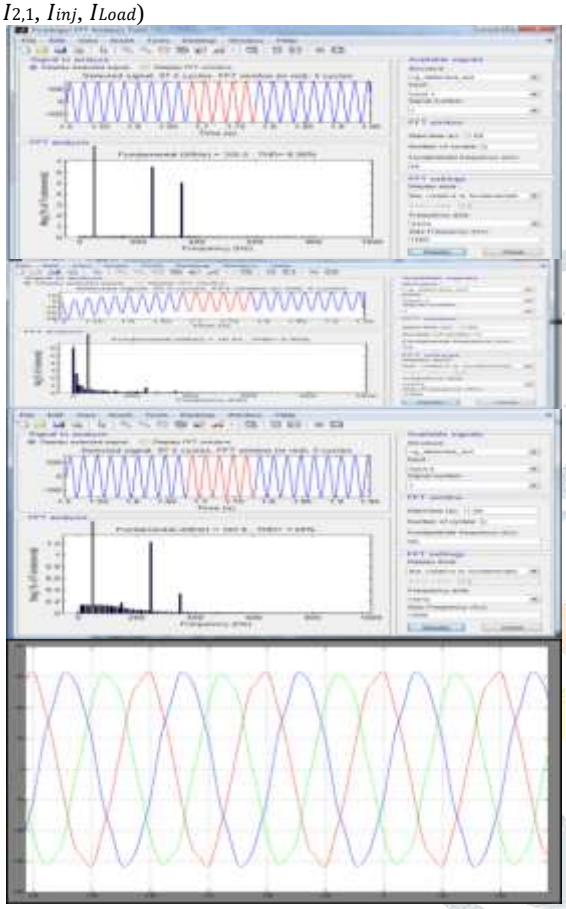
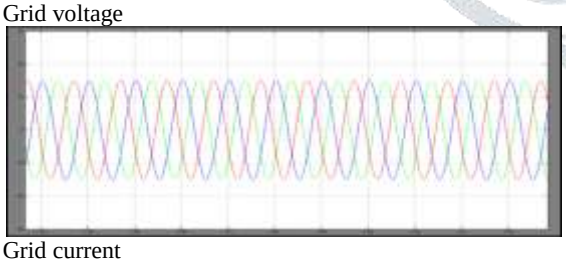


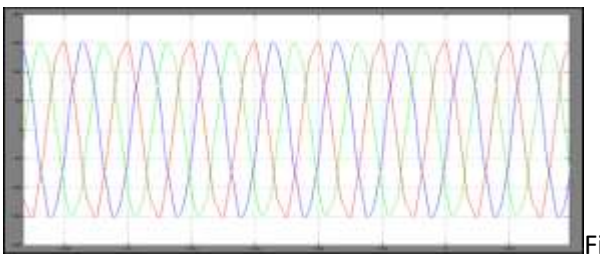
Fig. 13. Performance of converter1. (From upper to lower: V_{supply}, $I_{2,1}$, I_{inj}, I_{Load})



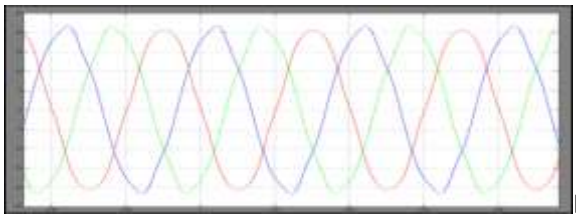
Grid voltage



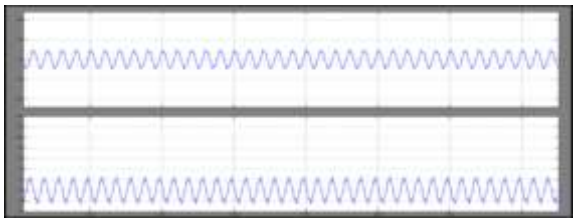
Grid current



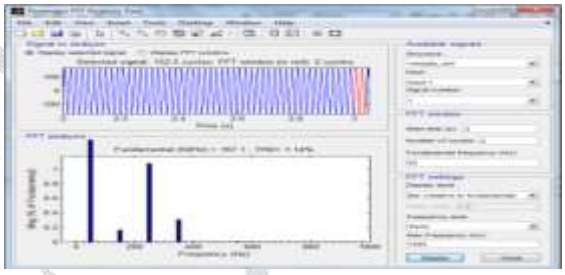
Filter capacitor voltage

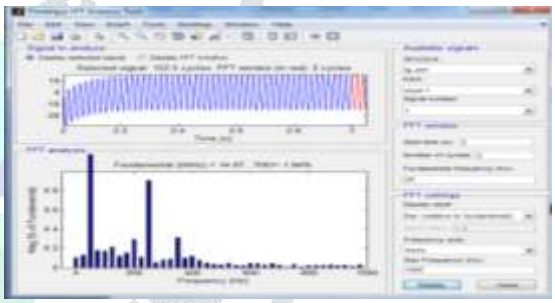


Line current



Harmonic current component





Conclusion

At the point when a single multi-useful interfacing converter is received to compensating generation the harmonic current from nearby nonlinear burdens, the nature of supply voltage to neighborhood load can barely be enhanced in the meantime, specific when the fundamental network voltage is blended. This paper examines a novel composed voltage and current controller for double converter system in which the nearby load is straightforwardly associated with the shunt capacitor of the primary converter. With the setup, the nature of supply voltage can be improved by means of a direct shut circle harmonic voltage control of filter capacitor voltage. In the meantime, the harmonic current brought on by the nonlinear load and the principal converter is repaid by the second converter. Consequently, the nature of the network current and the supply voltage are both essentially progressed. To lessen the computational heap of DG interfacing converter, the organized voltage and current control without utilizing load current/supply voltage harmonic extractions or stage bolt loops is produced to acknowledge to composed control of parallel converters.

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